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The technical content of this austriamicrosystems datasheet is still valid.

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AS1369

200mA Ultra-Compact Low Dropout Regulator

1 General Description

The AS1369 is an ultra compact high-performance low-dropout 200mA voltage regulator designed for use with very-low ESR output capacitors. The device can deliver superior performance in all specifications critical to battery-powered designs, and is perfectly suited for mobile phones, PDAs, MP3 players, and other battery powered devices.

The AS1369 is fully operational with small input and output capacitor of only 0.47µF offering PSRR of 72dB typical and a noise level of 30µVRMS.

Typical quiescent current is around 25µA while in shutdown the AS1369 requires less than 0.1µA quiescent current.

Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode.

The AS1369 offers excellent low-noise performance requiring no external bypass capacitance.

Multiple output voltage options between 1.2V and 5.0V in 100mV steps are available and the minimum input voltage is as low as 2.0V (depending on the output voltage version), so the component can be used with the new and emerging battery technologies.

The AS1369 is available in a 4-bump WL-CSP package.

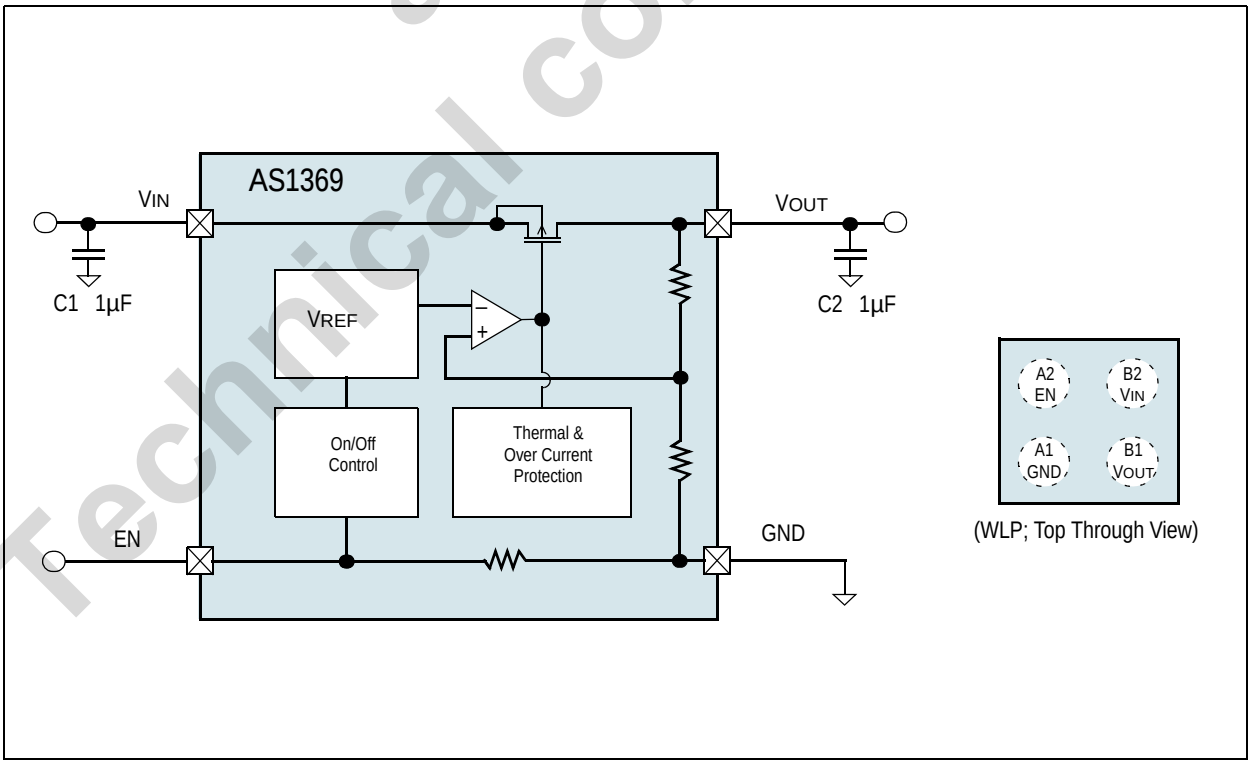
2 Key Features

- Low Dropout Voltage: typ. 40mV @ 100mA
- 200mA High Maximum Load Current
- 2.0V to 5.5V Input Voltage
- 1.2V to 5.0V Output Voltage (in 100mV steps)
- High Accuracy: ±2% Over Temperature
- Thermal and Over Current Protection
- 25µA Quiescent Current
- <0.1µA Standby Current
- High PSRR: 72dB @ 1kHz
- No Noise Bypass Capacitor Required
- Low Noise: 30µVRMS
- Enable Pin
- Package: 4-bump WL-CSP 0.5mm pitch

3 Applications

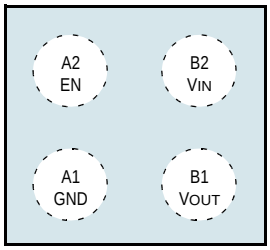
The device is ideal for mobile communication, battery powered systems and any electronic equipment.

Figure 1. AS1369 - Block Diagram



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



AS1369
(WLP; Top Through View)

4.1 Pin Descriptions

Table 1. Pin Descriptions

WLP	Name	Description
A1	GND	Ground
A2	EN	Logic-High Enable Input. $V_{IH} \geq 1.2V$: V_{OUT} is enabled. $V_{IH} \leq 0.4V$: V_{OUT} is disabled. **Note:** This pin is internally pulled down and must not float.
B1	V_{OUT}	Regulated Output Voltage
B2	V_{IN}	Input Voltage

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings[1]

Parameter	Min	Max	Units	Comments
Electrical Parameters				
Input Supply Voltage	-0.3	+7	V	
Shutdown Input Voltage	-0.3	+7	V	
Output Voltage	-0.3	+7	V	
I_{OUT}				Short-circuit protected
Input/Output Voltage[2]	-0.3	+7	V	
Latch-Up	-100	+100	mA	Norm: JEDEC 78
Electrostatic Discharge				
ESD		2	kV	Norm: MIL 883 E method 3015
		500	V	CDM JESD22-C101C methods
Temperature Ranges and Storage Conditions				
Thermal Resistance, θ_{JA} [3]		345	°C/W	The maximum allowable power dissipation is a function of the maximum junction temperature ($T_{J(MAX)}$), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_{AMB}). The maximum allowable power dissipation at any ambient temperature is calculated as: $P_{(MAX)} = (T_{J(MAX)} - (T_{AMB}))/\theta_{JA}$ (EQ 1) Where: The value of θ_{JA} for the WLP package is 345°C/W.
Operating Junction Temperature	-40	+125	°C	
Storage Temperature Range	-65	+150	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".*

1. The AS1369 uses an internal protective structure against light influence. However, exposing the WLP package to direct light could cause device malfunction.
2. The output PNP structure contains a diode between pins V_{IN} and V_{OUT} that is normally reverse-biased. reversing the polarity of pins V_{IN} and V_{OUT} will activate this diode.
3. Exceeding the maximum allowable dissipation will cause excessive device temperature and the regulator will go into thermal shutdown.

6 Electrical Characteristics

T_{AMB} = -40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5V, C_{OUT} = C_{IN} = 0.47µF, I_{OUT} = 1mA, V_{IH} = 1.2V (unless otherwise specified)

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{AMB}	Operating Temperature Range		-40		+85	ºC
	Operational Voltage Range		2.0		5.5	V
	Input Undervoltage Lockout			1.8		V
	Accuracy	Over full V_{IN}, V_{OUT}, T_{AMB} = 25°C including line and load regulation	-0.7		+0.7	%
		Over full V_{IN}, V_{OUT} and temperature including line and load regulation	-2		+2	
V_{DROP}	Dropout Voltage [1]	I_{OUT} = 50mA		20	50	mV
		I_{OUT} = 100mA		40	100	
		I_{OUT} = 150mA		60	150	
		I_{OUT} = 200mA		80	200	
ΔV_{OUT}	Line Regulation	V_{IN} = $V_{OUT(NOM)}$ + 0.5V to 5.5V, $V_{OUT} \geq$ 2.5V		0.02	0.1	%/V
		V_{IN} = $V_{OUT(NOM)}$ + 0.5V to 5.5V, V_{OUT} < 2.5V		0.02	0.2	
	Load Regulation	I_{OUT} = 5 to 100mA		0.001	0.003	%/mA
		I_{OUT} = 5 to 200mA		0.001	0.003	
ΔV_{OUT} / ΔT_{AMB}	Output voltage/temperature	I_{OUT} = 5mA		50		ppm/°C
	Output current	Maximum output current	210			mA
I_Q	Quiescent current	I_{LOAD} = 0mA		25	50	µA
		I_{LOAD} = 200mA		35	60	µA
I_{SHDN}	Standby current	In Shutdown		5	500	nA
t_{ON}	Turn On Time [2]			30		µs
	PSRR	I_{OUT} = 10mA, f = 1kHz, V_{OUT} = 1.5V		72		dB
		I_{OUT} = 10mA, f = 100kHz, V_{OUT} = 1.5V		55		dB
		I_{OUT} = 10mA, f = 1kHz, V_{OUT} = 2.8V		80		dB
		I_{OUT} = 10mA, f = 100kHz, V_{OUT} = 2.8V		56		dB
	Load transient response	1 to 150mA, T_{rise} = T_{fall} = 1µs, C_{OUT} = C_{IN} = 1µF, ESR load capacitor = 0		±65		mV
eN	Output Noise Voltage	BW = 400Hz to 80kHz, C_{OUT} = 1µF, I_{OUT} = 30mA		30		μV_{RMS}
I_{EN}	Enable Input Current	V_{EN} = 0.4V, V_{IN} = 5.5V		±1		µA
V_{EN}	Enable Input Logic Low	V_{IN} = 2.0V to 5.5V, T_{AMB} = -40°C to 85°C			0.4	V
	Enable Input Logic High		1.2			
$I_{IN(start)}$	Startup Peak Current	I_{OUT} = 0mA		340		mA
I_{SC}	Short Circuit Current	V_{OUT} = 0V	210	350		mA
T_{OFF}	Temperature Shutdown	Temperature rising		160		ºC
		Hysteresis		20		
C_{OUT}	Output Capacitor	Load Capacitor Range	0.47			µF
		Maximum ESR Load			0.5	Ω

1. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value (does not apply to input voltages below 2.0V).
2. Turn on time is time measured between the enable input just exceeding the V_{EN} high value and the output voltage just reaching 95% of its nominal value.

Figure 3. AC Line Regulation Input Voltage Test Signal

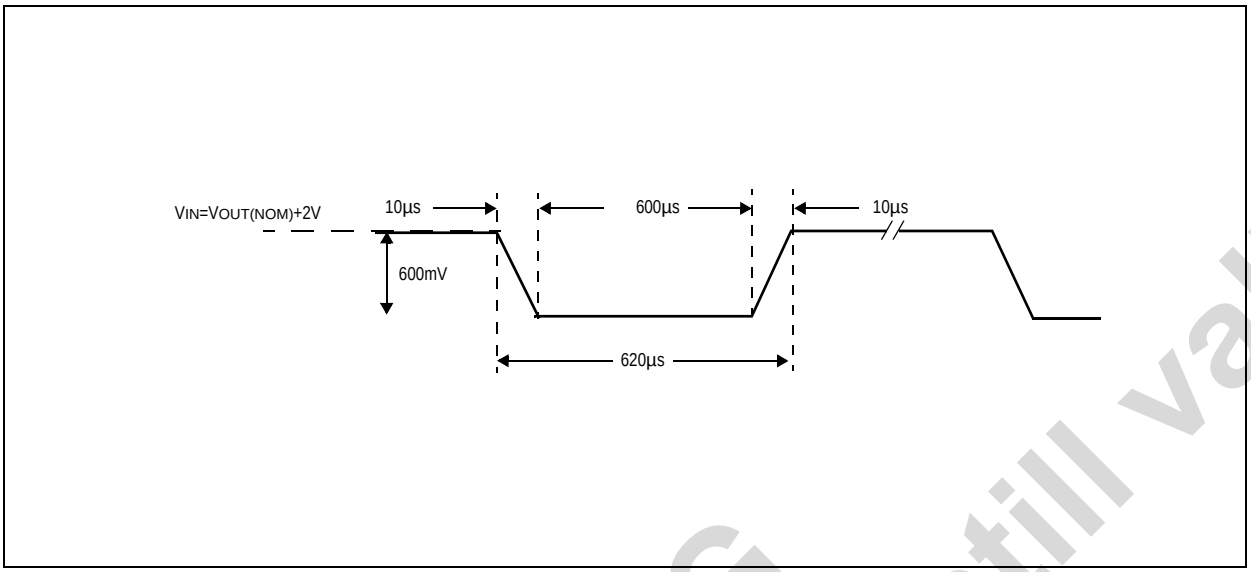
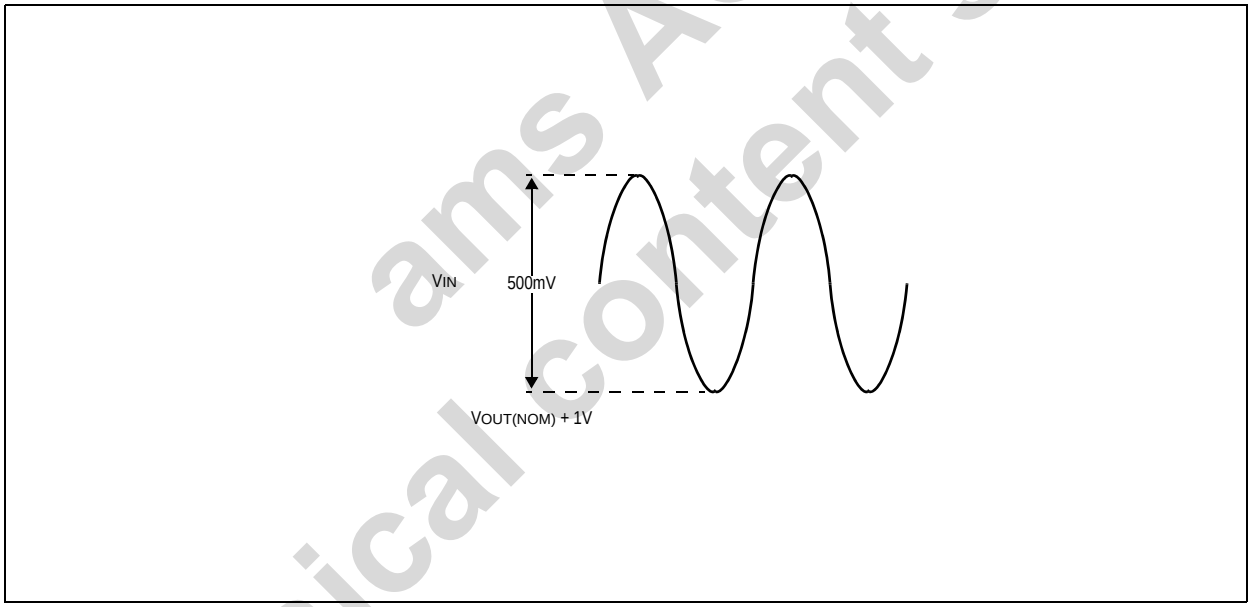


Figure 4. SVR Input Voltage Test Signal



7 Typical Operating Characteristics

V_{IN} = V_{OUT} + 0.5V, C_{IN} = C_{OUT} = 1µF, T_{AMB} = 25°C (unless otherwise specified).

Figure 5. ΔVOUT vs. VIN; VOUT(NOM)=1.5V

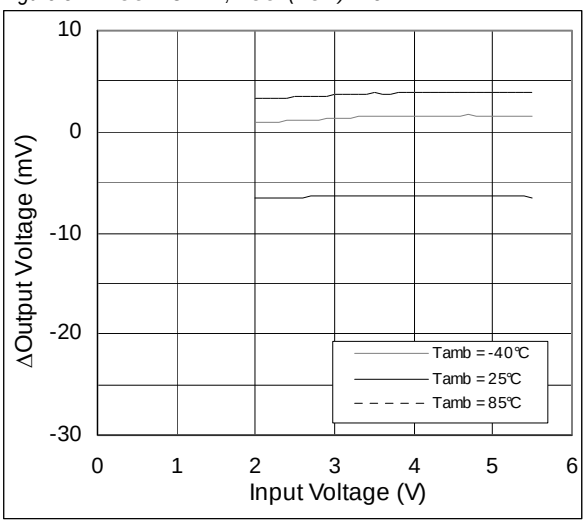


Figure 6. ΔVOUT vs. VIN; VOUT(NOM)=2.8V

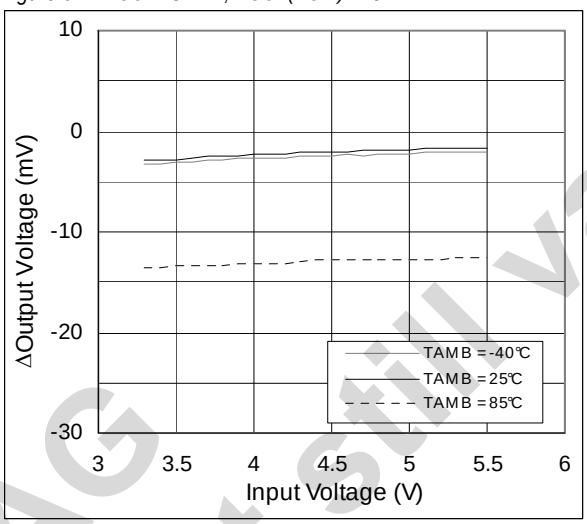


Figure 7. ΔVOUT vs. (VIN-VOUT); TAMB = -40°C

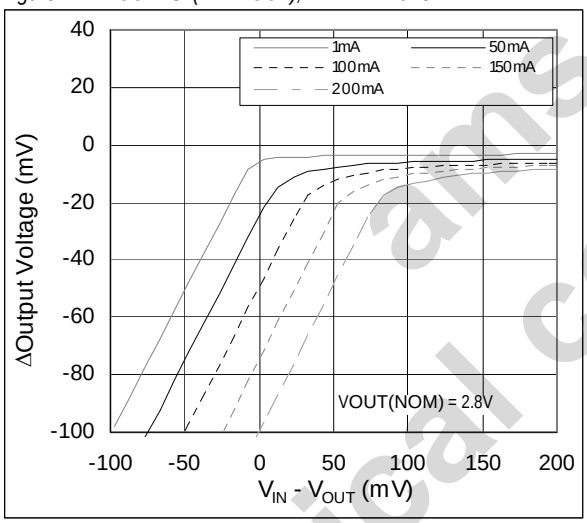


Figure 8. ΔVOUT vs. (VIN-VOUT); TAMB = +25°C

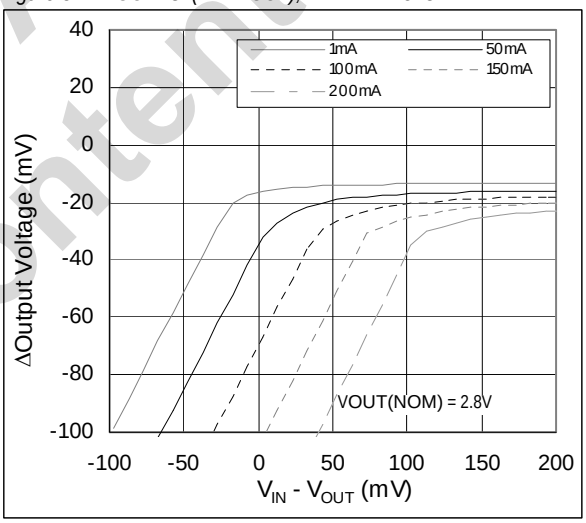


Figure 9. ΔVOUT vs. (VIN-VOUT); TAMB = +85°C

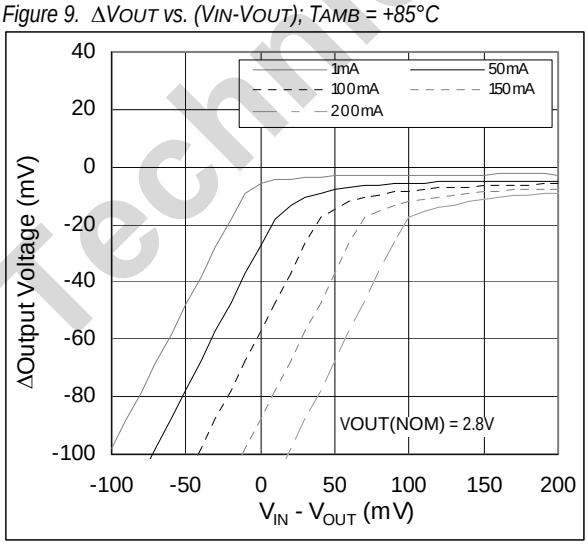


Figure 10. Dropout Voltage vs. IOUT; VOUT=2.8V

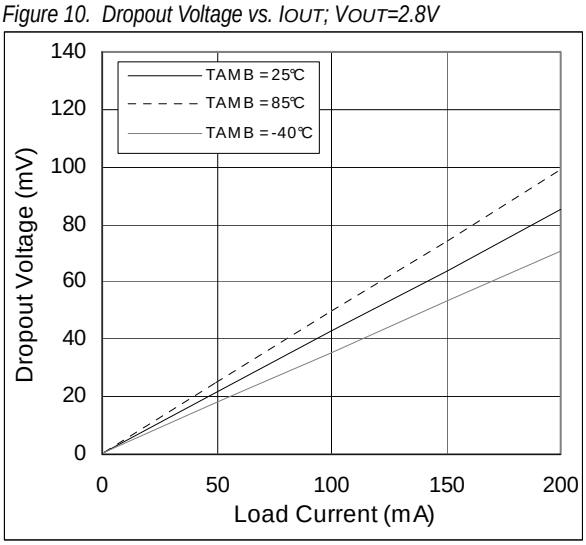


Figure 11. VOUT vs. IOUT; VOUT(NOM)=1.5V

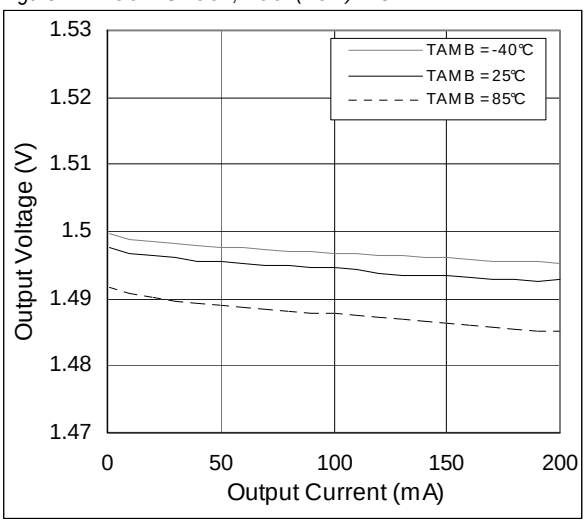


Figure 12. VOUT vs. IOUT; VOUT(NOM)=2.8V

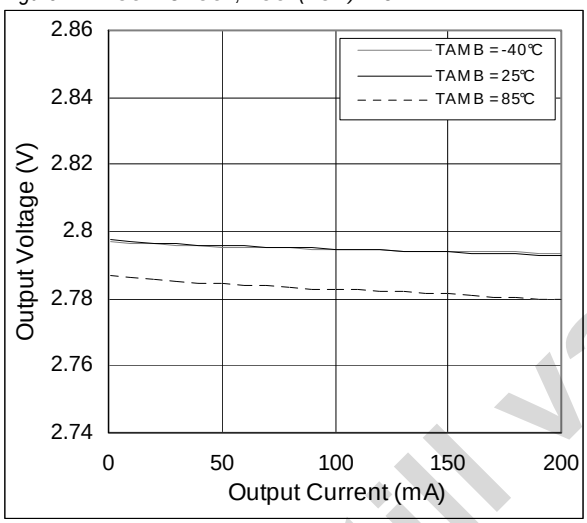


Figure 13. ΔVOUT vs. IOUT; VOUT(NOM)=1.5V

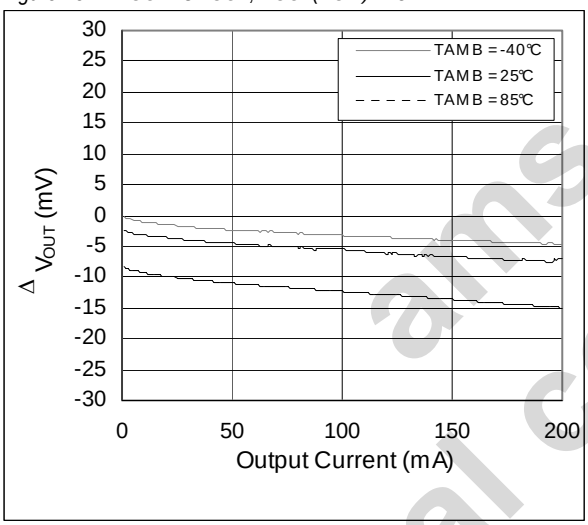


Figure 14. ΔVOUT vs. IOUT; VOUT(NOM)=2.8V

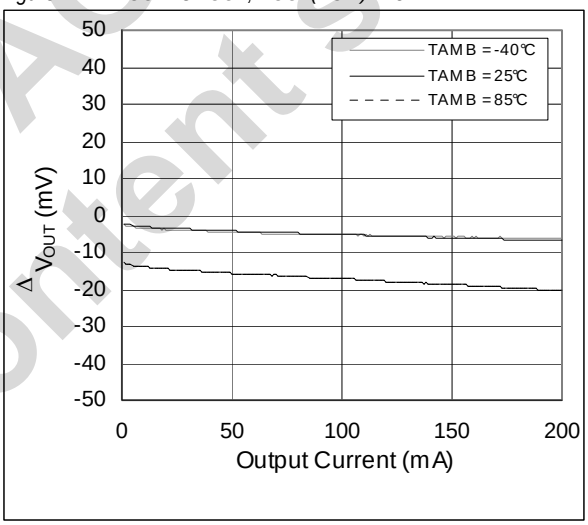


Figure 15. ΔVOUT vs. Temperature; VOUT(NOM)=1.5V

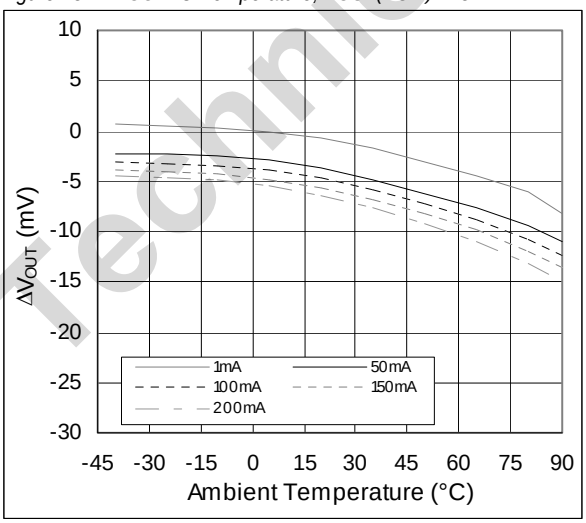


Figure 16. ΔVOUT vs. Temperature; VOUT(NOM)=2.8V

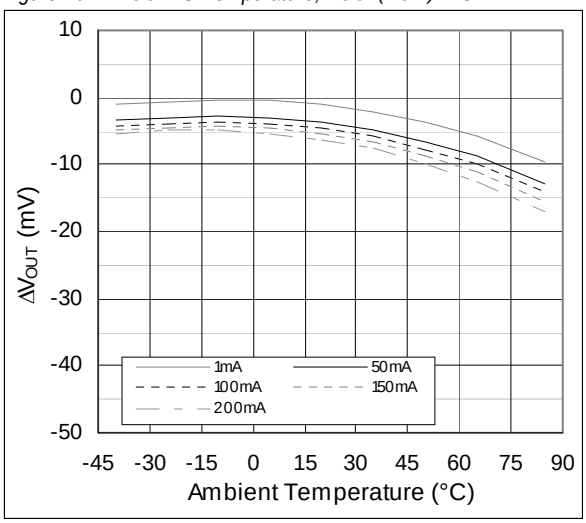


Figure 17. Dropout Voltage vs. Temperature; VOUT=2.8V

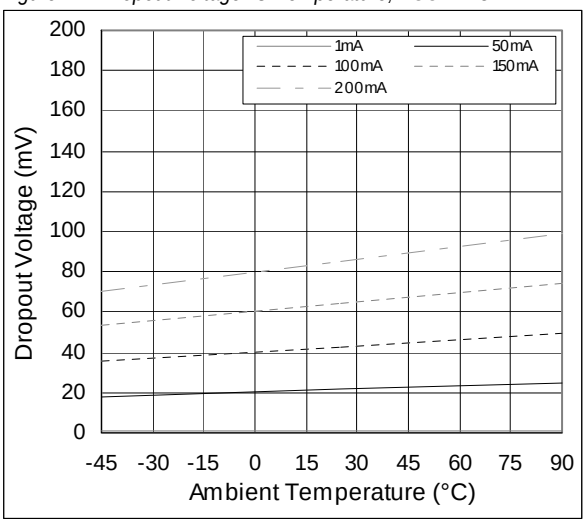


Figure 18. IOUT(MAX) vs. Temperature

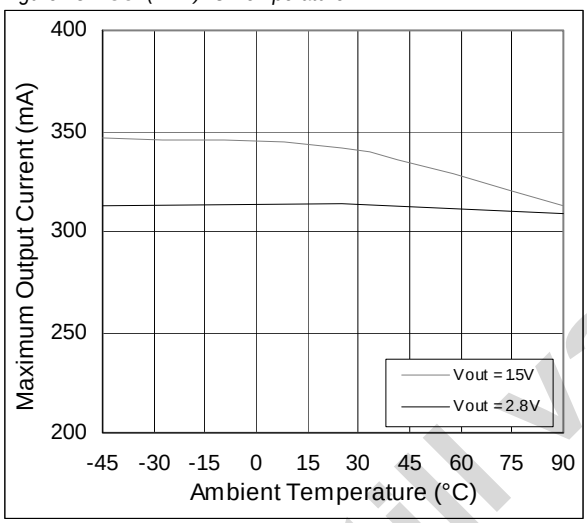


Figure 19. Quiescent Current vs. VIN

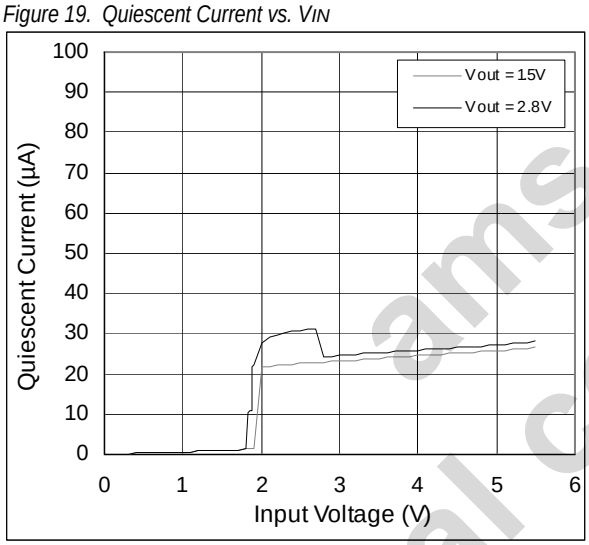


Figure 20. Standby Current vs. VIN

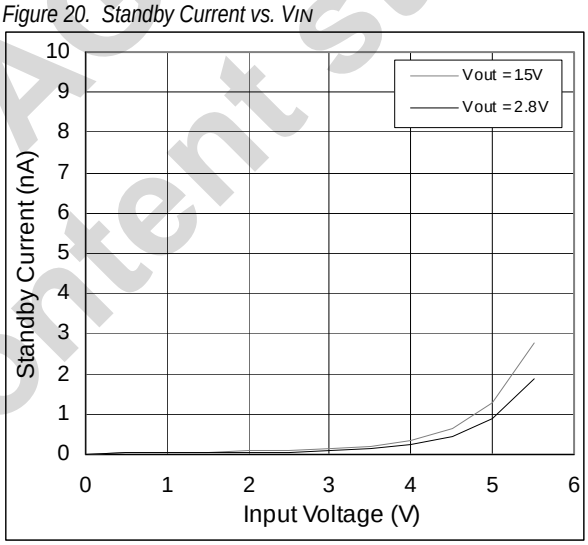


Figure 21. Ground Current vs. IOUT

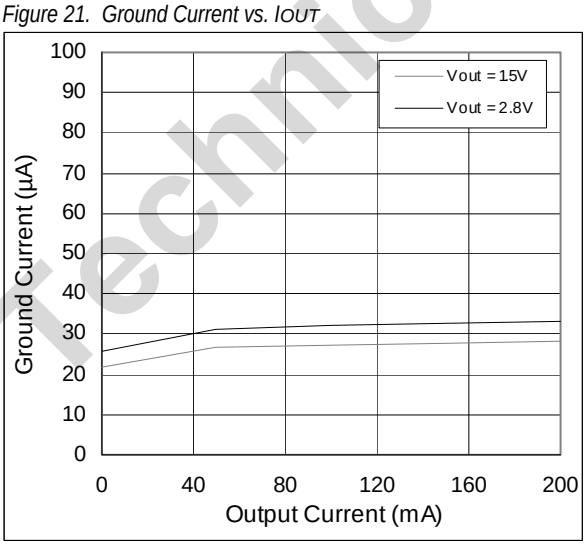


Figure 22. Quiescent Current vs. Temperature

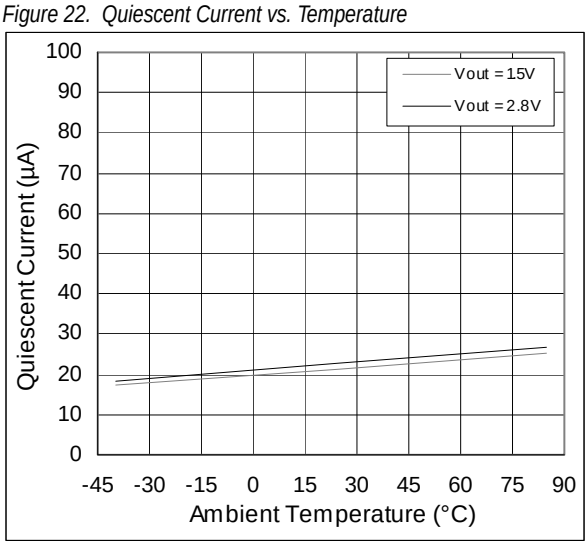


Figure 23. Ground Current vs. Temperature; VOUT=1.5V

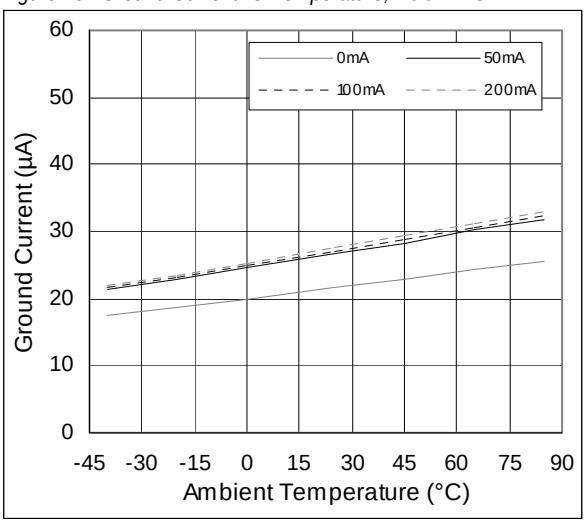


Figure 24. Ground Current vs. Temperature; VOUT=2.8V

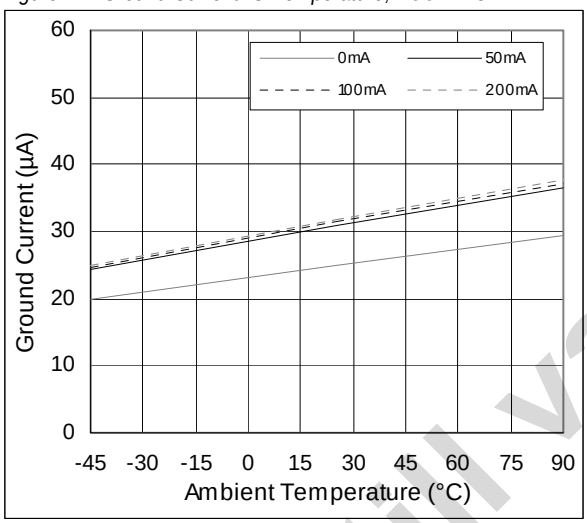


Figure 25. IEN vs. VOUT; VOUT=1.5V

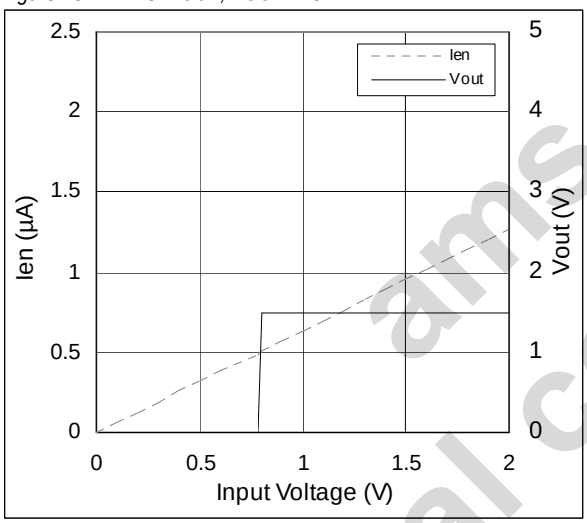


Figure 26. IEN vs. VOUT; VOUT=2.8V

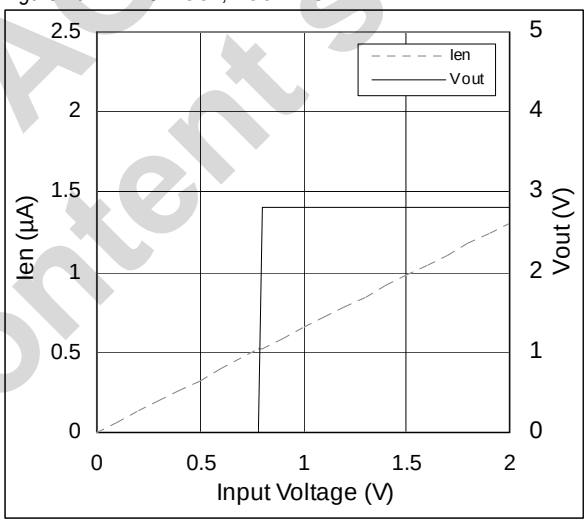


Figure 27. VEN vs. Temperature

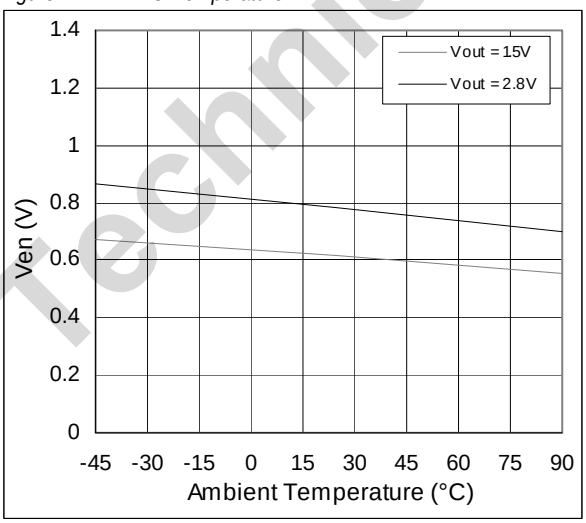


Figure 28. IEN vs. Temperature

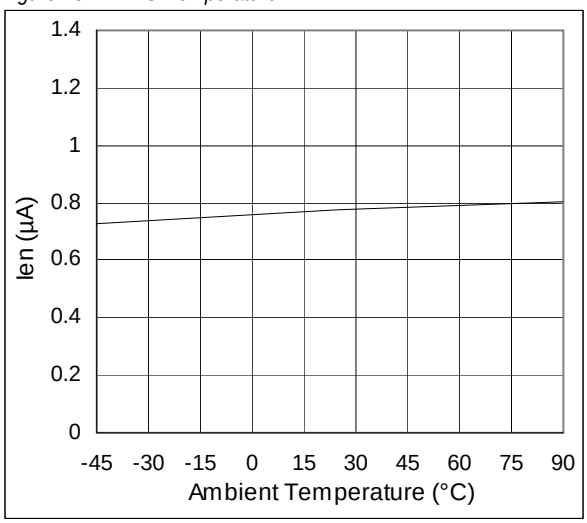


Figure 29. PSRR vs. VIN-VOUT(NOM), VOUT=1.5V

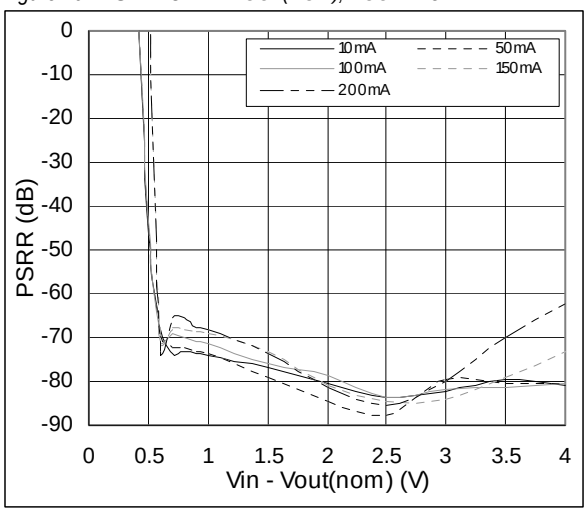


Figure 30. PSRR vs. VIN-VOUT(NOM), VOUT=2.8V

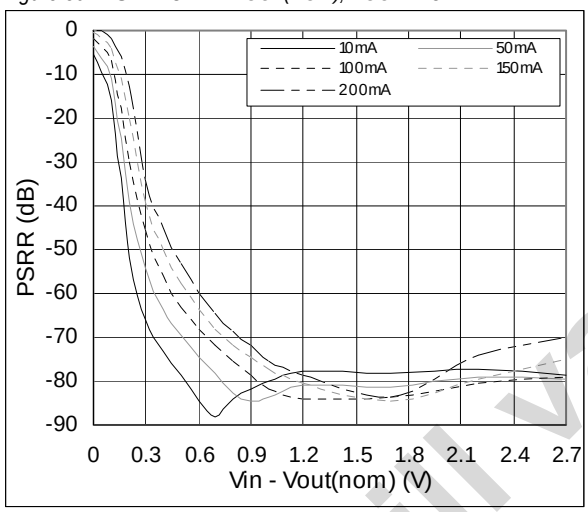


Figure 31. PSRR vs. Frequency, IOUT=10mA

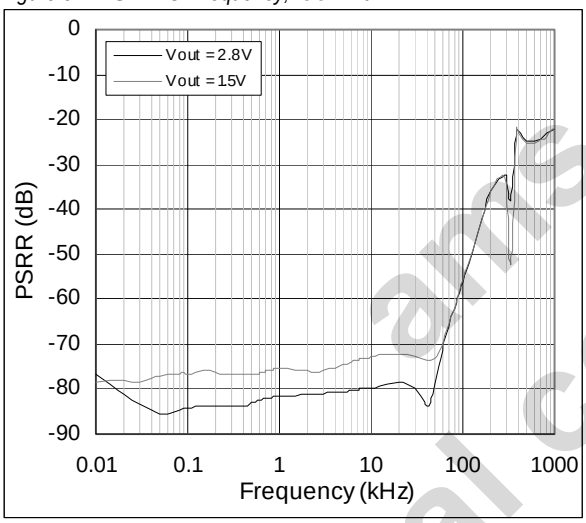


Figure 32. Spectral Noise vs. Frequency, IOUT=10mA

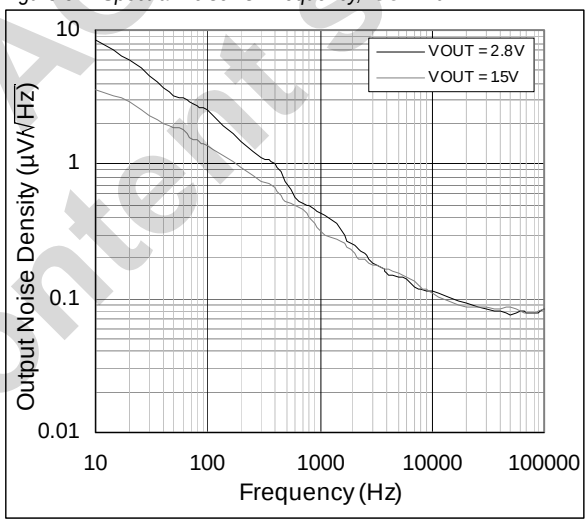


Figure 33. Voltage Noise vs. VOUT, IOUT=30mA

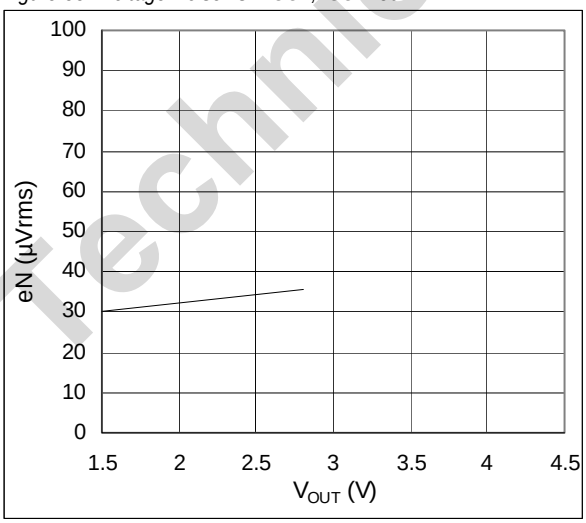


Figure 34. Line Transient Response; IOUT=50mA, VOUT=1.5V, VIN=3.5V to 2.9V

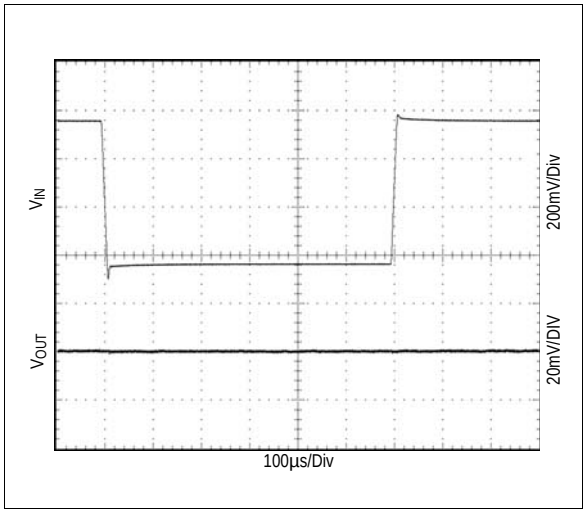


Figure 35. Line Transient Response; IOUT=50mA, VOUT=2.8V, VIN=4.8V to 4.2V

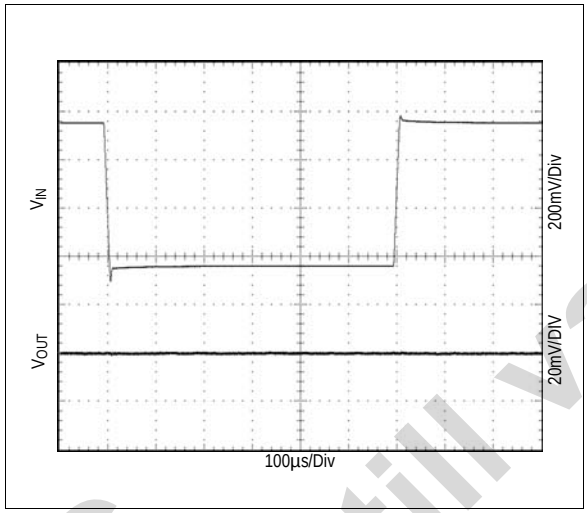


Figure 36. Line Transient Response; IOUT=100mA, VOUT=1.5V, VIN = 3.5V to 2.9V

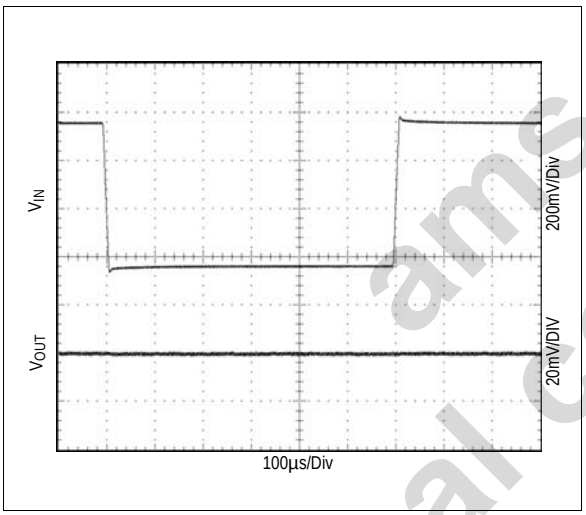


Figure 37. Line Transient Response; IOUT=100mA, VOUT=2.8V, VIN=4.8V to 4.2V

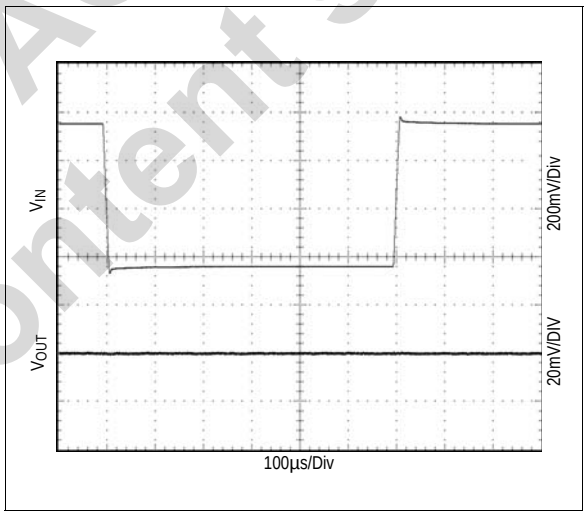


Figure 38. Line Transient Response; IOUT=200mA, VOUT=1.5V, VIN=3.5V to 2.9V

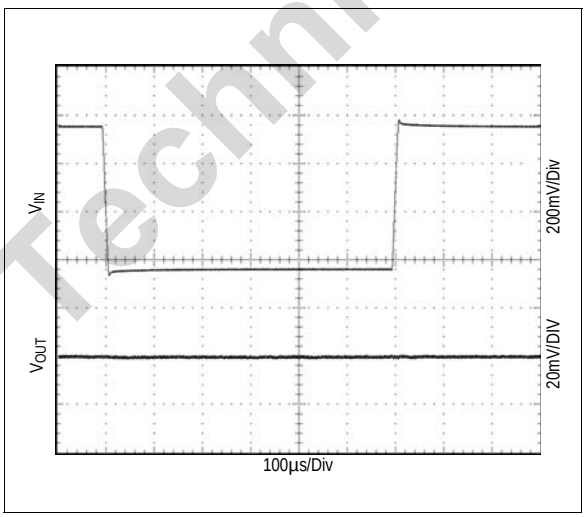


Figure 39. Line Transient Response; IOUT=200mA, VOUT=2.8V, VIN=4.8V to 4.2V

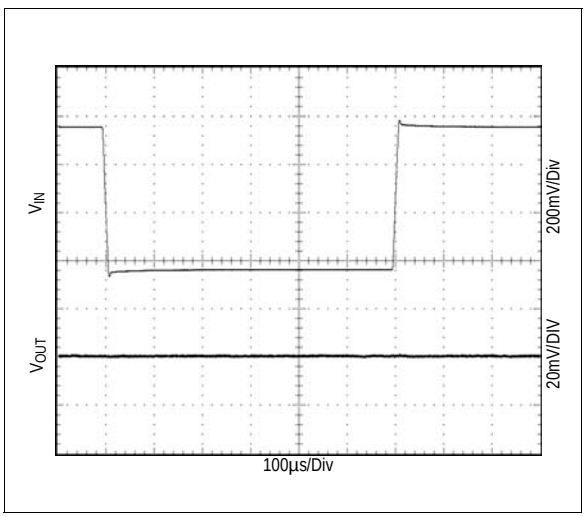


Figure 40. Load Transient; IOUT= 0mA to 150mA VIN=2.0V, VOUT=1.5V

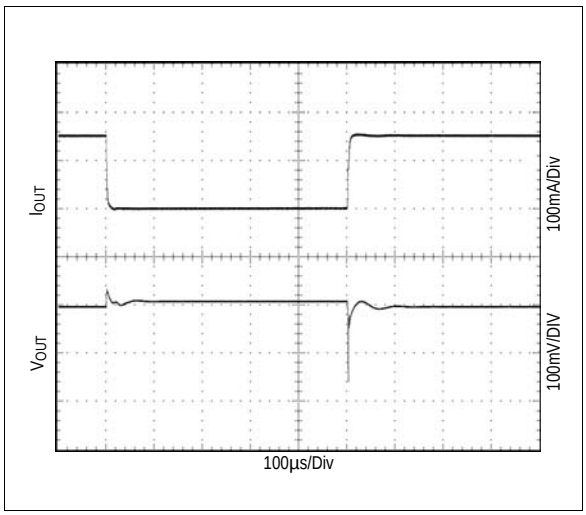


Figure 41. Load Transient; IOUT= 0mA to 150mA VIN=3.3V, VOUT=2.8V

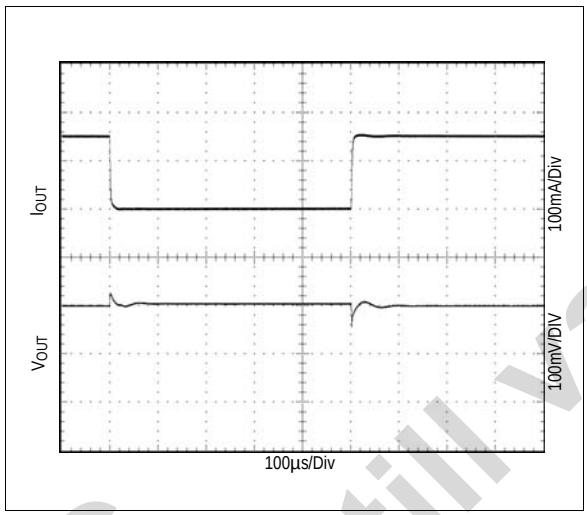


Figure 42. Load Transient; IOUT= 0mA to 150mA VIN=3.0V, VOUT=2.8V, in Dropout

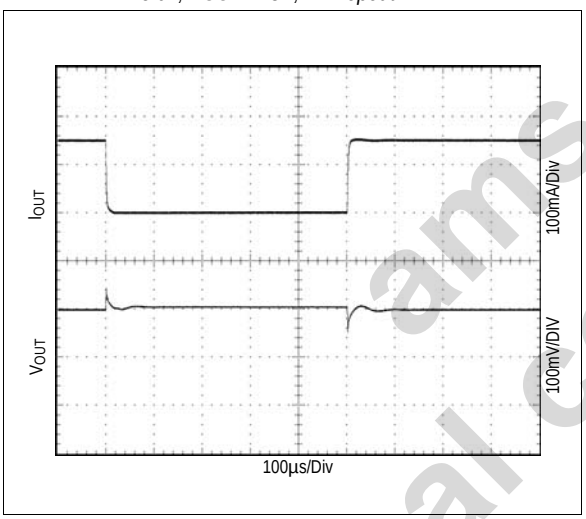


Figure 43. Load Transient; IOUT= 1mA to 150mA VIN=3.0V, VOUT=2.8V, in Dropout

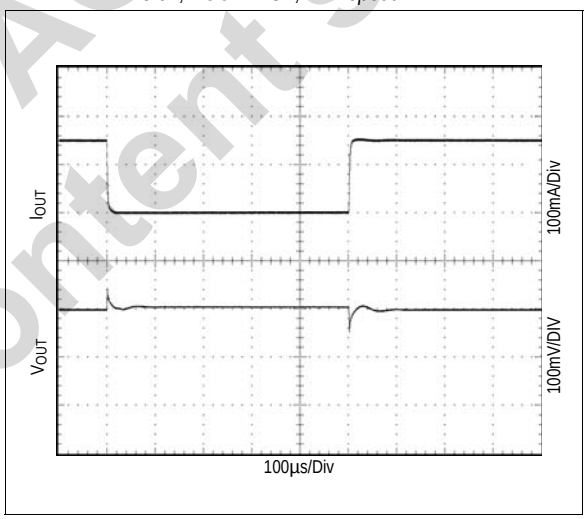


Figure 44. Startup

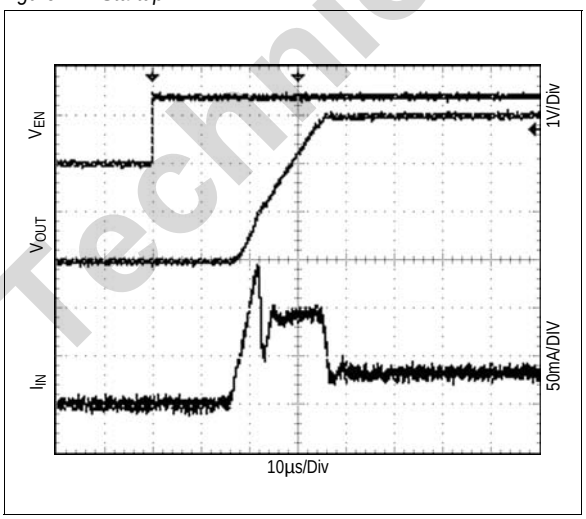
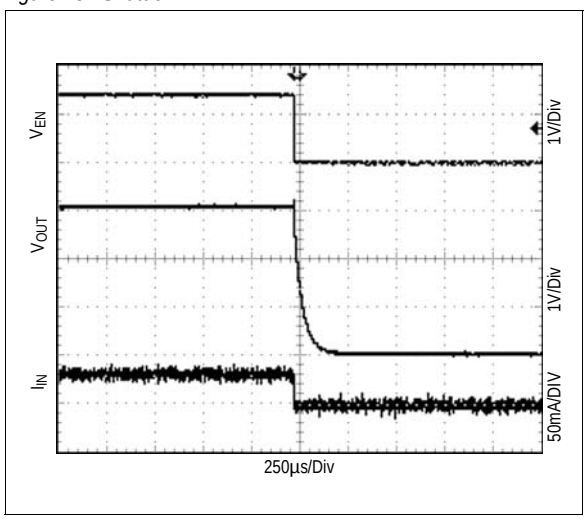


Figure 45. Shutdown



8 Application Information

Figure 46. Typical Application Diagram

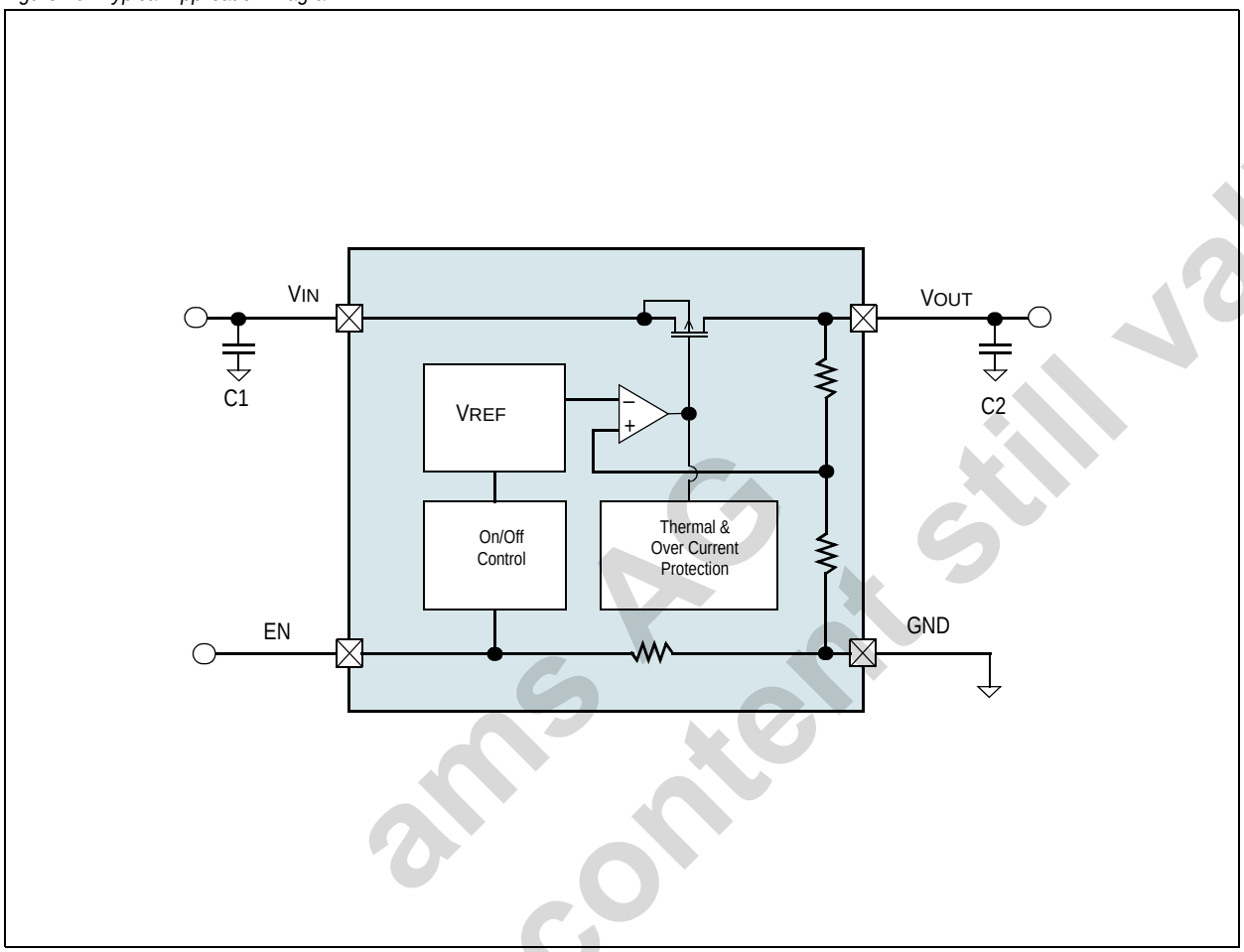


Figure 46 shows the block diagram of the AS1369. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (REF in Figure 46) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

8.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different load currents, but is usually specified at maximum output. As a result, the MOSFET maximum series resistance over temperature is obtained. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 2)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 47. Graphical Representation of Dropout Voltage

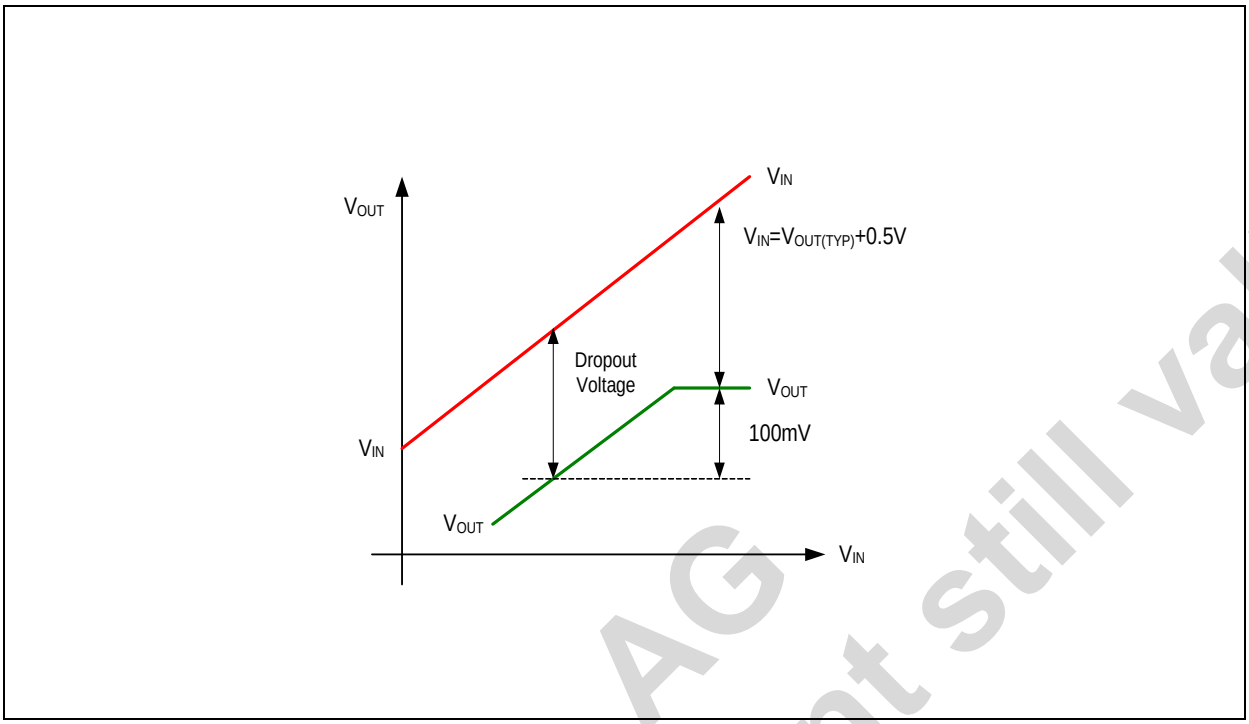


Figure 47 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT - VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

8.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$Efficiency = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \qquad \text{(EQ 3)}$$

Where:
IQ = Quiescent current of LDO

8.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)})\ \ Watts \qquad \text{(EQ 4)}$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)} I_Q\ \ Watts \qquad \text{(EQ 5)}$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias)\ \ Watts \qquad \text{(EQ 6)}$$

8.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125°C (unless otherwise specified in the datasheet). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}°C/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}°C/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 48. Package Physical Arrangements

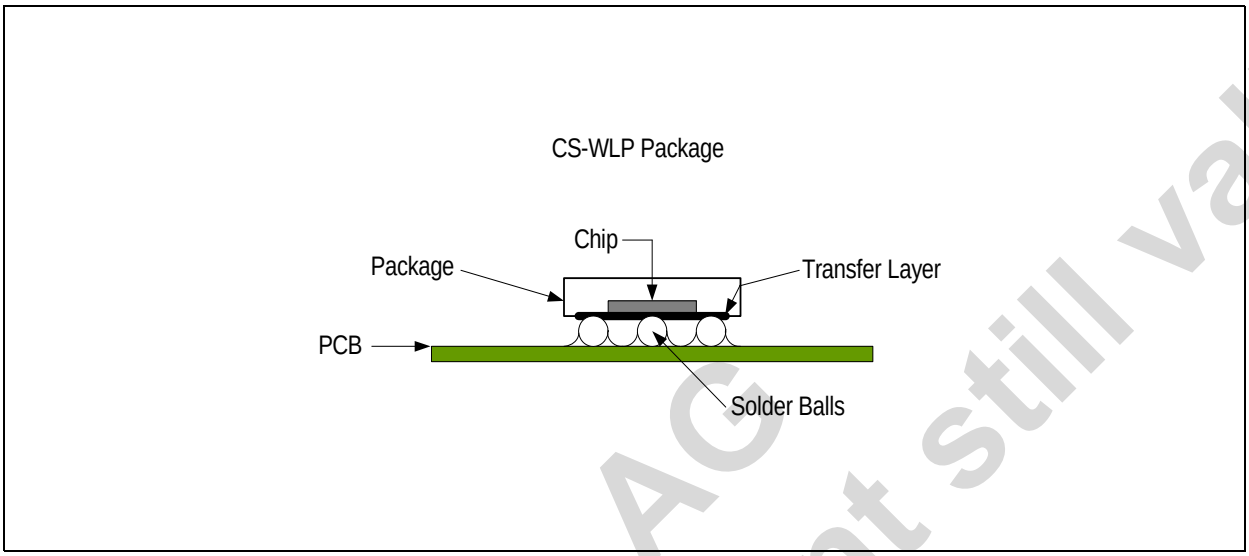
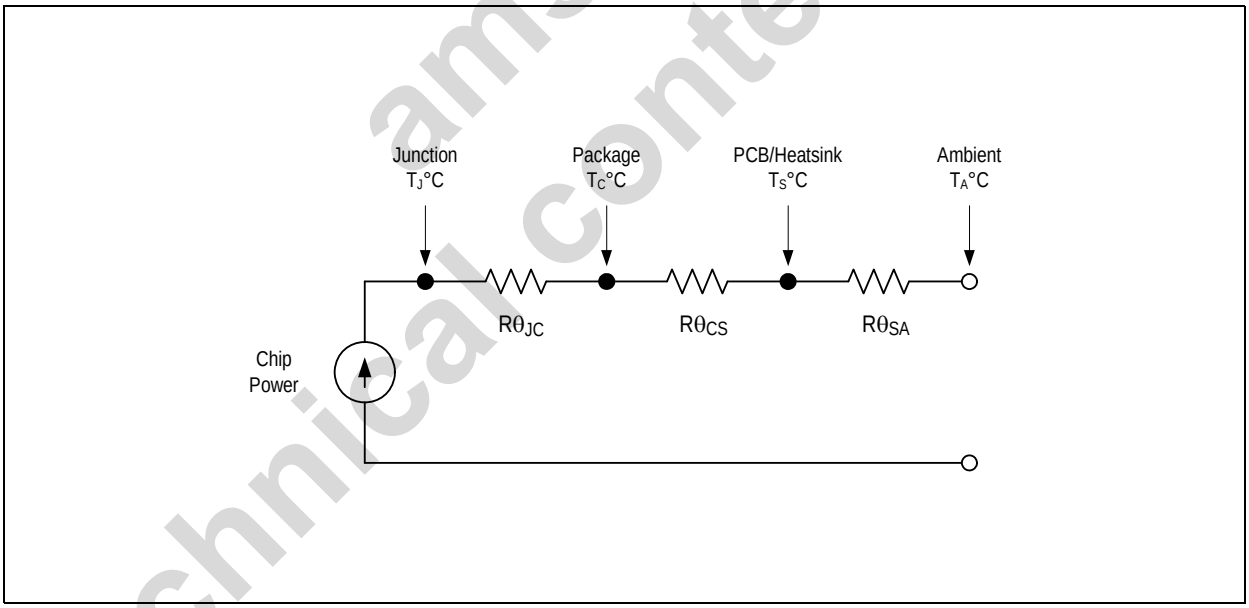


Figure 49. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \text{(EQ 7)}$$

Junction Temperature (T_J °C) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB}\ ^oC \quad \text{(EQ 8)}$$

8.5 Explanation of Steady State Specifications

8.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \textit{ and is a pure number} \qquad \textit{(EQ 9)}$$

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \textit{ \% / V} \qquad \textit{(EQ 10)}$$

8.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \textit{ and is units of ohms } (\Omega) \qquad \textit{(EQ 11)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{V_{OUT}} \textit{ \% / mA} \qquad \textit{(EQ 12)}$$

8.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \qquad \textit{(EQ 13)}$$

The reference tolerance is given both at 25°C and over the full operating temperature range.

8.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

$$\textit{Total \% Accuracy = Setting \% Accuracy + Load Regulation \% + Line Regulation \%} \qquad \textit{(EQ 14)}$$

8.6 Explanation of Dynamic Specifications

8.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$\textit{PSRR} = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}} \textit{ dB using lower case } \delta \textit{ to indicate AC values} \qquad \textit{(EQ 15)}$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

8.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a maximum value in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with variations in temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below TAMB = -10°C. With X7R or X5R capacitors, a 1µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF) help to reduce noise and improve load transient-response, stability and power-supply rejection.

8.6.3 Input Capacitor

An input capacitor at VIN is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1369 power supply input pin VIN and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the VIN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

8.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

8.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \textit{Units are Volts, Amps, Ohms.} \qquad \textit{(EQ 16)}$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}} \right) \quad \textit{Units are Volts, Seconds, Farads, Ohms.} \qquad \textit{(EQ 17)}$$

Where:
CLOAD is output capacitor
T= Propagation Delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

8.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at VIN is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

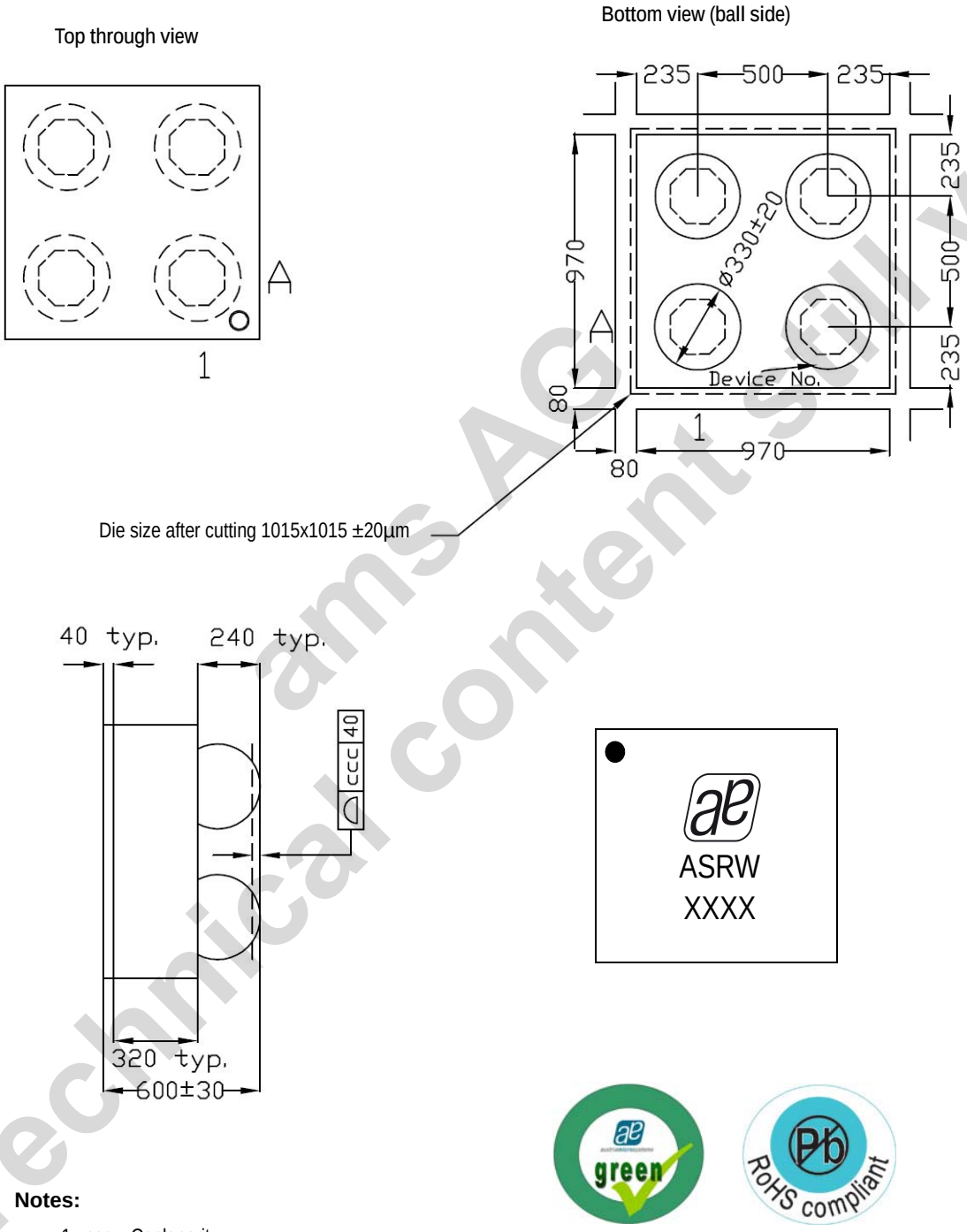
8.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 150°C threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 20°C prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

9 Package Drawings and Markings

The AS1369 is available in a 4-bump WL-CSP package.

Figure 50. 4-bump WL-CSP Package



Notes:

1. ccc – Coplanarity
2. All dimensions are in µm.

Revision History

Revision	Date	Owner	Description
1.4			Initial revision
1.5			Package marking updated
1.6	21 Sep, 2011	afe	Changes made across the document
1.7	12 Dec, 2011		Updated equations in Power Dissipation section

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The AS1369 is available as the standard versions listed in Table 4. Other versions are available upon request. Contact *austriamicrosystems*, AG for more information.

Table 4. Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1369-BWLT-12	ASRW	1.2V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-13	ASRX	1.3V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-15	ASPZ	1.5V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-18	ASP0	1.8V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-25	ASP1	2.5V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-28	ASP2	2.8V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-30	ASP3	3.0V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-33	ASP4	3.3V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-45[1]	ASP5	4.5V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP
AS1369-BWLT-50[1]	ASP6	5.0V	200mA Ultra-Compact Low Dropout Regulator	Tape and Reel	4-bump WL-CSP

1. Available upon request. Contact *austriamicrosystems AG* for details.

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