PIC16F91X/946

PIC16F91X/946 Family
Silicon Errata and Data Sheet Clarification

The PIC16F91X/946 family devices that you have received conform functionally to the current Device Data Sheet (DS41250**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F91X/946 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision.

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2, MPLAB ICD 3, PICkit™ 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 and MPLAB ICD 3 programmer/debugger, PICkit™ 2 or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Programmer>Select Tool*).
4. Perform a "Connect" operation to the device (*Programmer>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device ID values for the various devices and silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)							
		A0	A1	A2	A3	B0	B1	B2	B3
PIC16F913	13Exh	0	0	1	2				
PIC16F914	13Cxh	0	0	1	2				
PIC16F916	13Axh	0	0	1		2	2	3	4
PIC16F917	138xh	0	0	1		2	2	3	4
PIC16F946	146xh	0	0	1					

Note 1: The device and revision data is stored in the Device ID located at 2006h in program memory.

2: Refer to the *"PIC16F91X/946 Memory Programming Specification"* (DS41244) for detailed information.

TABLE 2: SILICON ISSUE SUMMARY (PIC16F913/914)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A0	A1	A2	A3			
LCD	Type B	1.	Incorrect waveforms.	x	x	x	x			
Timer1	LP	2.	Low drive as temp. approaches -40°C.	x	x	x	x			
Timer1	Ext. Crystal	3.	Overflow may take additional count.	x	x	x	x			
Timer0/ WDT	Prescaler	4.	Reset under specific conditions.	x	x	x	x			

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 3: SILICON ISSUE SUMMARY (PIC16F916/917)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A0	A1	A2	B0	B1	B2	B3
LCD	Type B	1.	Incorrect waveforms.	x	x	x	x	x	x	x
Timer1	LP	2.	Low drive as temp. approaches -40°C.	x	x	x	x	x	x	x
Timer1	Ext. Crystal	3.	Overflow may take additional count.	x	x	x	x	x	x	x
Timer0/ WDT	Prescaler	4.	Reset under specific conditions.	x	x	x	x	x	x	x

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 4: SILICON ISSUE SUMMARY (PIC16F946)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A0	A1	A2				
LCD	Type B	1.	Incorrect waveforms.	x	x	x				
Timer1	LP	2.	Low drive as temp. approaches -40°C.	x	x	x				
Timer1	Ext. Crystal	3.	Overflow may take additional count.	x	x	x				
Timer0/ WDT	Prescaler	4.	Reset under specific conditions.	x	x	x				

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (as applicable).

1. Module: LCD

The LCD module may generate incorrect waveforms when using type-B waveforms (WFT = 1) with one-third multiplex (LMUX<1:0> = 10).

Work around

Avoid the use of type-B waveforms with one-third multiplex. When one-third is required, use type-A waveforms.

Affected Silicon Revisions

PIC16F913/914

A0	A1	A2	A3				
X	X	X	X				

PIC16F916/917

A0	A1	A2	B0	B1	B2	B3	
X	X	X	X	X	X	X	

PIC16F946

A0	A1	A2					
X	X	X					

2. Module: LP/Timer1 Oscillator Operation Below 25°C

1-2% of devices experience reduced drive as temperatures approach -40°C. This will result in a loss of Timer1 counts or stopped Timer1 oscillation.

This can also prevent Timer1 oscillator start-up under cold conditions.

Work around

Use of low-power crystals properly matched to the device will reduce the likelihood of failure. A 1MΩ resister between OSC2 and V_{DD} will further improve the drive strength of the circuit.

Affected Silicon Revisions

PIC16F913/914

A0	A1	A2	A3				
X	X	X	X				

PIC16F916/917

A0	A1	A2	B0	B1	B2	B3	
X	X	X	X	X	X	X	

PIC16F946

A0	A1	A2					
X	X	X					

3. Module: Asynchronous Timer1

This Errata supersedes Errata DS80329.

When TImer1 is started or updated, the timer needs to see a falling edge from the external clock source before a rising edge can increment the counter. If writes to TMR1H and TMR1L are not completed while the external clock pulse is still high, Timer1 will not count the first clock pulse after the update.

When using an external crystal, the pulse width from rising to falling edge is temperature dependent and may decrease with temperature. As a result, the timer may require an additional oscillation to overflow.

Work around

Switching to the HFINTOSC after reloading, the timer ensures the Timer1 will see a falling edge before switching back to the external clock source.

Due to the time from Timer1 overflow to the reload being application specific, wait for the timer to increment before beginning the reload sequence. This ensures the timer does not miss a rising edge during reload.

EXAMPLE 1:

```
    BTFSC   TMR1L,0
    GOTO    $-1
    BTFSS   TMR1L,0
    GOTO    $-1             ;Timer has just incremented, 31 µs before next rising edge to
                            ;complete reload

Update:

    BCF     T1CON,TMR1CS    ;Select HFINTOSC for Timer1
    BSF     TMR1H,7         ;Timer1 high byte 0x80
    BCF     T1CON,TMR1ON    ;Timer1 off
    BSF     T1CON,TMR1CS    ;Select external crystal
    BCF     T1CON,TMR1ON    ;Timer1 on


    Critical Timing of code sequence for instructions following last write to TMR1L or TMR1H.
```

Affected Silicon Revisions

PIC16F913/914

A0	A1	A2	A3				
X	X	X	X				

PIC16F916/917

A0	A1	A2	B0	B1	B2	B3	
X	X	X	X	X	X	X	

PIC16F946

A0	A1	A2					
X	X	X					

4. Module: Timer0 and WDT Prescaler Assignment Spurious Reset

A spurious Reset may occur if the Timer0/Watchdog Timer (WDT) prescaler is assigned from the WDT to Timer0 and then back to the WDT.

Summary

The issue only arises when all of the below conditions are met:

- Timer0 external clock input (TOCKI) is enabled.
- The Prescaler is assigned to the WDT, then to the Timer0 and back to the WDT.
- During the assignments, the T0CKI pin is high when bit TOSE is set, or low when TOSE is clear.
- The 1:1 Prescaler option is chosen.

Description

On a POR, the Timer0/WDT prescaler is assigned to the WDT.

If the prescaler is reassigned to Timer0 and Timer0 external clock input (TOCKI) is enabled then the prescaler would be clocked by a transition on the TOCKI pin.

On power-up, the TOCKI pin is (by default) enabled for Timer0 in the OPTION register.

If the T0CKI pin is:

- High and Timer0 is configured to transition on a falling edge (TOSE set), or
- Low and Timer0 is configured to transition on a rising edge (TOSE clear)

Then, if the prescaler is reassigned to the WDT, a clock pulse to the prescaler will be generated on the reassignment.

If the prescaler is configured for the 1:1 option, the clock pulse will incorrectly cause a WDT Time-out Reset of the device.

Work around

1. Disable the Timer0 external clock input by clearing the TOCKI bit in the OPTION register.
2. Modify the TOSE bit in the OPTION register to the opposite configuration for the logic level on the T0CKI pin.
3. Select a prescaler rate other than 1:1 and issue a `CLRWDT` instruction before switching to the final prescaler rate.

Affected Silicon Revisions

PIC16F913/914

A0	A1	A2	A3				
X	X	X	X				

PIC16F916/917

A0	A1	A2	B0	B1	B2	B3	
X	X	X	X	X	X	X	

PIC16F946

A0	A1	A2					
X	X	X					

Data Sheet Clarifications

The following typographical corrections and clarifications are to be noted for the latest version of the device data sheet (DS41250**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: LCD Driver Module Block Diagram (Note 1)

In Figure 10-1; “LCD Driver Module Block Diagram,” page 144, change Note 1:

From: These are not directly connected to the I/O pads, but may be tri-stated, depending on the configuration of the LCD module.

To: These signals are connected directly to the I/O pads, but may be tri-stated, depending on the configuration of the LCD module.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2005)
Initial release of Errata, adding Items 1-3.

Rev B Document (2/2007)
Added Module 1: LCD.

Rev. C Document (4/2009)

Updated Errata to new format. This Errata supersedes Errata DS80329.

Data Sheet Clarification: Removed Module 1: CCPR2L/CCPR2H Address and Module 3: MCLR.

Added Module 2: LP/Timer1 Oscillator Operation Below 25°C; Added Module 3: Asynchronous Timer1; Module 4: Timer0 and WDT Prescaler Assignment Spurious Reset.

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