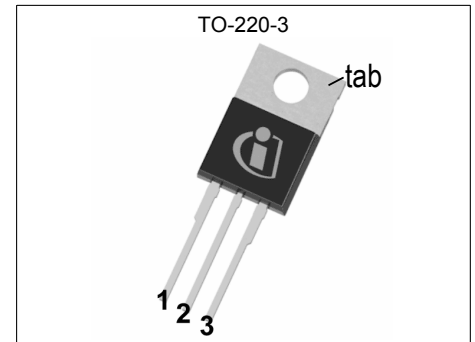


# MOSFET

## OptiMOS™ 5 Power-Transistor, 150 V

### Features

- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- Very low reverse recovery charge ( $Q_{rr}$ )
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target application
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	7.6	mΩ
$I_D$	112	A
$Q_{rr}$	96	nC



Type / Ordering Code	Package	Marking	Related Links
IPP076N15N5	PG-TO220-3	076N15N5	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	112 79	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	448	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	130	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	214	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.4	0.7	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	K/W	-

## 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	$V_{DS}=V_{GS}$ , $I_D=160\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.9 6.4	7.6 8.4	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=56\text{ A}$ $V_{GS}=8\text{ V}$ , $I_D=28\text{ A}$
Gate resistance <sup>3)</sup>	$R_G$	-	1.1	1.7	$\Omega$	-
Transconductance	$g_{fs}$	45	90	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=56\text{ A}$

<sup>1)</sup> See Diagram 3

<sup>2)</sup> See Diagram 13

<sup>3)</sup> Defined by design. Not subject to production test.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	3600	4700	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	900	1200	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	21	37	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=56\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Rise time	$t_r$	-	4	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=56\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	20	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=56\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Fall time	$t_f$	-	4	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=56\text{ A}$ , $R_{G,ext}=1.6\ \Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	21	-	nC	$V_{DD}=75\text{ V}$ , $I_D=56\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	10	15	nC	$V_{DD}=75\text{ V}$ , $I_D=56\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	17	-	nC	$V_{DD}=75\text{ V}$ , $I_D=56\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	49	61	nC	$V_{DD}=75\text{ V}$ , $I_D=56\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=75\text{ V}$ , $I_D=56\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	136	181	nC	$V_{DD}=75\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	112	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	448	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.89	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=56\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	69	138	ns	$V_R=75\text{ V}$ , $I_F=56\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	96	192	nC	$V_R=75\text{ V}$ , $I_F=56\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

### 4 Electrical characteristics diagrams

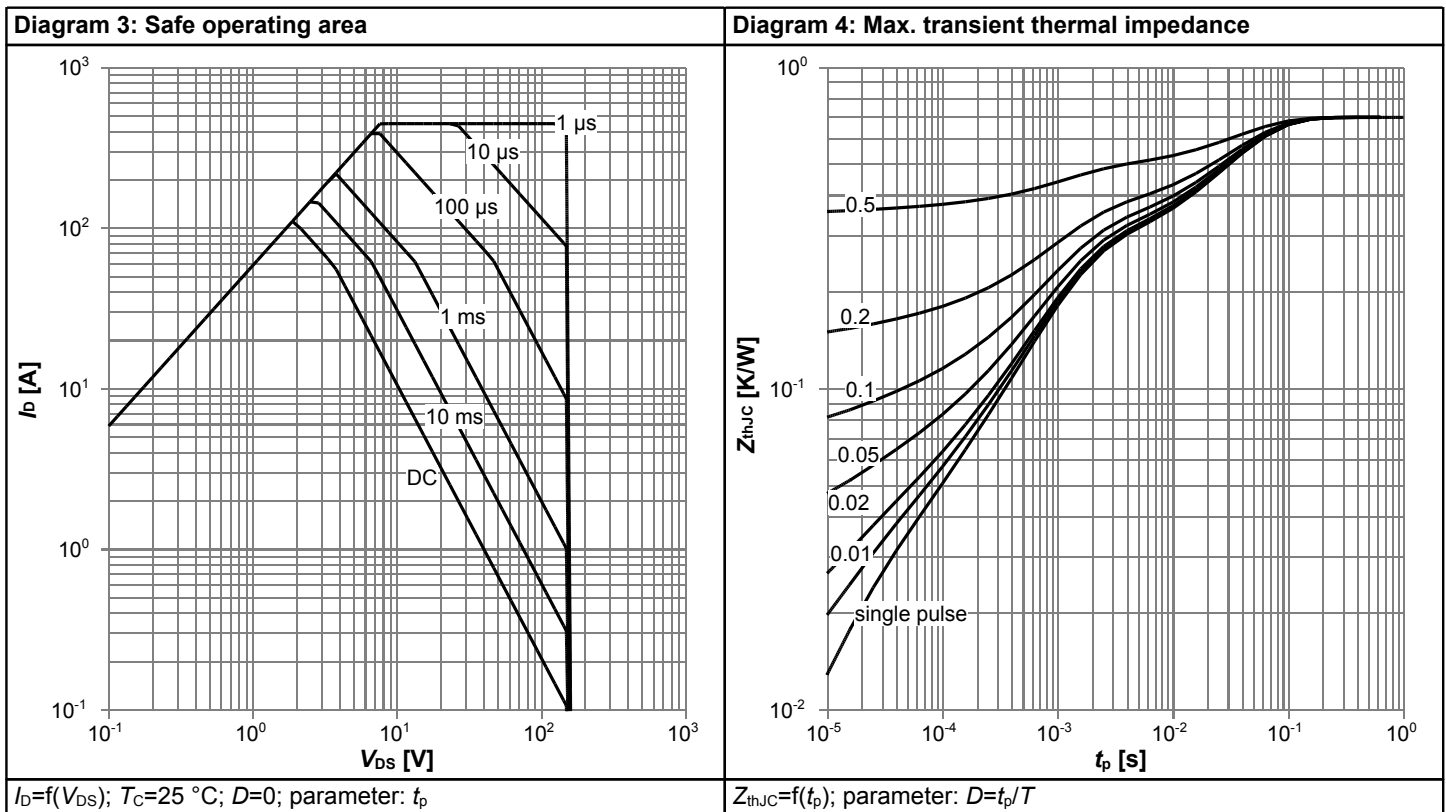
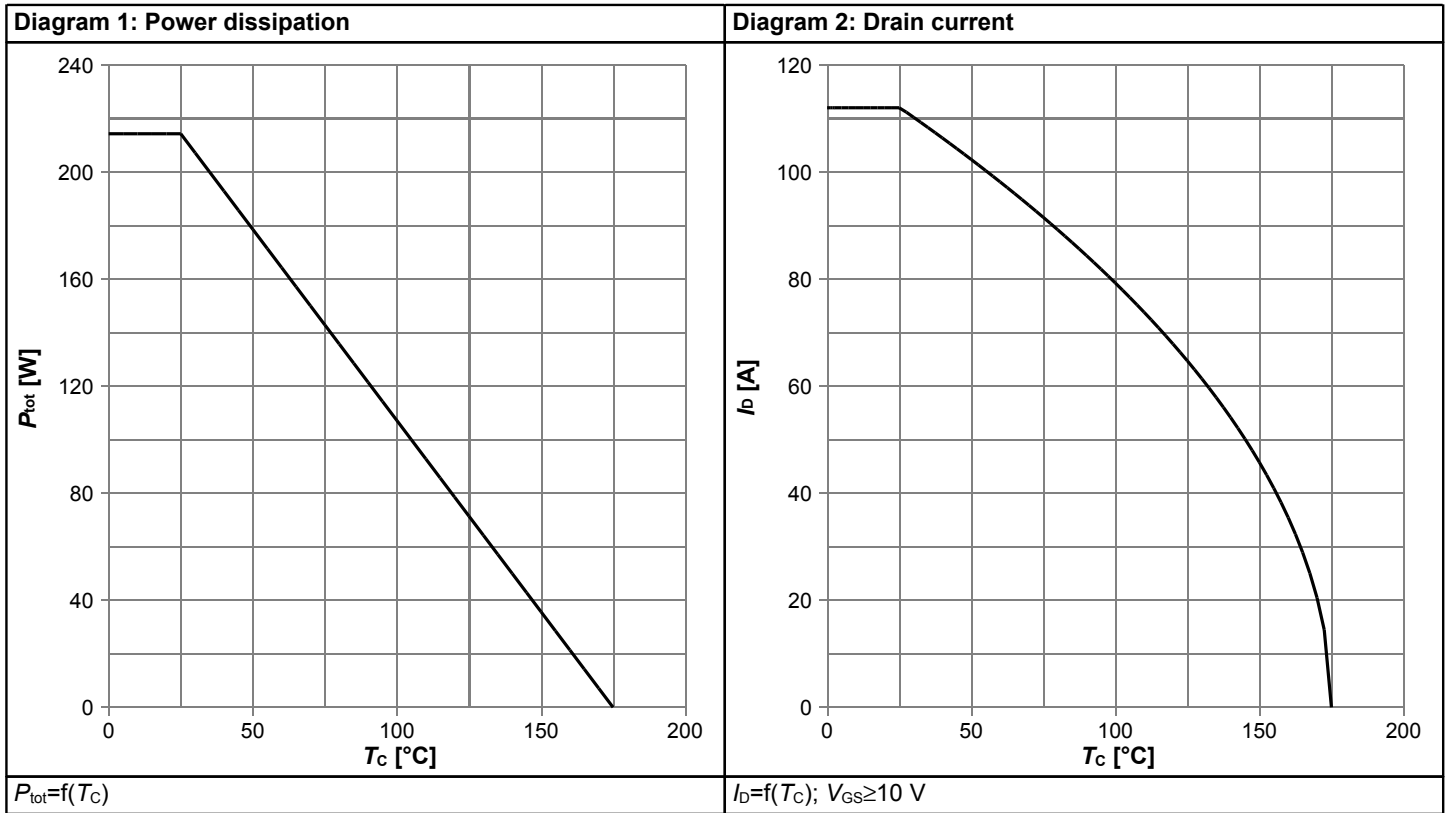
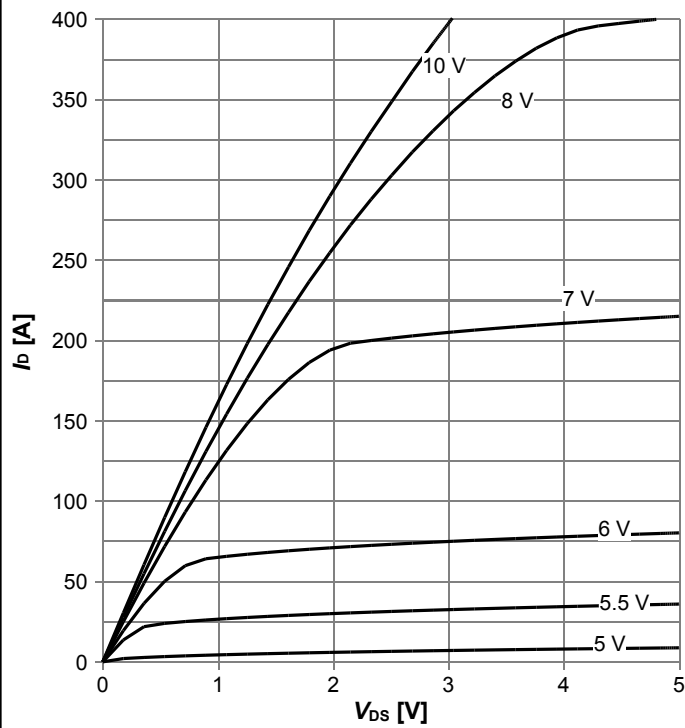
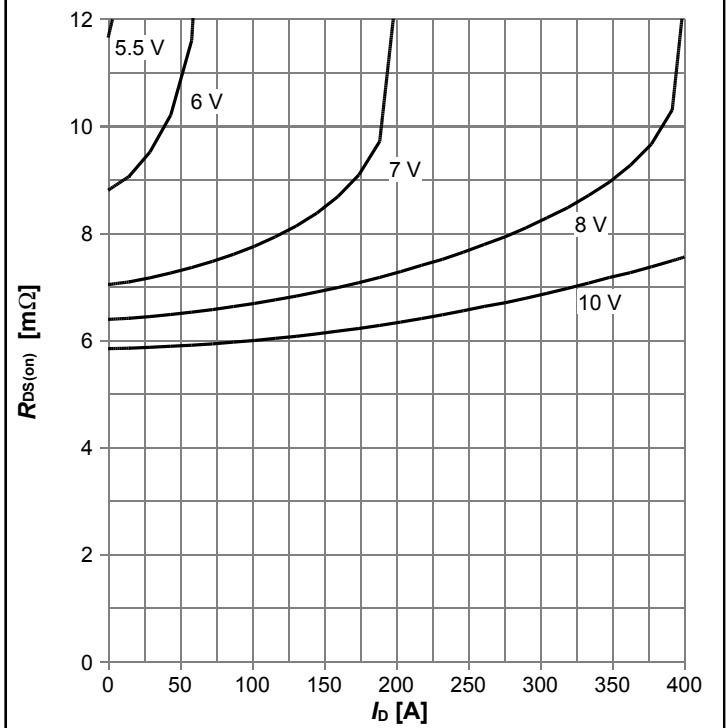


Diagram 5: Typ. output characteristics



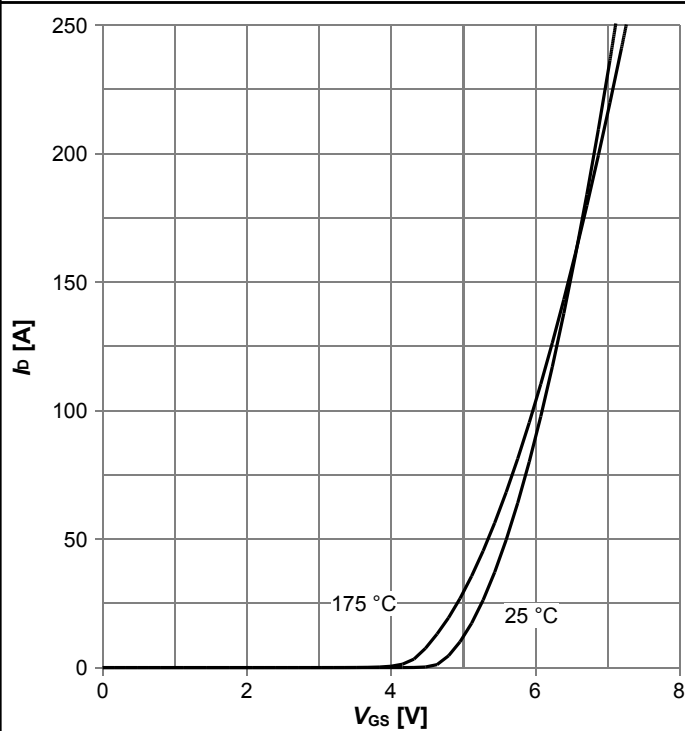
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



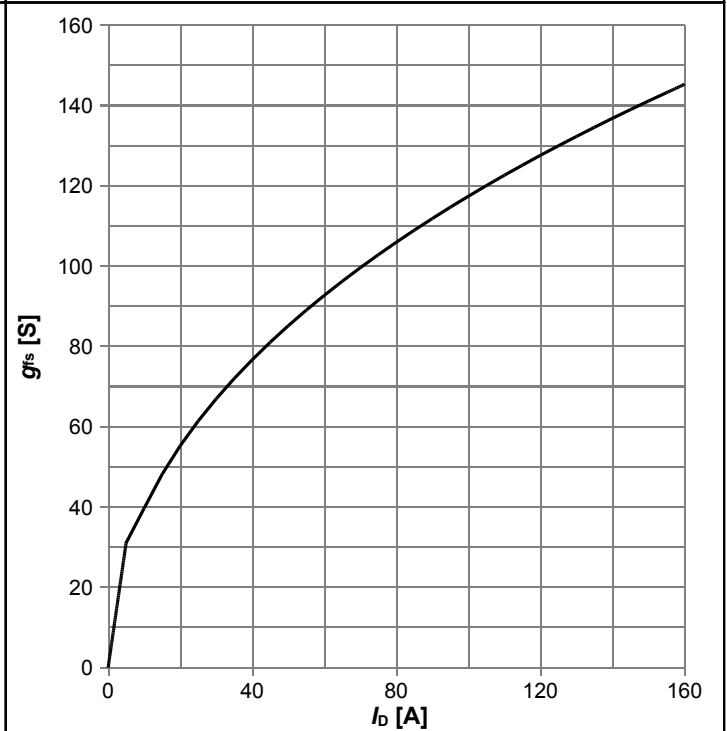
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



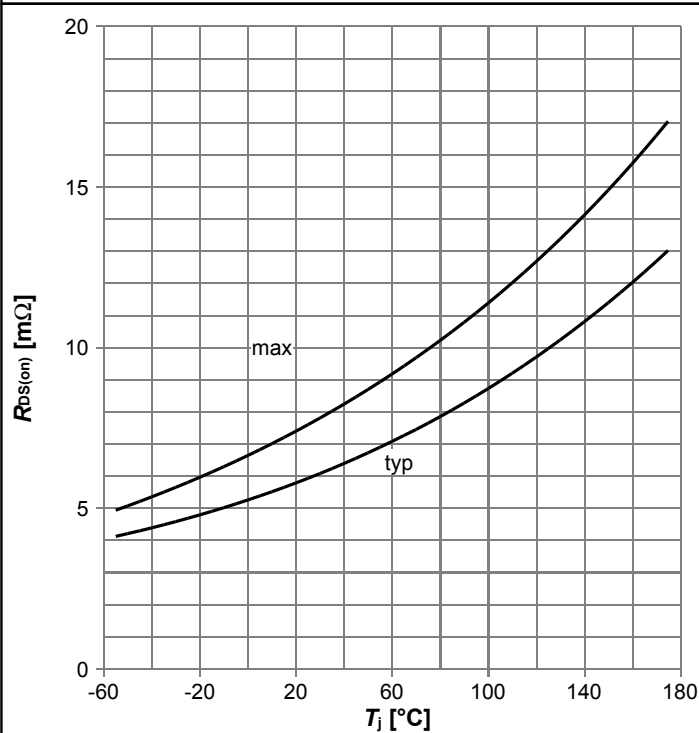
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



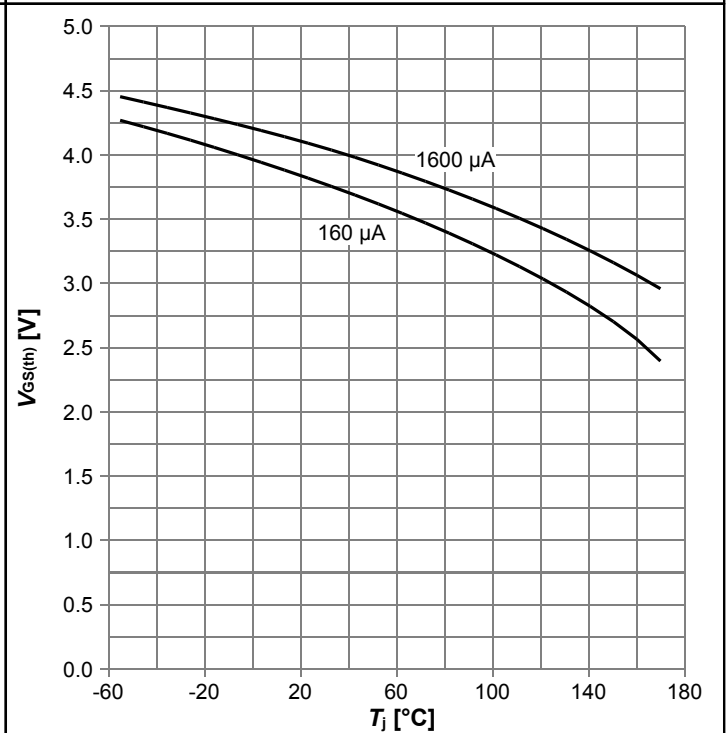
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



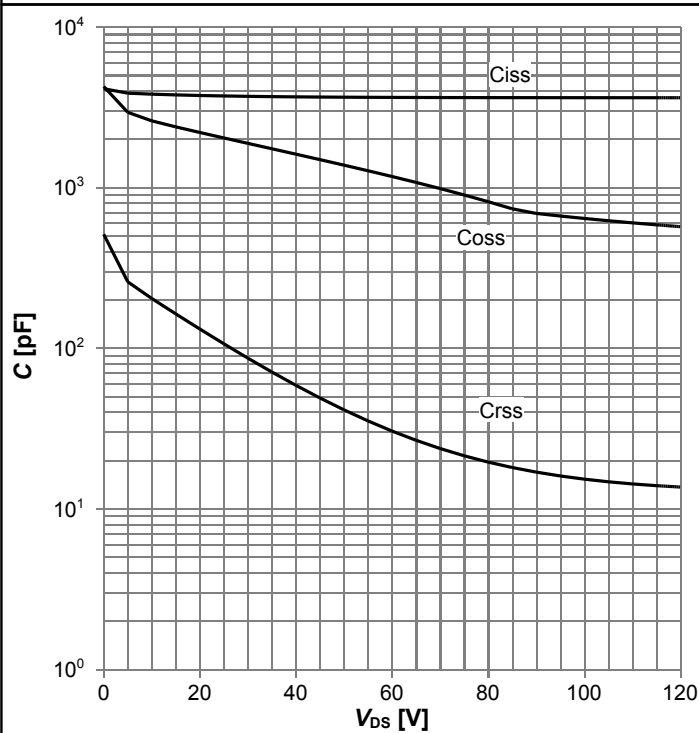
$R_{DS(on)}=f(T_j)$ ;  $I_D=56$  A;  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



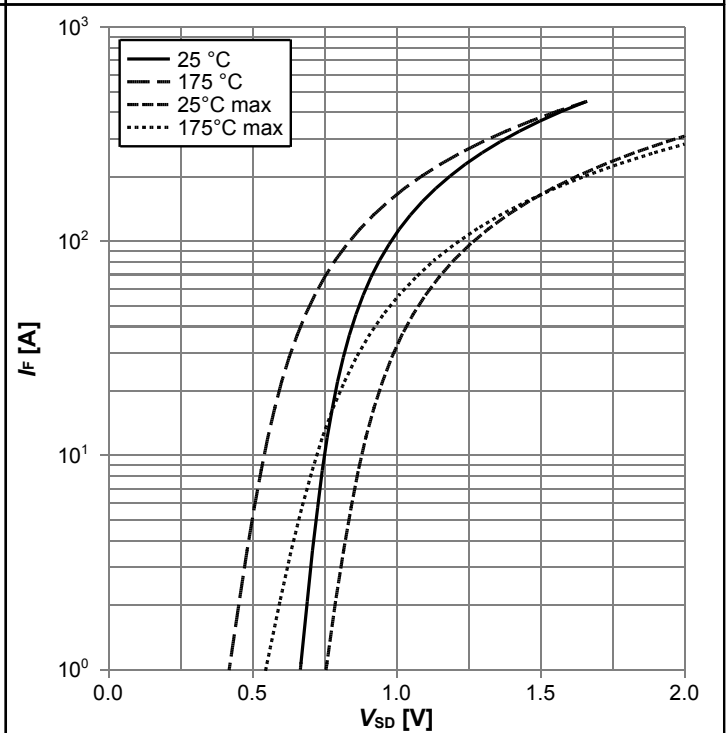
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



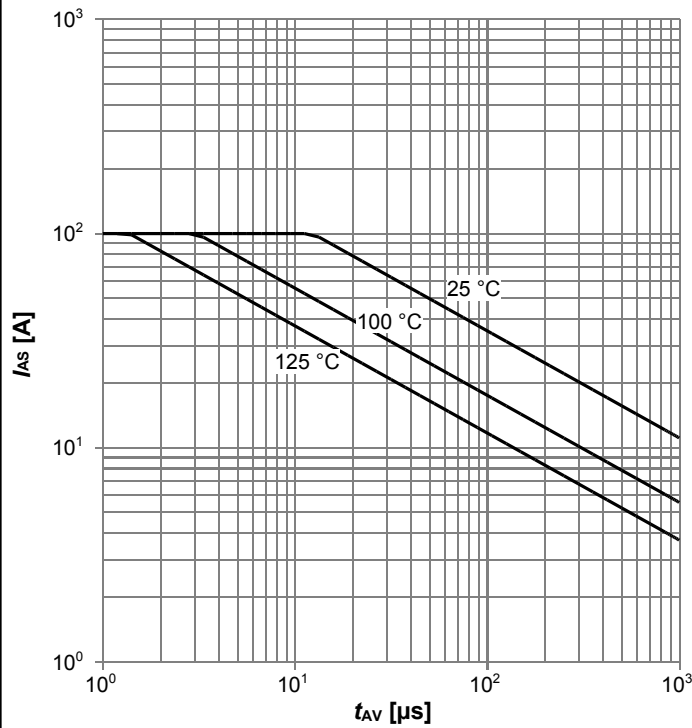
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

Diagram 12: Forward characteristics of reverse diode



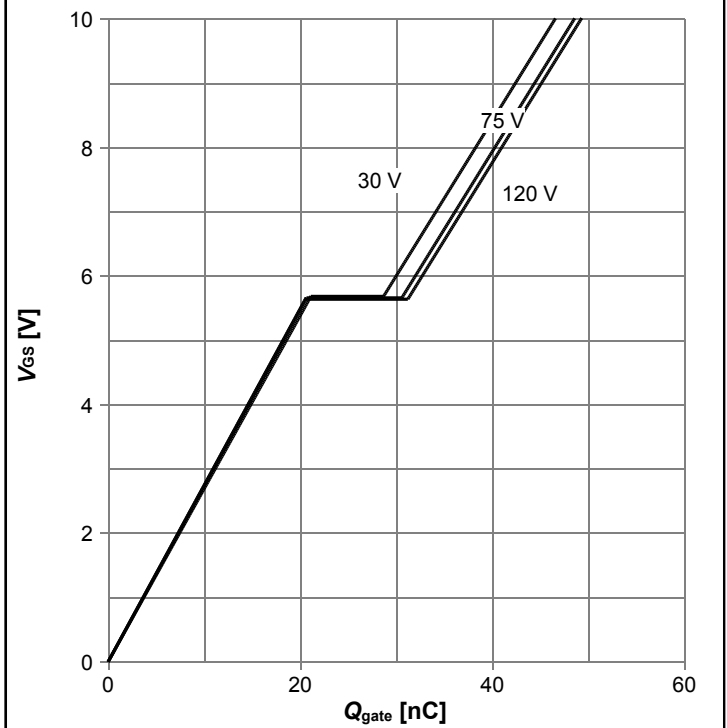
$I_F=f(V_{SD})$ ; parameter:  $T_j$

**Diagram 13: Avalanche characteristics**



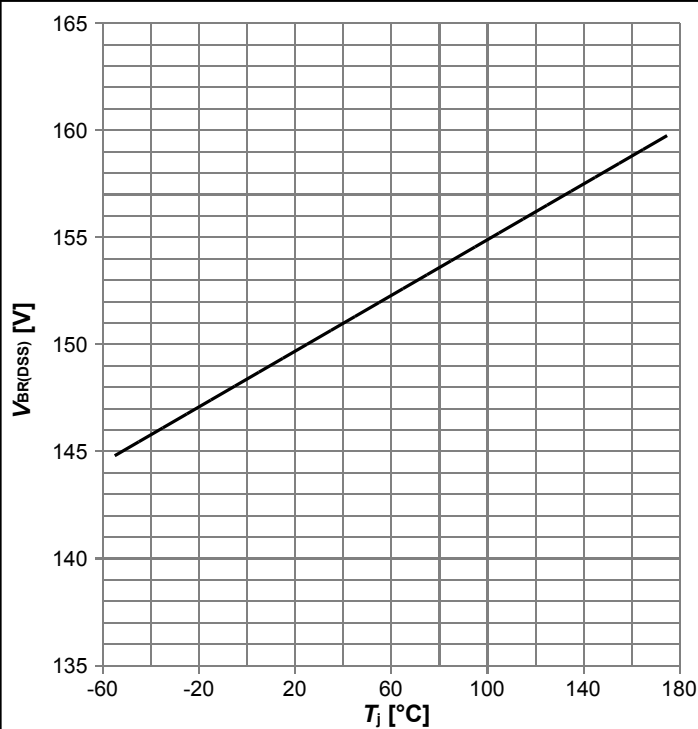
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



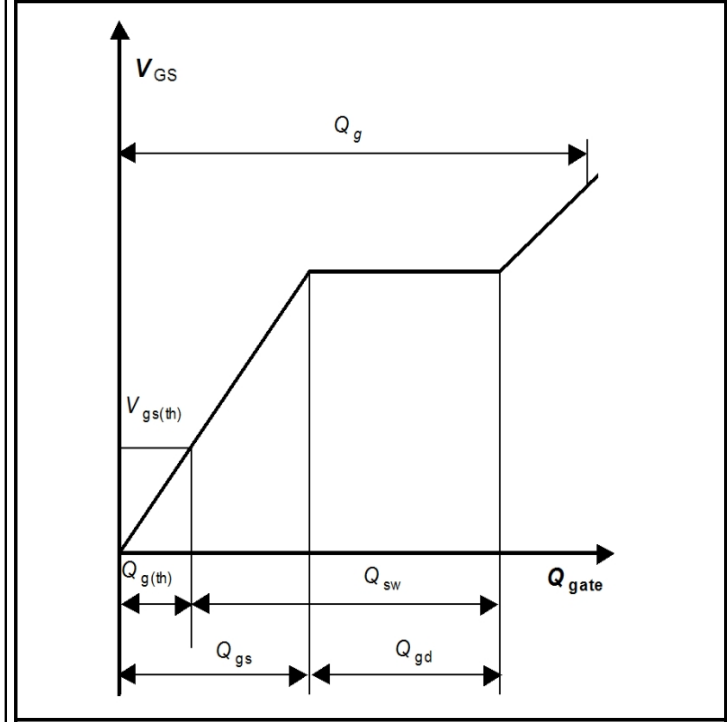
$V_{GS}=f(Q_{gate}); I_D=56 \text{ A pulsed}$ ; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**



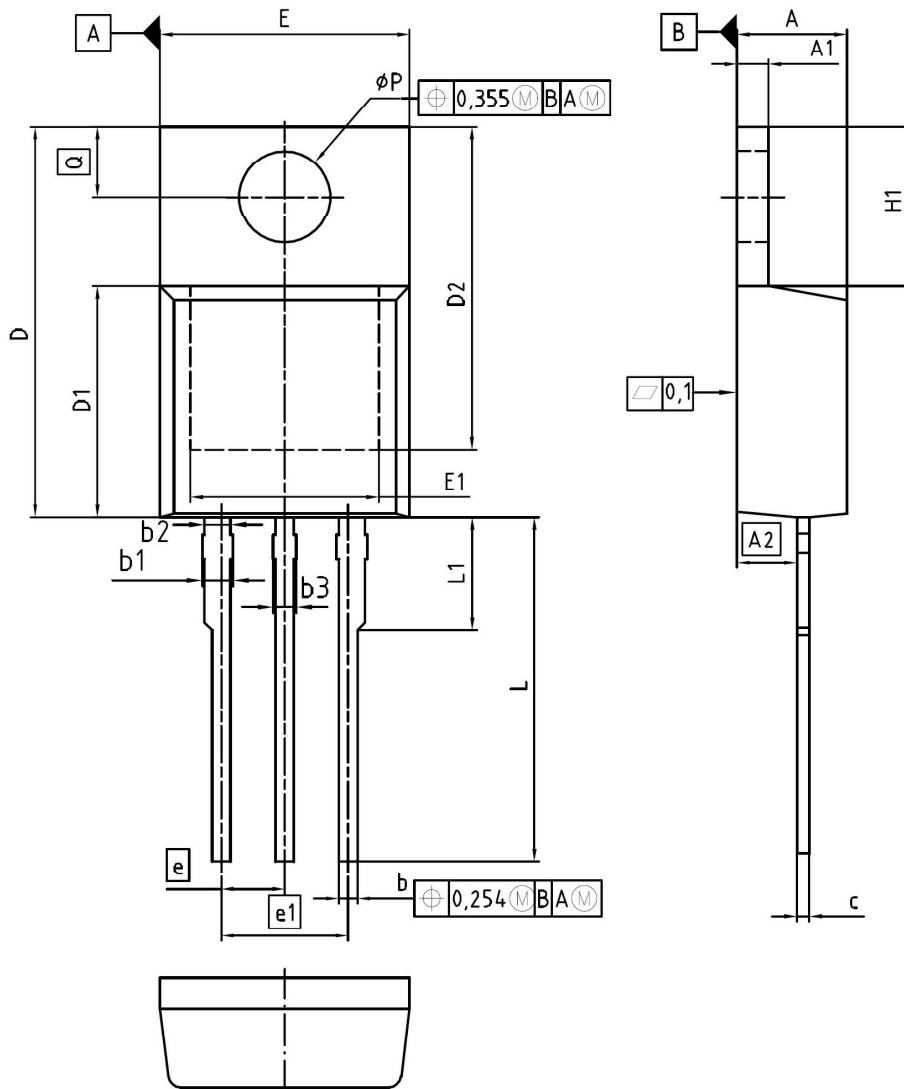
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**





### 5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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06

Figure 1 Outline PG-TO220-3, dimensions in mm/inches

## Revision History

IPP076N15N5

**Revision: 2016-03-03, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-03-03	Release of final version

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