

STRUCTURE Silicon Monolithic integrated circuit

PRODUCTS Input switching interface LSI for the DVD recorder

TYPE **BH7623KS2**

PACKAGE Figure-1 SQFP-T52 (Plastic Mold)

PINOUT Figure-2

BLOCK DIAGRAM Figure-3

Absolute maximum rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Power supply voltage	V	7.0	V
Power dissipation	Pd	※1 1300	mW
Operating temperature range	Topr	-25 ~ +75	°C
Storage temperature range	Tstg	-55 ~ +125	°C

※ 1 When absolute temperature exceeds Ta=25°C, the rated value is reduced at the unit of 14mW/°C.

#### Operation range

Item	Symbol	Limit	Unit
Supply voltage	Vcc1, Vcc2, Vcc3, Vcc, DVCC, SYNC_Vcc	4.5 ~ 5.5	V

- ※ This product is not designed for protection against radioactive rays.
- ※ Vcc1, Vcc2, Vcc3, Vcc, DVCC, SYNC\_Vcc should use the same power source.
- ※ Improper operation will result if the input and/ or output terminal is connected either to the supply.
- ※ I<sup>2</sup>C BUS is compatible with Version2.0. ( It is compatible with FAST MODE, without HS MODE.)

#### Application example

The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

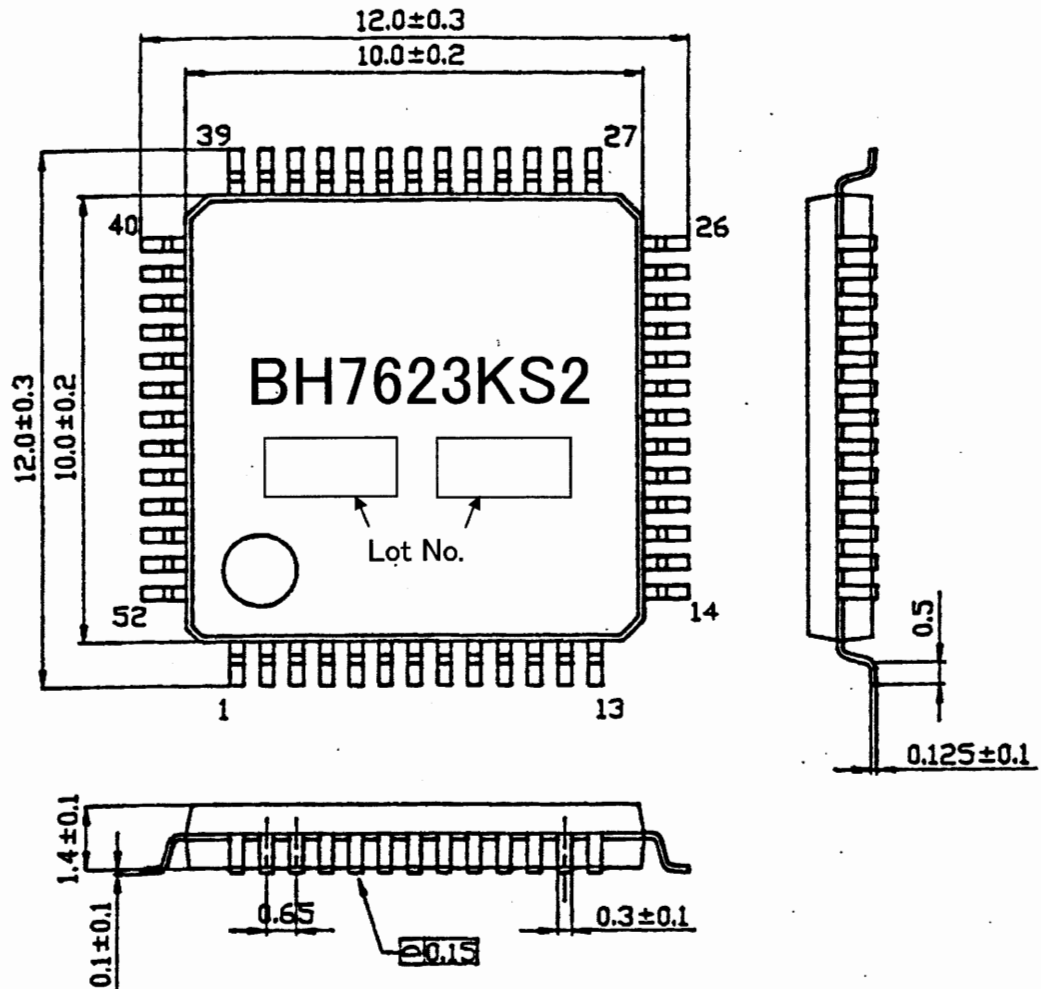
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

DESIGN	CHECK	APPROVAL	DATE :	SPECIFICATION No. :
<i>Ad. Adachi</i> mar. 01/05	<i>T. Kato</i>	<i>Caoru Sawa</i>	Mar/01/2005	TSZ02201-BH7623KS2-1-2
			REV. C	<b>ROHM CO., LTD.</b>

## Feature

- Built-in-5 input Video switch, Y switch and 5-input C switch
- The input terminal of the S2 standard suitability.
- I2C BUS control (High impedance when power source off)
- 0/6dB switch AMP built-in (CVBS OUT, Y/CVBS OUT, C OUT)
- Synchronization isolation circuit built-in. (2 circuits SYNC OUT, V SYNC OUT)
- Synchronization detection circuit built-in. (2 circuits)
- 3 LPF circuits built-in. (4 order + TRAP)



(UNIT : mm)

5 / 1

Fig.1 Contour figure  
(SQFP-T52)

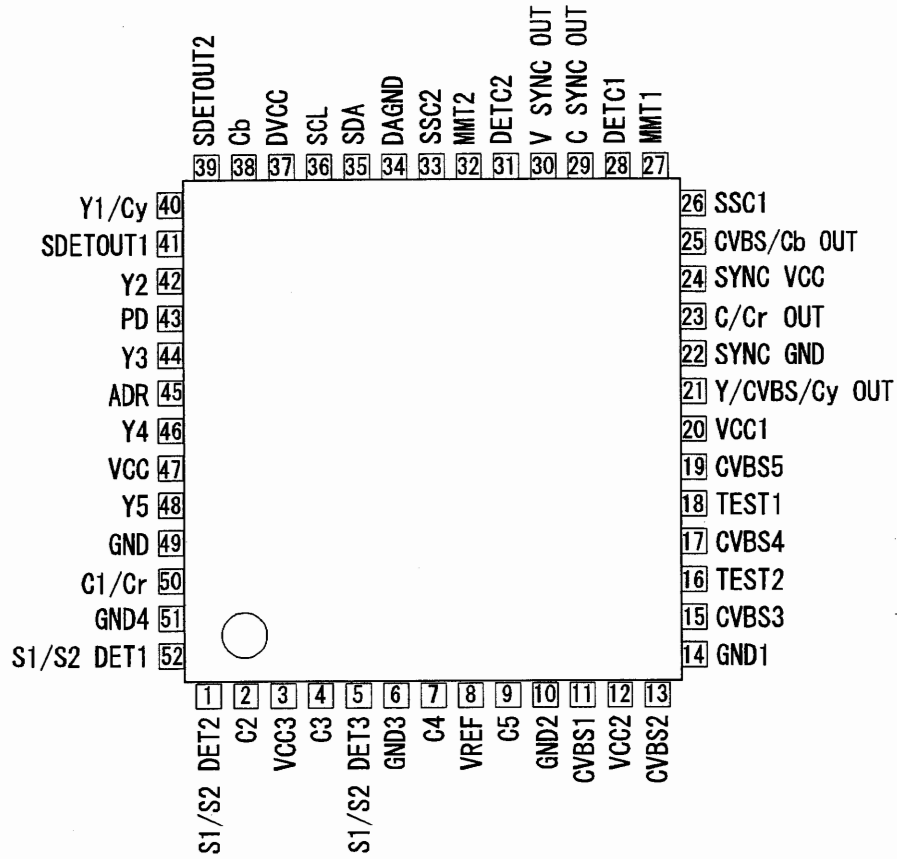


Fig.2 PINOUT

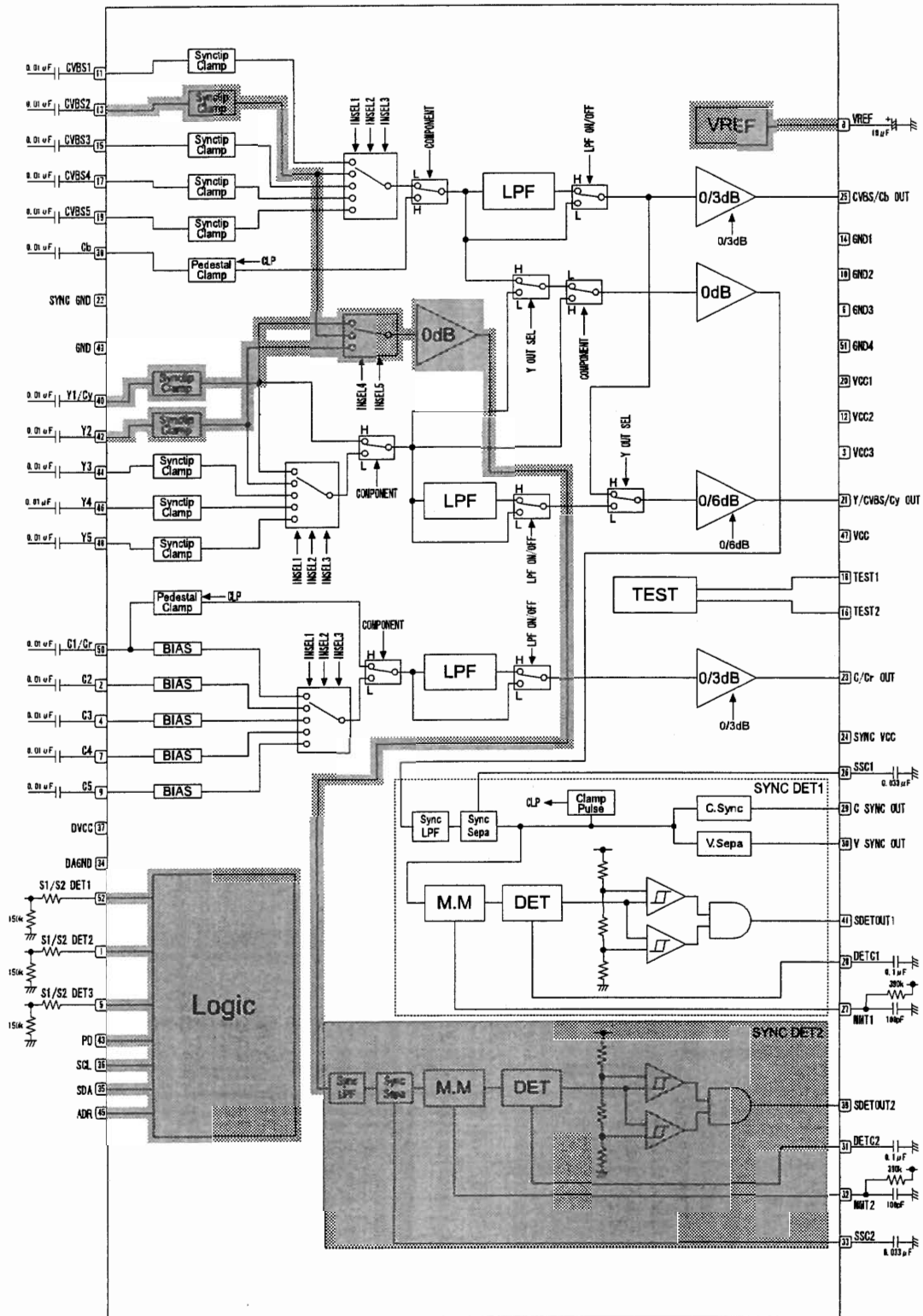


Fig.3. BLOCK Diagram

## Electrical Characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions	
		MIN.	TYP.	MAX.			
<All Circuits>							
VCC Circuit Current	I <sub>CC</sub>	71	95	128	mA	Normal condition	
VCC STBY Circuit Current	I <sub>CCST</sub>	9.38	12.5	16.9	mA	Standby condition	
VCC PD Circuit Current	I <sub>CCPD</sub>	-	0	10	μA	Power down condition	
<SW Part>							
CVBS OUT Cb OUT	Voltage Gain H	G <sub>V1H</sub>	2.4	2.9	3.4	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
CVBS OUT Cb OUT	Voltage Gain L	G <sub>V1L</sub>	-0.7	-0.2	0.3	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT	Voltage Gain H	G <sub>V2H</sub>	5.5	6.0	6.5	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
Y/CVBS OUT Cy OUT	Voltage Gain L	G <sub>V2L</sub>	-0.7	-0.2	0.3	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
C OUT Cr OUT	Voltage Gain H	G <sub>V3H</sub>	2.4	2.9	3.4	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
C OUT Cr OUT	Voltage Gain L	G <sub>V3L</sub>	-0.7	-0.2	0.3	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF OFF
CVBS OUT Cb OUT	Voltage Gain H	G <sub>V4H</sub>	2.2	2.7	3.2	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON
CVBS OUT Cb OUT	Voltage Gain L	G <sub>V4L</sub>	-0.9	-0.4	0.1	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON
Y/CVBS OUT Cy OUT	Voltage Gain H	G <sub>V5H</sub>	5.3	5.8	6.3	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON
Y/CVBS OUT Cy OUT	Voltage Gain L	G <sub>V5L</sub>	-0.9	-0.4	0.1	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON
C OUT Cr OUT	Voltage Gain H	G <sub>V6H</sub>	2.2	2.7	3.2	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON
C OUT Cr OUT	Voltage Gain L	G <sub>V6L</sub>	-0.9	-0.4	0.1	dB	V <sub>in</sub> =1.0Vpp, f=100kHz, LPF ON

## Electrical Characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions	
		MIN.	TYP.	MAX.			
CVBS OUT Cb OUT	Maximum Output Level	V <sub>OM1</sub>	2.6	3.0	-	V <sub>pp</sub>	f=100kHz(10kHz), THD=1%
Y/CVBS OUT Cy OUT	Maximum Output Level	V <sub>OM2</sub>	2.6	3.0	-	V <sub>pp</sub>	f=100kHz(10kHz), THD=1%
C OUT Cr OUT	Maximum Output Level	V <sub>OM3</sub>	2.6	3.0	-	V <sub>pp</sub>	f=100kHz(10kHz), THD=1%
<SW part>							
CVBS OUT Cb OUT	Frequency Characteristic 1	G <sub>F11</sub>	-1.5	-0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/6.75MHz (LPF ON)
CVBS OUT Cb OUT	Frequency Characteristic 2	G <sub>F12</sub>	-	-38	-27	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/27MHz (LPF ON)
CVBS OUT Cb OUT	Frequency Characteristic 3	G <sub>F13</sub>	-1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/7MHz (through)
Y/CVBS OUT Cy OUT	Frequency Characteristic 1	G <sub>F21</sub>	-1.5	-0.5	0.5	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=100kHz/6.75MHz (LPF ON)
Y/CVBS OUT Cy OUT	Frequency Characteristic 2	G <sub>F22</sub>	-	-38	-27	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=100kHz/27MHz (LPF ON)
Y/CVBS OUT Cy OUT	Frequency Characteristic 3	G <sub>F23</sub>	-1.0	0	1.0	dB	Vin=1.0Vpp Gain=6dB Vin=2.0Vpp Gain=0dB f=100kHz/7MHz (through)
C OUT Cr OUT	Frequency Characteristic 1	G <sub>F31</sub>	-1.5	-0.5	0.5	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/6.75MHz (LPF ON)
C OUT Cr OUT	Frequency Characteristic 2	G <sub>F32</sub>	-	-38	-27	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/27MHz (LPF ON)
C OUT Cr OUT	Frequency Characteristic 3	G <sub>F33</sub>	-1.0	0	1.0	dB	Vin=1.0Vpp Gain=3dB Vin=2.0Vpp Gain=0dB f=100kHz/7MHz (through)

## Electrical Characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
V-SW Difference In Switch Voltage Gain	$\Delta G_V$	-0.5	0.0	0.5	dB	f=100kHz Vin=1.0Vpp Gain=0/6dB
Y-SW Difference In Switch Voltage Gain	$\Delta G_Y$	-0.5	0.0	0.5	dB	f=100kHz Vin=1.0Vpp Gain=0/6dB
C-SW Difference In Switch Voltage Gain	$\Delta G_C$	-0.5	0.0	0.5	dB	f=100kHz Vin=1.0Vpp Gain=0/6dB
V-SW Switch Crosstalk	$C_{TSV}$	-	-60	-55	dB	f=4.43MHz Gain=0/6dB Vin=1.0Vpp
Y-SW Switch Crosstalk	$C_{TSY}$	-	-60	-55	dB	f=4.43MHz Gain=0/6dB Vin=1.0Vpp
C-SW Switch Crosstalk	$C_{TSC}$	-	-60	-55	dB	f=4.43MHz Gain=0/6dB Vin=1.0Vpp
V↔Y↔C Channel Crosstalk	$C_{TCH}$	-	-60	-55	dB	f=4.43MHz Gain=0/6dB Vin=1.0Vpp
C IN Input Impedance	$Z_{CIN}$	12.5	18.0	23.5	kΩ	



Electrical Characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
< SYNC DETECTOR Part >						
Min Synchronization Isolation Level	SL <sub>MIN</sub>	-	0.08	0.15	Vpp	LPF condition "000"
V SYNC OUT Output Voltage H	V <sub>VSH</sub>	Vcc -0.5	Vcc -0.1	Vcc	V	No Load
V SYNC OUT Output Voltage L	V <sub>VSL</sub>	-	0.1	0.5	V	No Load
VD Pulse Width	T <sub>WV1</sub>	-	185	-	μ sec	Vin=1.0Vpp standard signal LPF condition "000"
HD Pulse Width	T <sub>WH1</sub>	-	4.1	-	μ sec	Vin=1.0Vpp standard signal LPF condition "000"
C SYNC OUT Output Voltage H	V <sub>VCH</sub>	Vcc -0.5	Vcc -0.1	Vcc	V	No Load
C SYNC OUT Output Voltage L	V <sub>VCL</sub>	-	0.1	0.5	V	No Load
SYNC DET OUT Output Voltage H	V <sub>SDH</sub>	Vcc -0.5	Vcc -0.1	Vcc	V	No Load
SYNC DET OUT Output Voltage L	V <sub>SDL</sub>	-	0.1	0.5	V	No Load

## Electrical characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<I2C-BUS Control>						
S1/S2 DET Detection Level H	DL <sub>H</sub>	3.4	-	V <sub>cc</sub>	V	16:9 Squeeze Signal
S1/S2 DET Detection Level M	DL <sub>M</sub>	1.3	1.9	2.5	V	4:3 Letter Box Signal
S1/S2 DET Detection Level L	DL <sub>L</sub>	0.0	-	0.7	V	4:3 Video Signal, No Signal
<ADR>						
Input Voltage H	V <sub>1HADR</sub>	2.0	-	V <sub>cc</sub>	V	
Input Voltage L	V <sub>1LADR</sub>	0.0	-	1.0	V	
Input Impedance	Z <sub>1NADR</sub>	65	100	135	kΩ	Pull Down Resistance
<SCL, SDA>						
Input Voltage H	V <sub>IH11C</sub>	2.0	-	V <sub>cc</sub>	V	
Input Voltage L	V <sub>IL11C</sub>	0.0	-	1.0	V	
Input Bias Current	V <sub>B11C</sub>	0	-1	-10	μA	
<PD>						
Input Voltage H	V <sub>IHPD</sub>	2.0	-	V <sub>cc</sub>	V	
Input Voltage L	V <sub>ILPD</sub>	0.0	-	0.7	V	
Input Impedance	Z <sub>INPD</sub>	65	100	135	kΩ	Pull Down Resistance

Electrical Characteristics (Ta=25°C, Vcc=5.0V unless otherwise specified)

Item	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
<Design Guarantee Item>						
Differential Gain	D <sub>G</sub>	-	0.5	-	%	CVBS OUT, Y/CVBS OUT, C OUT Vin=2.0Vpp Gain=0dB Vin=1.0Vpp Gain=6dB
Differential Phase	D <sub>P</sub>	-	0.5	-	deg	CVBS OUT, Y/CVBS OUT, C OUT Vin=2.0Vpp Gain=0dB Vin=1.0Vpp Gain=6dB
Y S/N	S <sub>NY</sub>	-	-70	-	dB	CVBS OUT, Y/CVBS OUT 50% white signals 100kHz~6MHz
C S/N	S <sub>NC</sub>	-	-70	-	dB	C OUT 100% Chroma S/N measurement typical signal 100Hz~500kHz

■ I<sup>2</sup>C-BUS Control input Specifications  
 ○ I2C-BUS Format (WRITE MOOE)



S : Start Condition  
 A : Acknowledge  
 P : Stop Condition

	b7	b6	b5	b4	b3	b2	b1	B0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	5	4	3	2	1	L2	L1	L0
	INSEL							
DATA2	Y-OUT SEL	Component	LPF ON/OFF	GAIN 0/6dB	STBY	T2	T1	T0

# Don't Care

- \* At the power on, LOW condition starts.
- \* Please be cautious in maintaining the value of ADR and S1S2DET terminal inputs between stop and start condition and avoid a change in value because it may result to an miss operation.

○ SELECT INPUT SWITCH-SETTING MODE

ADR: Slave Address (write mode) set by ADR pin  
 0 : Address is "90H", when ADR pin input is set to L.  
 1 : Address is "92H", when ADR pin input is set to H.

R/W: READ/WRITE Setting Mode  
 0 : WRITE  
 1 : READ

INSEL3~1: Change setting of input selector SW.  
 Refer to the next page SW correspondence table.

INSEL5,4: SYNC DET2 input setting  
 00 : Y1/Cy  
 01 : Y1/Cy  
 10 : CVBS2  
 11 : Y2

Y-OUT SEL: Y-OUT SEL SW output setting  
 0 : L  
 1 : H

Component: Component SEL SW output setting  
 0 : L (Composit)  
 1 : H (Component)

LPF ON/OFF: LPF ON/OFF setting  
 0 : L (OFF)  
 1 : H (ON)

GAIN 0/6dB: AMP GAIN setting  
 0 : L (0dB)  
 1 : H (6dB)/(3dB)

Stand-By: Stand-By Mode setting  
 0 : L (move)  
 1 : H (standby)

※When standby condition, this IC is move only the circuits in the block diagram.

○ INPUT SW CONTROL Correspondence table

INSEL 3	INSEL 2	INSEL 1	Y-OUT SEL	Component	CVBS OUT	Y OUT	C OUT	CSYNC etc.
0	0	0	1	0	CVBS1	CVBS1	C1	CVBS1
0	0	1	1	0	CVBS2	CVBS2	C2	CVBS2
0	1	0	1	0	CVBS3	CVBS3	C3	CVBS3
0	1	1	1	0	CVBS4	CVBS4	C4	CVBS4
1	0	0	1	0	CVBS5	CVBS5	C5	CVBS5
0	0	0	0	0	CVBS1	Y1	C1	Y1
0	0	1	0	0	CVBS2	Y2	C2	Y2
0	1	0	0	0	CVBS3	Y3	C3	Y3
0	1	1	0	0	CVBS4	Y4	C4	Y4
1	0	0	0	0	CVBS5	Y5	C5	Y5
-	-	-	0	1	Cb	Y1(Cy)	C1(Cr)	Y1(Cy)
-	-	-	1	1	Cb	Cb	C1(Cr)	Y1(Cy)

L2-L0: SYNC SEPA LPF Cut-off conditioning.

000 : Low (Norm)

001 : ↓

010 : ↓

011 : ↓

100 : ↓

101 : ↓

110 : ↓

111 : High

T2-T0: DET Output decision comparator threshold conditioning.

000 : Low (Norm)

001 : ↓

010 : ↓

011 : ↓

100 : ↓

101 : ↓

110 : ↓

111 : High

## ○ I2C-BUS Format (READ MOOE)

S	SLAVE ADDRESS	A	DATA1	A/N	P
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S : Start Condition

A : Acknowledge

A/N : NO acknowledge

P : Stop Condition

	B7	b6	b5	b4	b3	b2	b1	b0
Slave address	1	0	0	1	0	0	ADR	R/W
DATA1	SD1		SD2		SD3		V-DET2	V-DET1

# Don't Care

\* Please be cautious in maintaining the value of ADR and S1S2DET terminal inputs between stop and start condition and avoid a change in value because it may result to an miss operation.

ADR: Slave address (read mode) Set by ADR pin.  
 0 : Address is "91H", when ADR pin input is set to L.  
 1 : Address is "93H", when ADR pin input is set to H.

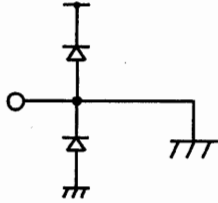
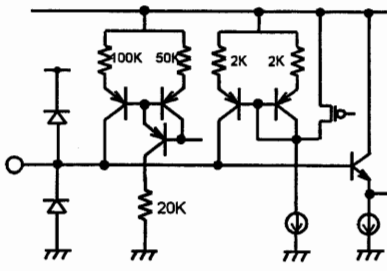
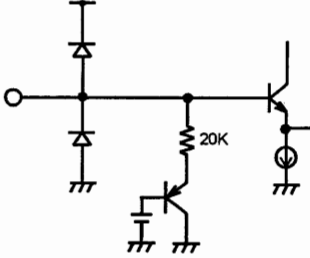
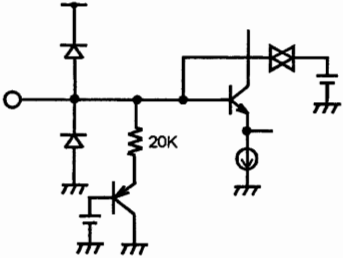
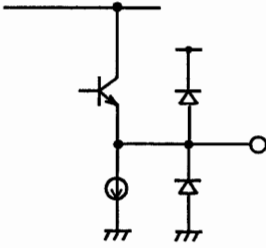
SD1, SD2, SD3 : The state of S1/S2 DET1~S1/S2 DET3 is read out.  
 00 : 4:3 Video signal (0~0.7V)  
 01 : 4:3 Letter Box signal (1.3~2.5V)  
 10 : 16:9 Squeeze signal (3.4V~Vcc)

V-DET1, V-DET2 : The signal of SDET OUT is read out.  
 0 : H (VIDEO signal ON)  
 1 : L (VIDEO signal OFF)

**■ About the power down state.**

It becomes power down state when PD terminal is LOW. As for this state, internal circuitry becomes non-active state.

LOW : Power down state.  
 HI : Active state.

Pin Name (Input/Output)	Pin Explanation	INPUT/OUTPUT Equivalent Circuit	Input Range(V)
			Terminal Voltage (V)
14. GND 1 10. GND 2 6. GND 3 51. GND 4	GND		0
11. CVBS 1 13. CVBS 2 15. CVBS 3 17. CVBS 4 19. CVBS 5 40. Y1_Cy 42. Y2 44. Y3 46. Y4 48. Y5	Signal Input Pin The video signal input pins, it is a sink chip clamp.		1.4
2. C2 4. C3 7. C4 9. C5	Signal Input Pin The video signal input pins, it is a resistance bias.		2.9
50. C1_Cr	Signal Input Pin These pins are inputs of chroma signal1 (C1) and Cr, change resistor bias and pedestal clamp.		2.9
25. CVBS/Cb OUT 21. Y/CVBS/Cy OUT 23. C/Cr OUT	Signal Output Pin It can select gain, I <sup>2</sup> C BUS.		0.7 2.1

※The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.



Pin Name (Input/Output)	Pin Explanation	INPUT/OUTPUT Equivalent Circuit	Input Range(V)
			Terminal Voltage(V)
29. C SYNC OUT 30. V SYNC OUT	C, V Synchronized Signal Output  It output synchronized signal.		5.0
28. DETC 1 31. DETC 2	Generate DET Voltage Pin  It smoothes the MM pulse.		-
27. MMT 1 32. MMT 2	MM Trimming Pin  It determines the MM time constant.		-
41. SDET OUT 1 39. SDET OUT 2	Signal Output Pin  These pins output cycle detect pins.		0
8. VREF	Standard Voltage Pin  A capacitor is connected to opposite GND.		2.8

※The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

Pin Name (Input/Output)	Pin Explanation	INPUT/OUTPUT Equivalent Circuit	Input Range(V)
			Terminal Voltage(V)
38. Cb	Signal Input Pin The video signal input pin(Cb), it is a pedestal clamp.		-
52. S1/S2 DET 1 1. S1/S2 DET 2 5. S1/S2 DET 3	Signal Input Pin The state of inputted signal is possible Read-OUT at I <sup>2</sup> C BUS.		-
43. PD	PD Pin It can set power down mode.		0
18. TEST 1 16. TEST 2	TEST Pin It short to GND.		0
26. SSC 1 33. SSS 2	SSC Pin It makes standard voltage for SYNC.		-

※The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

Pin Name (Input/Output)	Pin Explanation	INPUT/OUTPUT Equivalent Circuit	Input Range(V)
			Terminal Voltage(V)
25. ADR	<p>ADA Pin</p> <p>These pins set 90H (91H) to slave address, or 92H(93H).</p>		0
36. SCL	<p>I<sup>2</sup>C BUS Clock Input Pin</p> <p>It input clock of I<sup>2</sup>C BUS. It is possible to use pulling up usual resistor.</p>		—
35. SDA	<p>I<sup>2</sup>C BUS Data Pin</p> <p>These pins input I<sup>2</sup>C BUS data. It use standard resistor to pull up.</p>		—

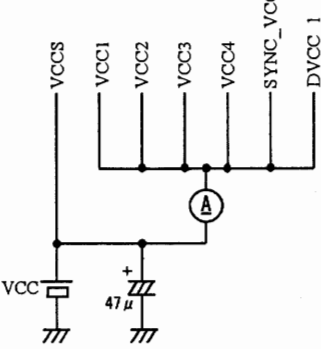
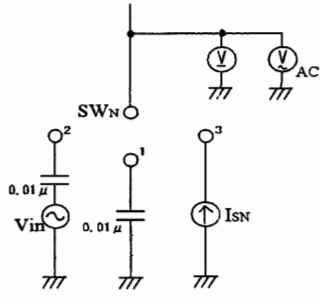

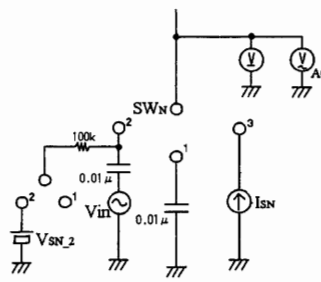
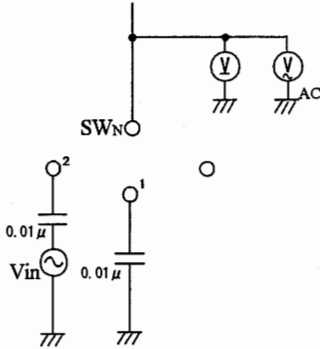
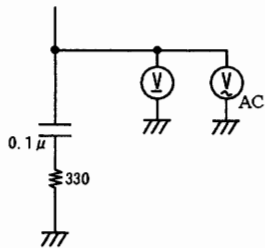
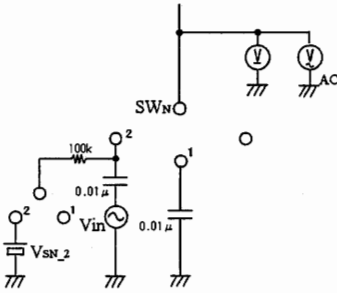
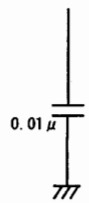
※The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.





Measurement Item	SW NO.																																
	2	4	7	9	11	13	15	17	19	38	38.2	40	42	43	44	45	46	48	50	50.2	11.2	40.2	18	16	52	35	36	26	27	33	32	31	
SSC1 Freq. Characteristic 000												2	2																				
SSC1 Freq. Characteristic 000												2	2																				
SSC1 Voltage Gain 111												2	2																				
SSC1 Freq. Characteristic 111												2	2																				
MMT1 Output Voltage													2																			3	
DETC1 Output Voltage L													2																			2	
DETC1 Output Voltage H													2																			2	
DETC1 Impedance													2																			2	
SDET1 OUT1 Output Voltage L													2																				
SDET1 OUT1 Output Voltage H-1												2	2																				
SDET1 OUT1 Output Voltage H-2												2	2																				
SDET1 OUT1 Output Voltage H-3						2							2																				
C SYNC OUT Output Voltage Check												2	2																				
C SYNC OUT HD Pulse Wide												2	2																				
C SYNC OUT HD Pulse												2	2																				
V SYNC OUT VD Pulse Wide												2	2																				
V SYNC OUT VD Pulse												2	2																				
SSC2 Output Voltage													2																				3
SSC2 Voltage Gain 000												2	2																				
SSC2 Freq. Characteristic 000												2	2																				
SSC2 Voltage Gain 111												2	2																				
SSC2 Freq. Characteristic 111												2	2																				
MMT2 Output Voltage Source													2																				3
DETC2 Output Voltage L													2																				2
DETC2 Output Voltage H													2																				2
DETC2 Impedance													2																				3
SDET2OUT1 Output Voltage L						2							2																				
SDET2OUT1 Output Voltage H-1						2							2																				
SDET2OUT1 Output Voltage H-2										2				2																			
SDET2OUT1 Output Voltage H-3														2																			
SDET2OUT1 Output Voltage H-4													2	2																			

Measurement Circuit (1/2)

PIN NO/Pin Name	Measurement Circuit	PIN NO/Pin Name	Measurement Circuit
20 VCC1 12 VCC2 3 VCC3 47 VCC4 24 SYNC_VCC 37 DVCC_1		2 C2 4 C3 7 C4 9 C5	
14 GND1 10 GND2 6 GND3 51 GND4 22 SYNC_GND 49 GND 34 DAGND		50 C1_Cr	
13 CVBS2 15 CVBS3 17 CVBS4 19 CVBS5 42 Y2 44 Y3 46 Y4 48 Y5		25 CVBS/CbOUT 21 Y_CVBS_CyOU T 23C_CrOUT	
11 CVBS1 38 Cb 40 Y1_Cy		8 VREF	

Measurement Circuit (2/2)

PIN NO./Pin Name	Measurement Circuit	PIN NO./Pin Name	Measurement Circuit
45 ADR 43 PD		27 MMT1 32 MMT2	
52 S1_S2_DET1 1 S1_S2_DET2 5 S1_S2_DET3		28 DETC1 31 DETC2	
36 SDA 35 SCL		18 TEST1 16 TEST2 29 C_SYNC_OUT 30 V_SYNC_OUT 41 SDETOUT1 39 SDETOUT2	
26 SSC1 33 SSC2			

- ※ When the control signal by I2C-BUS is required for each item, please combine with the contents of measurement and input a control signal.
- ※ Please set the blank of measurement condition table as the SW position1 is a measurement circuit specified SW should measure by the appointed position.



## ■Attention on use

## 1. Supply voltage of operation

Although basic circuit function is guaranteed within the limits of supply voltage (4.5V~5.5V) of operation, please be sure element and each parameter, when this device use.

## 2. Operating temperature range

Although basic function is guaranteed within the limits of operating temperature (-25°C~+75°C), please take into consideration enough for a hindsight.

An occasion of a set design, please measure against heat dissipation sufficiently secured circulation of the air of IC circumference according to installation a fan and PCB layout

## 3. Please lay out external parts nearest IC, and lines from output amplifier set short.

## 4. VCC for this IC should use the same power source. And impedance should connect as low as possible for each VCC pin, for each GND pin.