

Automotive P-Channel 40 V (D-S) 175 °C MOSFET

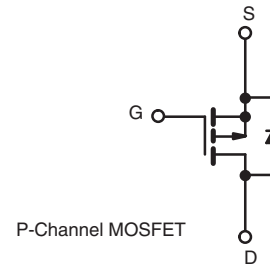
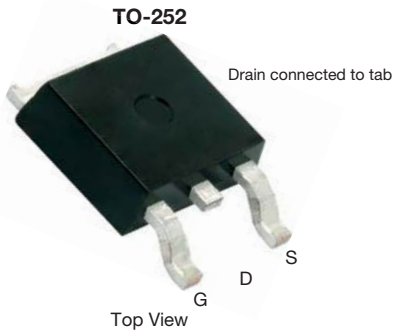


RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	-40
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.013
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.022
I_D (A)	-50
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_g and UIS tested
- AEC-Q101 qualified^d
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50P04-13L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	-40	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	I_D	$T_C = 25$ °C ^a	-50	
		$T_C = 125$ °C	-39	
Continuous Source Current (Diode Conduction) ^a	I_S	-50	A	
Pulsed Drain Current ^b	I_{DM}	-200		
Single Pulse Avalanche Current	I_{AS}	-40		
Single Pulse Avalanche Energy	E_{AS}	L = 0.1 mH	80	mJ
Maximum Power Dissipation ^b			$T_A = 25$ °C	
	$T_C = 25$ °C	136		
	$T_C = 125$ °C	45		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)			

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1.5	-	-2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$, $V_{DS} = -40\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	-150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = -10\text{ V}$, $V_{DS} \leq -5\text{ V}$	-50	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -17\text{ A}$	-	0.010	0.013	Ω
		$V_{GS} = -10\text{ V}$, $I_D = -50\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.017	
		$V_{GS} = -10\text{ V}$, $I_D = -50\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.020	
		$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$	-	0.016	0.022	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -17\text{ A}$	-	61	-	S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$	-	2872	3950	μF
Output Capacitance	C_{oss}		-	508	635	
Reverse Transfer Capacitance	C_{rss}		-	352	440	
Total Gate Charge ^c	Q_g	$V_{GS} = -10\text{ V}$, $V_{DS} = -30\text{ V}$, $I_D = -50\text{ A}$	-	60	80	nC
Gate-Source Charge ^c	Q_{gs}		-	5.7	8.6	
Gate-Drain Charge ^c	Q_{gd}		-	14.7	22	
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.5	3	4.5	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -20\text{ V}$, $R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	-	10	15	ns
Rise Time ^c	t_r		-	12	18	
Turn-Off Delay Time ^c	$t_{d(off)}$		-	40	60	
Fall Time ^c	t_f		-	16	24	
Source-Drain Diode Ratings and Characteristics^b						
Pulsed Current ^a	I_{SM}		-	-	-200	A
Forward Voltage	V_{SD}	$I_F = -50\text{ A}$, $V_{GS} = 0\text{ V}$	-	-1	-1.5	V

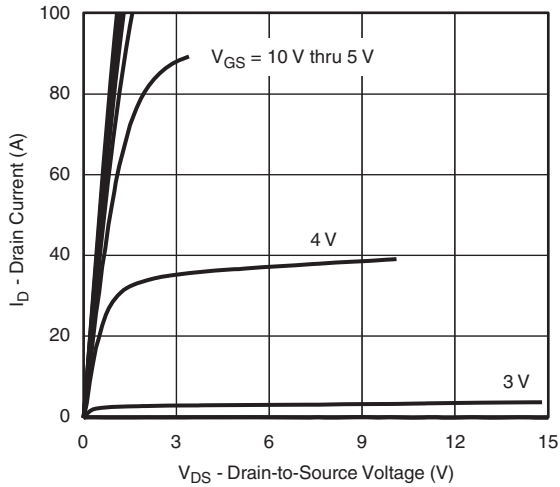
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

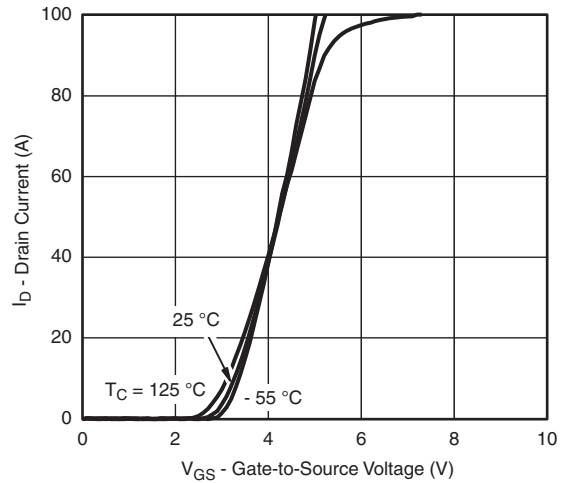
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



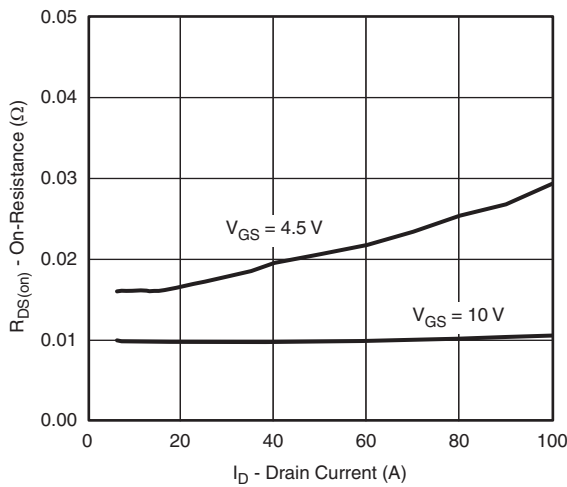
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



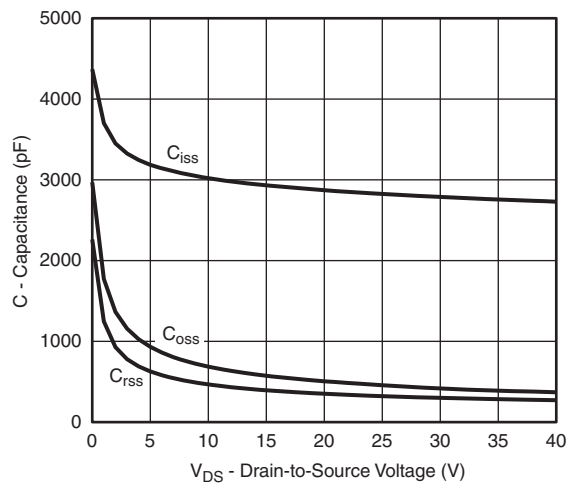
Output Characteristics



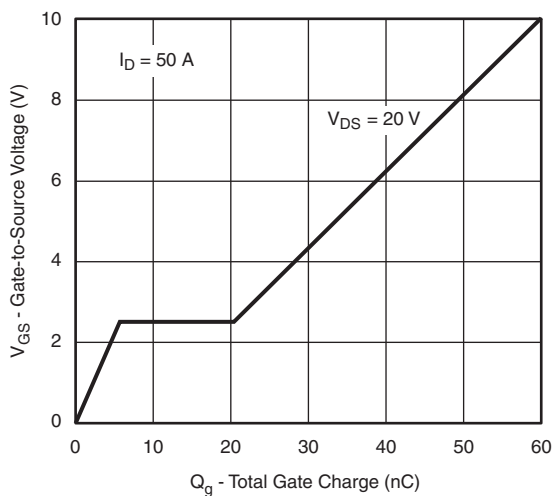
Transfer Characteristics



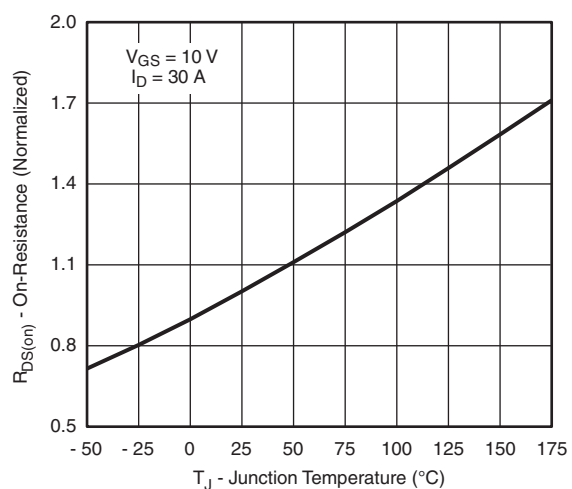
On-Resistance vs. Drain Current



Capacitance



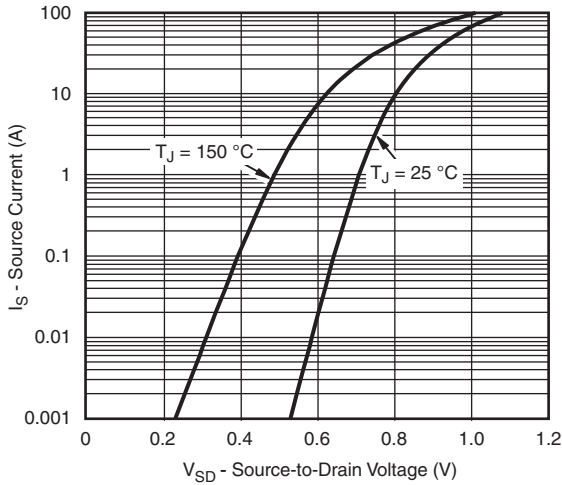
Gate Charge



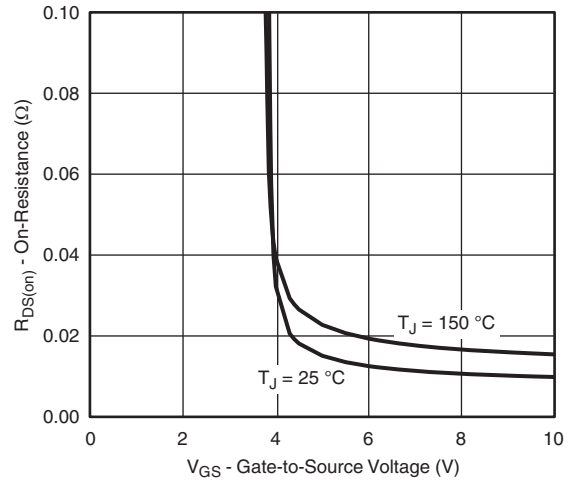
On-Resistance vs. Junction Temperature



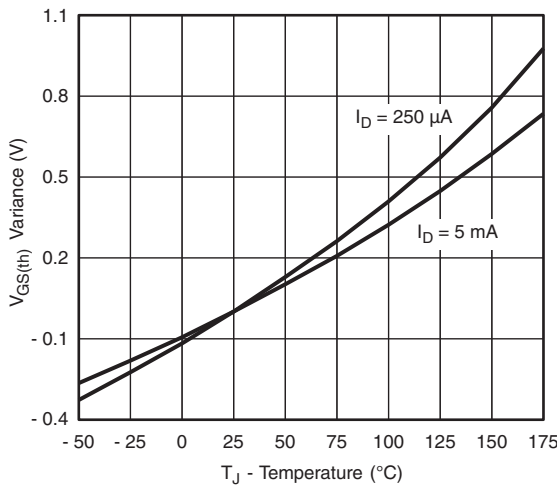
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



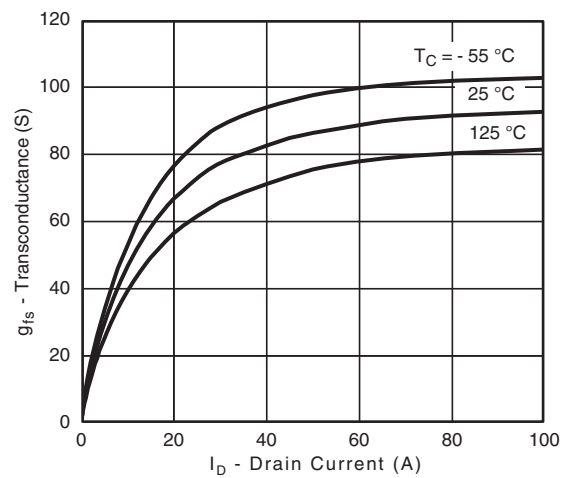
Source Drain Diode Forward Voltage



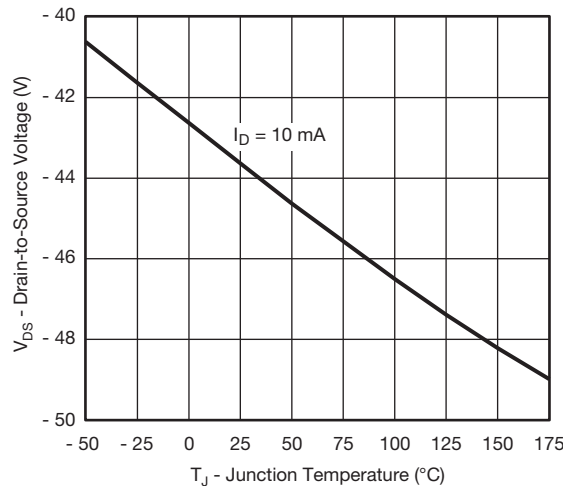
On-Resistance vs. Gate-to Source Voltage



Threshold Voltage



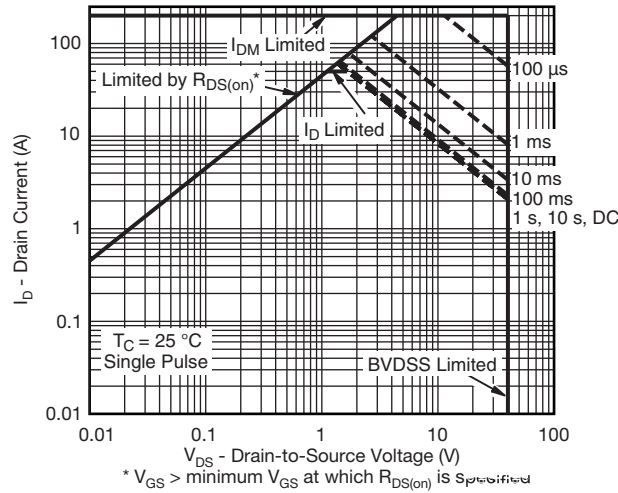
Transconductance



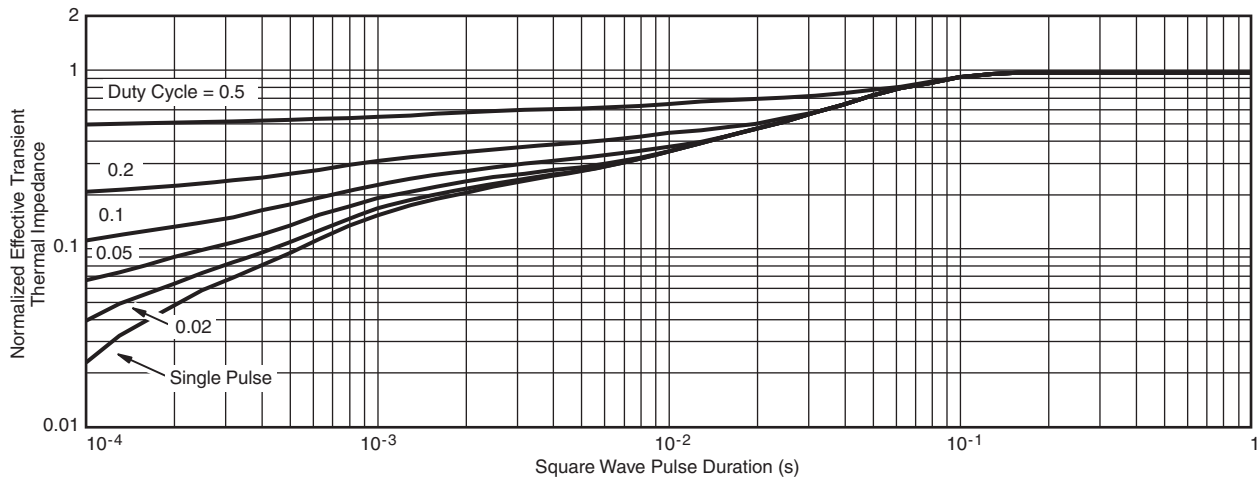
Drain Source Breakdown vs. Junction Temperature



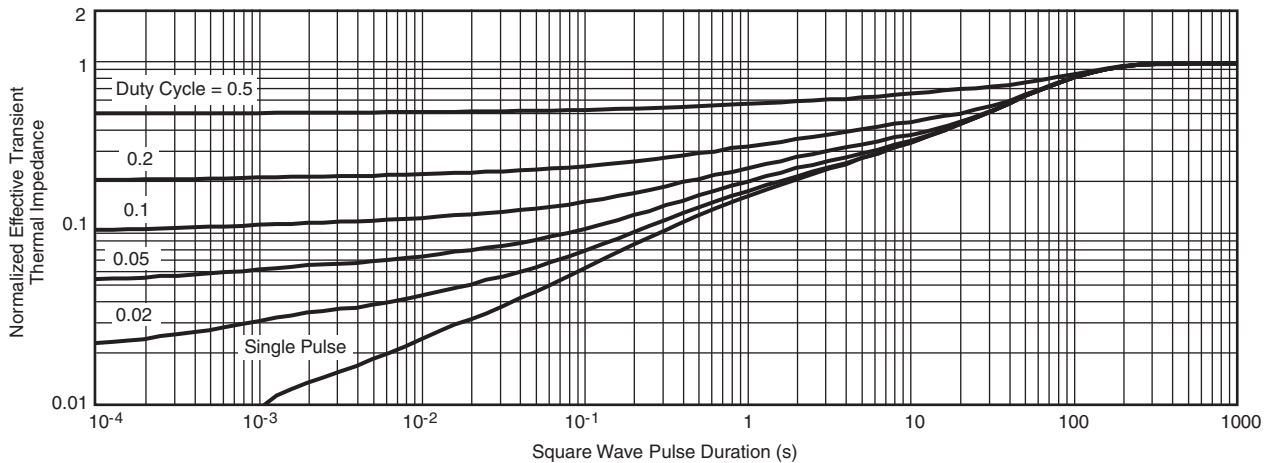
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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REVISION HISTORY ^a		
REVISION	DATE	DESCRIPTION OF CHANGE
D	12-Dec-14	• I_D and P_D ($T_C = 125\text{ }^\circ\text{C}$), UIS , R_{thJC} , $R_{DS(on)}$ ($V_{GS} = 10\text{ V}$ for $T_J = 125\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$) and g_{fs} modified

Note

a. As of April 2014



DPAK / TO-252 and Reverse DPAK

Ordering codes for the SQ rugged series power MOSFETs in the DPAK / TO-252 and Reverse DPAK packages:

Table with 3 columns: DATASHEET PART NUMBER, OLD ORDERING CODE a, and NEW ORDERING CODE. It lists various MOSFET part numbers and their corresponding ordering codes.

Note

a. Old ordering code is obsolete and no longer valid for new orders



TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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