



PH4830L

N-channel TrenchMOS logic level FET

Rev. 01 — 6 September 2007

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level threshold
- Optimized for use in DC-to-DC converters
- 100 % R_G tested
- Lead-free package
- Very low switching and conduction losses
- 100 % ruggedness tested

1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- PC Motherboards

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $R_{DS(on)} \leq 4.8$ m Ω
- $I_D \leq 84$ A
- $Q_{GD} = 5.4$ nC (typ)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)	<p style="text-align: center;">SOT669 (LFAK)</p>	<p style="text-align: center;">mbb076</p>
4	gate (G)		
mb	mounting base; connected to drain (D)		

3. Ordering information

Table 2. Ordering information

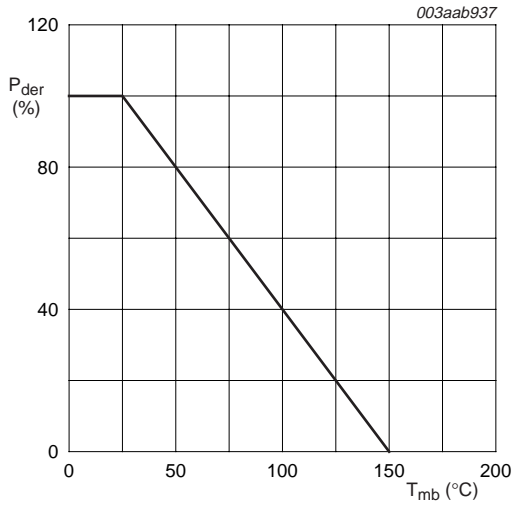
Type number	Package		Version
	Name	Description	
PH4830L	LFPAK	plastic single-ended surface-mounted package (lfpak); 4 leads	SOT669

4. Limiting values

Table 3. Limiting values

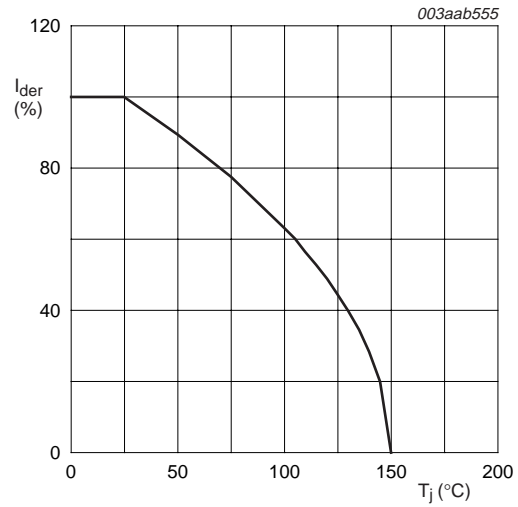
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	84	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	63	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 49\text{ A}$; $t_p = 0.12\text{ ms}$; $V_{DS} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	121	mJ



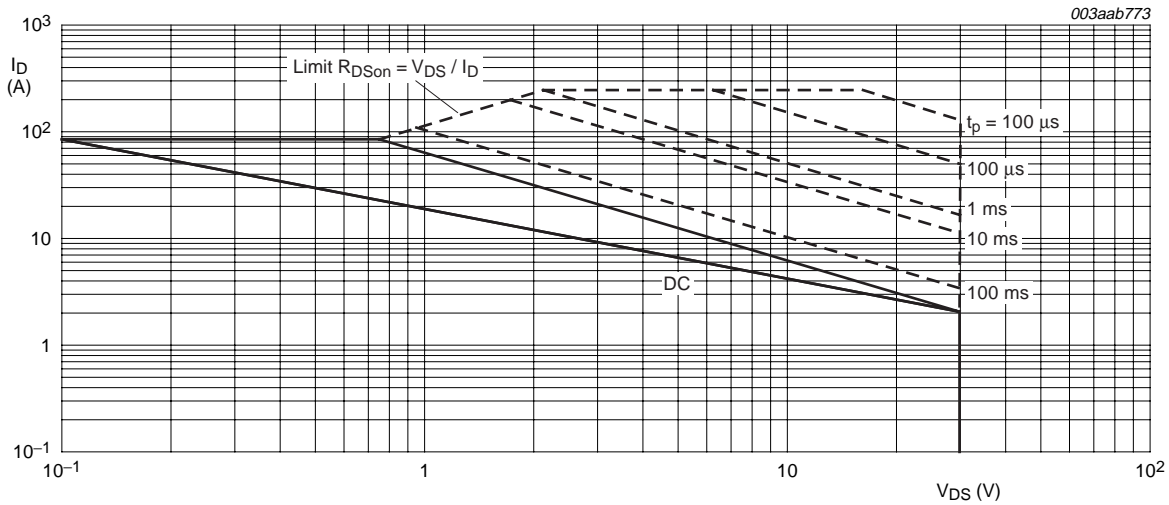
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

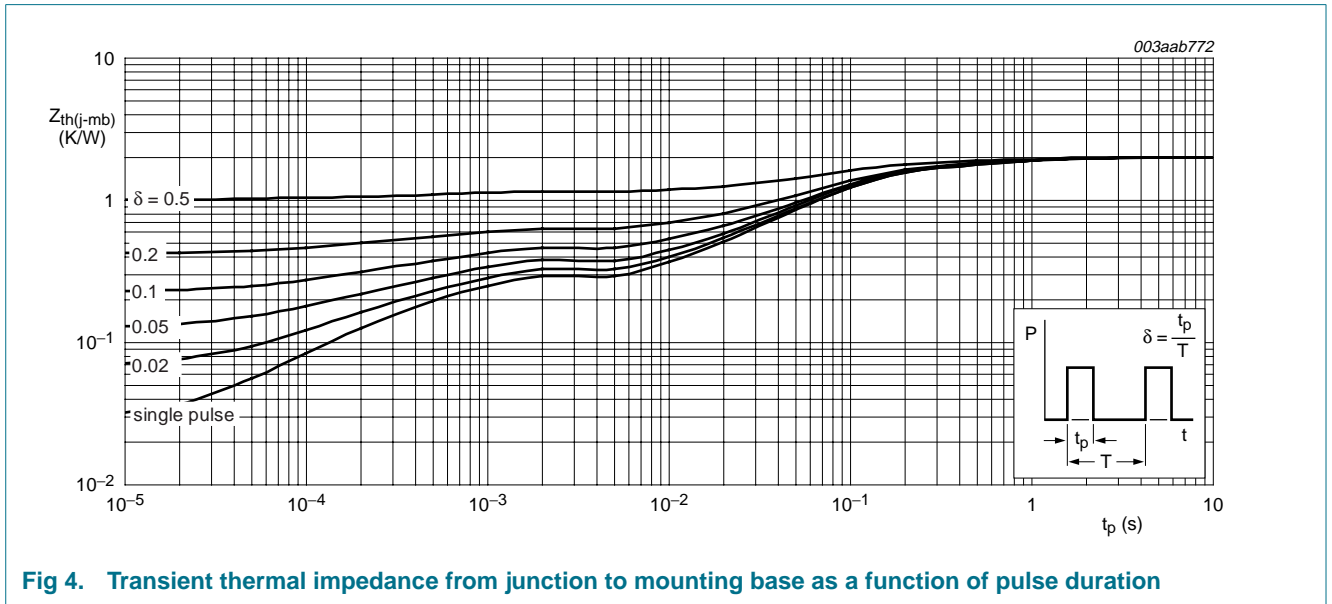


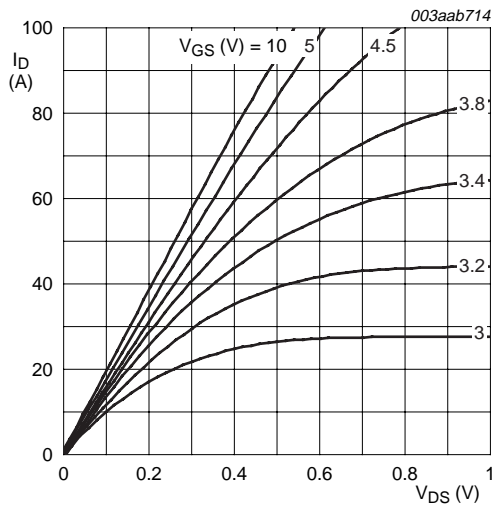
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

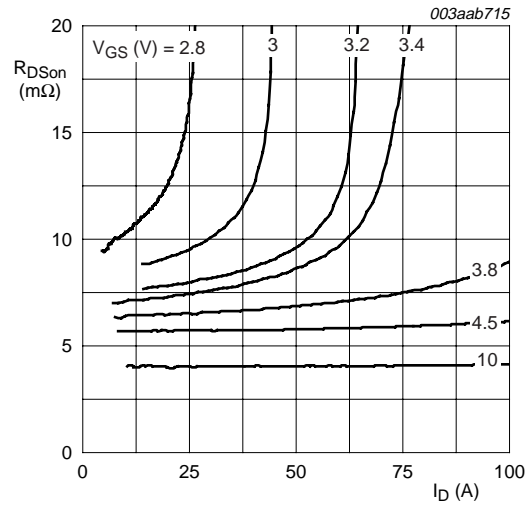
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10 $T_j = 25\text{ °C}$	1.3	1.7	2.15	V
		$T_j = 150\text{ °C}$	0.8	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1.0	μA
		$T_j = 150\text{ °C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	-	100	nA
R_G	gate resistance	$f = 1\ \text{MHz}$	-	0.51	-	Ω
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; see Figure 6 and 8 $T_j = 25\text{ °C}$	-	3.8	4.8	m Ω
		$T_j = 150\text{ °C}$	-	6.3	7.7	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 25\ \text{A}$; see Figure 6 and 8	-	5.6	7.0	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ \text{A}$; $V_{DS} = 12\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 11 and 12	-	22.9	-	nC
Q_{GS}	gate-source charge		-	9.0	-	nC
Q_{GS1}	pre- $V_{GS(th)}$ gate-source charge		-	5.5	-	nC
Q_{GS2}	post- $V_{GS(th)}$ gate-source charge		-	3.5	-	nC
Q_{GD}	gate-drain charge		-	5.4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	2.8	-	V
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 12\ \text{V}$; $f = 1\ \text{MHz}$; see Figure 14	-	2786	-	pF
C_{oss}	output capacitance		-	579	-	pF
C_{rss}	reverse transfer capacitance		-	297	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 0\ \text{V}$; $f = 1\ \text{MHz}$	-	3300	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\ \text{V}$; $R_L = 0.5\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_G = 5.6\ \Omega$	-	28	-	ns
t_r	rise time		-	43	-	ns
$t_{d(off)}$	turn-off delay time		-	35	-	ns
t_f	fall time		-	19	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\ \text{A}$; $V_{GS} = 0\ \text{V}$; see Figure 13	-	0.85	-	V
t_{rr}	reverse recovery time	$I_S = 20\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$; $V_R = 30\ \text{V}$	-	47	-	ns
Q_r	recovered charge		-	17	-	nC



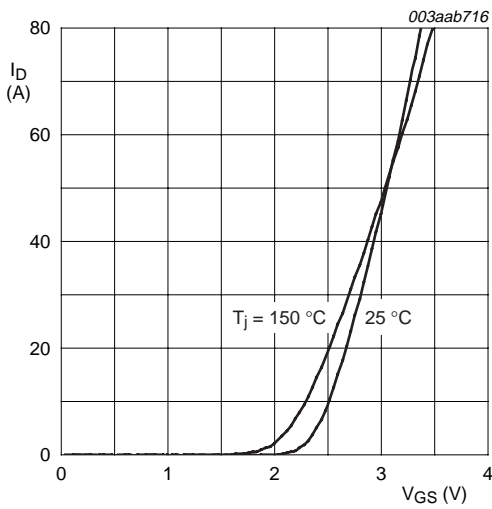
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



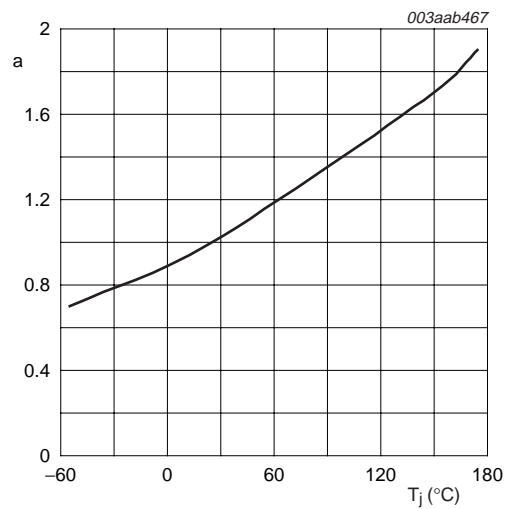
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



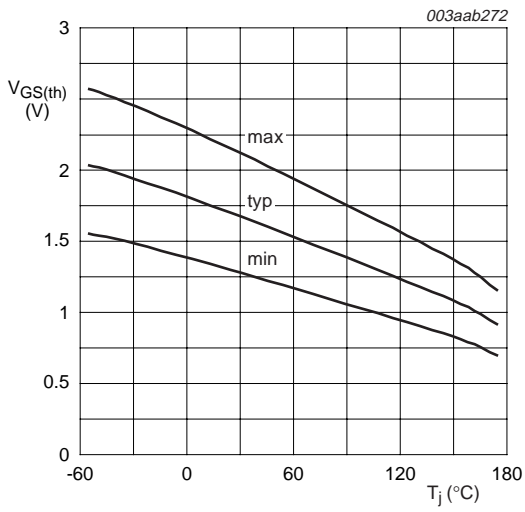
$T_j = 25\text{ }^\circ\text{C}$ and 150 $^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



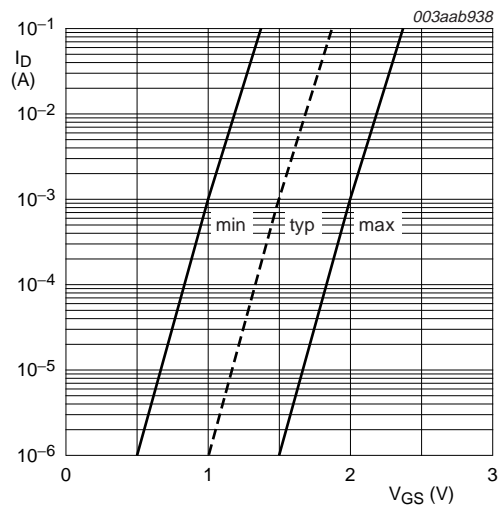
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



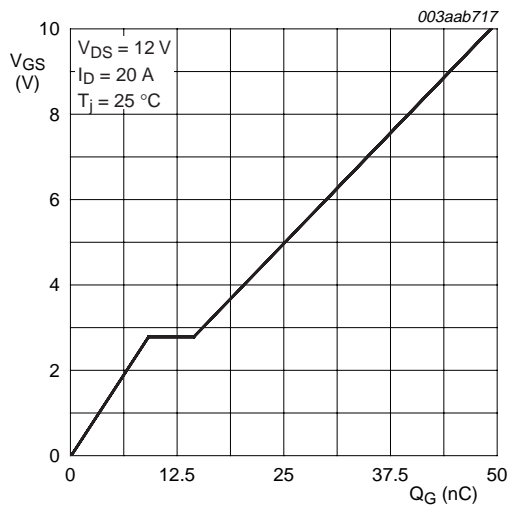
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



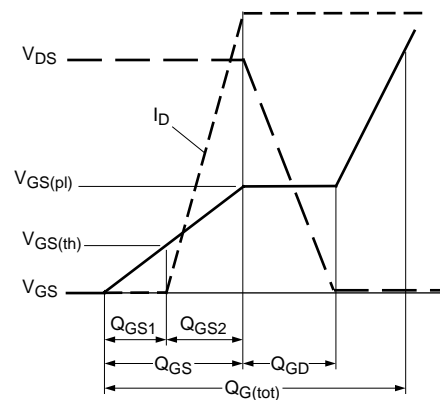
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



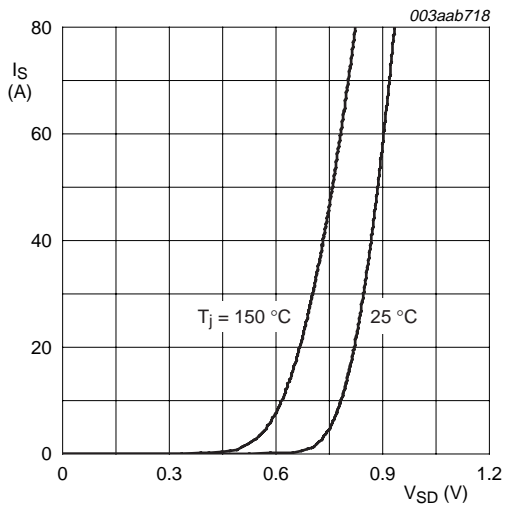
$I_D = 20 \text{ A}; V_{DS} = 12 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



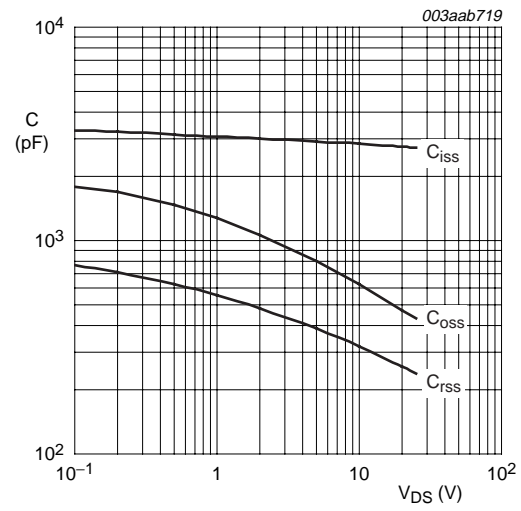
003aaa508

Fig 12. Gate charge waveform definitions



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



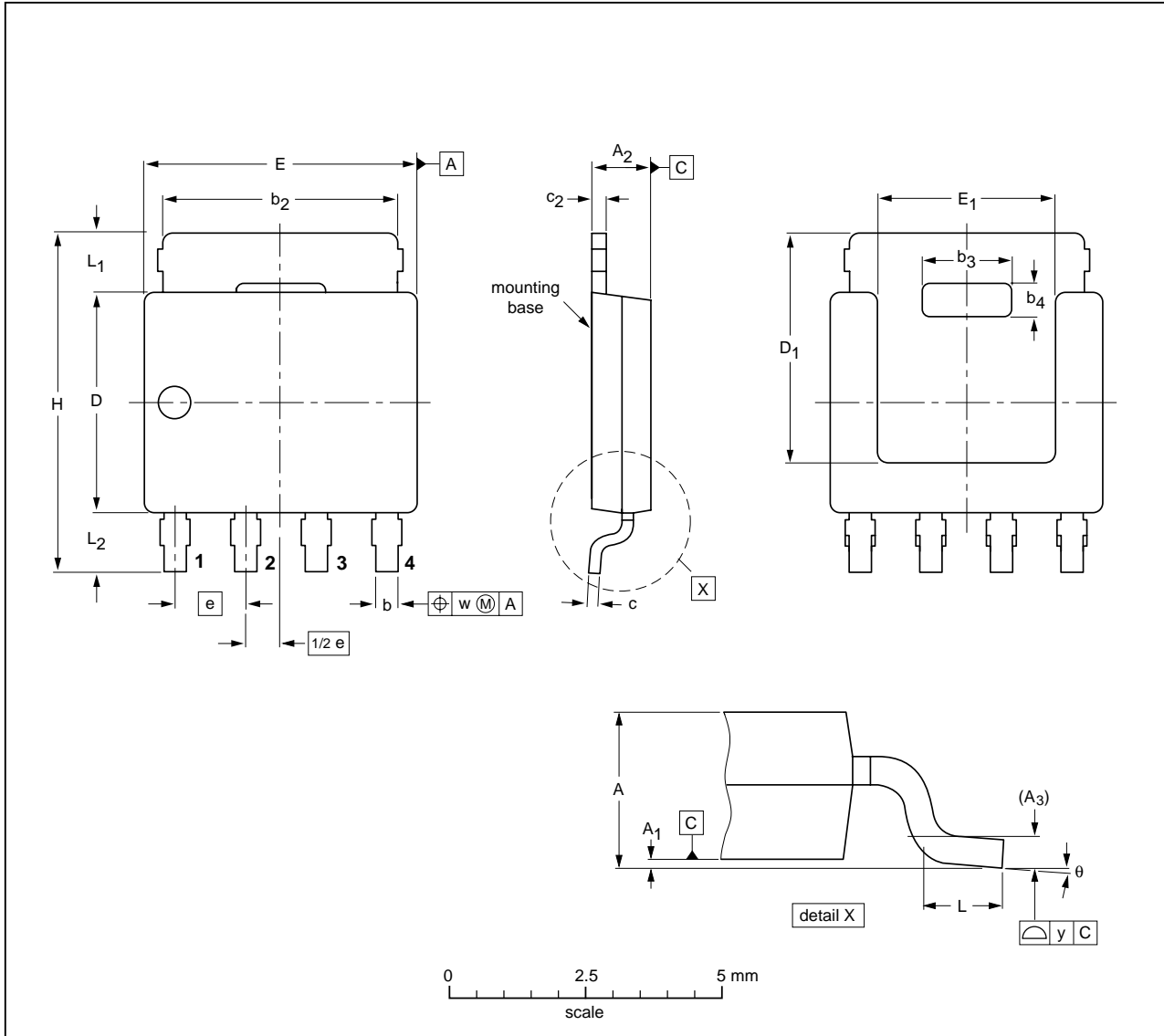
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ max	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			04-10-13 06-03-16

Fig 15. Package outline SOT669 (LPAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH4830L_1	20070906	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Legal information	11
9.1	Data sheet status	11
9.2	Definitions	11
9.3	Disclaimers	11
9.4	Trademarks	11
10	Contact information	11
11	Contents	12

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