# 4-Line BUS-Port ESD-Protection



20397



20453

**MARKING** (example only)



21001

Dot = pin 1 marking
XX = date code
YY = type code (see table below)

## FEATURES

- Ultra compact LLP75-6L package
- Low package height < 0.6 mm
- 4-line USB ESD-protection
- Low leakage current
- Low load capacitance $C_D$ = 0.8 pF
- ESD-protection acc. IEC 61000-4-2
  ± 15 kV contact discharge
  ± 15 kV air discharge
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Pb-free

e4

**RoHS**
COMPLIANT
**HALOGEN**
*FREE*
*GREEN*
*(5-2008)*

## ORDERING INFORMATION

| DEVICE NAME | ORDERING CODE | TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL) | MINIMUM ORDER QUANTITY |
|---|---|---|---|
| VBUS054B-HSF | VBUS054B-HSF-GS08 | 3000 | 15 000 |

## PACKAGE DATA

| DEVICE NAME | PACKAGE NAME | TYPE CODE | WEIGHT | MOLDING COMPOUND FLAMMABILITY RATING | MOISTURE SENSITIVITY LEVEL | SOLDERING CONDITIONS |
|---|---|---|---|---|---|---|
| VBUS054B-HSF | LLP75-6L | U3 | 4.2 mg | UL 94 V-0 | MSL level 1 (according J-STD-020) | 260 °C/10 s at terminals |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | TEST CONDITIONS | SYMBOL | VALUE | UNIT |
|---|---|---|---|---|
| Peak pulse current | Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $I_{PPM}$ | 3 | A |
| | Pin 5 to pin 2 acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $I_{PPM}$ | 10 | A |
| Peak pulse power | Pin 1, 3, 4 or 6 to pin 2 acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $P_{PP}$ | 45 | W |
| | Pin 5 to pin 2 acc. IEC 61000-4-5; $t_P$ = 8/20 µs; single shot | $P_{PP}$ | 200 | W |
| ESD immunity | Contact discharge acc. IEC61000-4-2; 10 pulses | $V_{ESD}$ | ± 15 | kV |
| | Air discharge acc. IEC61000-4-2; 10 pulses | $V_{ESD}$ | ± 15 | kV |
| Operating temperature | Junction temperature | $T_J$ | -40 to +125 | °C |
| Storage temperature | | $T_{STG}$ | -55 to +150 | °C |

## ELECTRICAL CHARACTERISTICS VBUS054B-HSF

| PARAMETER | TEST CONDITIONS/REMARKS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Protection paths | Number of line which can be protected | $N_{channel}$ | - | - | 4 | lines |
| Reverse stand-off voltage | at $I_R$ = 0.1 µA, pin 1, 3, 4 or 6 to pin 2 | $V_{RWM}$ | - | - | 5 | V |
| Reverse current | at $V_{IN}$ = $V_{RWM}$ = 5 V, pin 1, 3, 4 or 6 to pin 2 | $I_R$ | - | < 0.01 | 0.1 | µA |
| Reverse breakdown voltage | at $I_R$ = 1 mA, pin 5 to pin 2 | $V_{BR}$ | 6.3 | 7.1 | 8 | V |
| | at $I_R$ = 1 mA, pin 1, 3, 4 or 6 to pin 2 | $V_{BR}$ | 6.9 | 7.9 | 8.7 | V |
| Reverse clamping voltage | at $I_{PP}$ = 3 A; pin 1, 3, 4 or 6 to pin 2; acc. IEC 61000-4-5 | $V_C$ | - | - | 15 | V |
| Forward clamping voltage | at $I_F$ = 3 A; pin 2 to pin 1, 3, 4 or 6; acc. IEC 61000-4-5 | $V_F$ | - | - | 5 | V |
| Capacitance | Pin 1, 3, 4 or 6 to pin 2 $V_{IN}$ (at pin 1, 3, 4 or 6) = 0 V and $V_{BUS}$ (at pin 5) = 5 V; f = 1 MHz | $C_D$ | - | 0.8 | 1 | pF |
| | Pin 1, 3, 4 or 6 to pin 2 $V_{IN}$ (at pin 1, 3, 4 or 6) = 2.5 V and $V_{BUS}$ (at pin 5) = 5 V; f = 1 MHz | $C_D$ | - | 0.5 | 0.8 | pF |
| Line symmetry | Difference of the line capacitances | $dC_D$ | - | - | 0.05 | pF |
| Supply line capacitance | Pin 5 to pin 2; at $V_R$ = 0; f = 1 MHz | $C_{ZD}$ | - | 110 | - | pF |

**Note**

• Ratings at 25 °C, ambient temperature unless otherwise specified

## TYPICAL CHARACTERISTICS ($T_{amb}$ = 25 °C, unless otherwise specified)
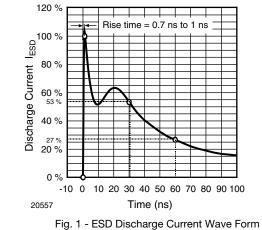


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Fig. 1 - ESD Discharge Current Wave Form
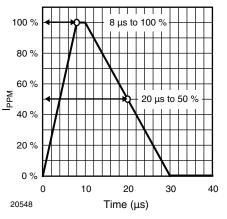acc. IEC 61000-4-2 (330 Ω/150 pF)



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Fig. 2 - 8/20 µs Peak Pulse Current Wave Form
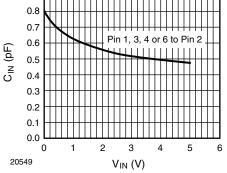acc. IEC 61000-4-5

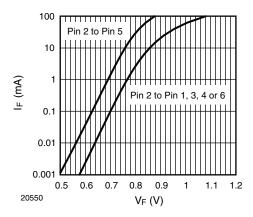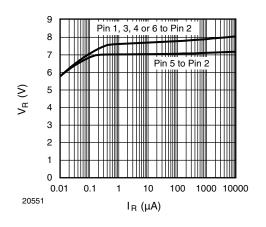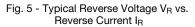Fig. 3 - Typical Input Capacitance $C_{IN}$ at Pin 1, 3, 4, or 6 vs. Input Voltage $V_{IN}$

Fig. 4 - Typical Forward Current $I_F$ vs. Forward Voltage $V_F$

Fig. 5 - Typical Reverse Voltage $V_R$ vs. Reverse Current $I_R$
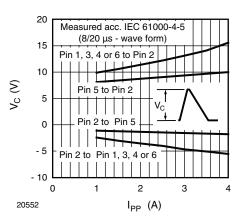
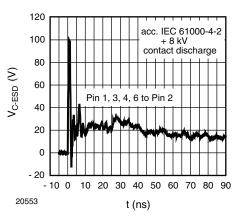Fig. 6 - Typical Peak Clamping Voltage $V_C$ vs. Peak Pulse Current $I_{PP}$

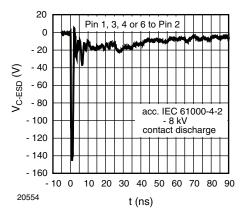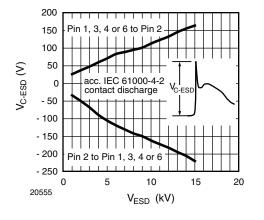Fig. 7 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

Fig. 8 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

Fig. 9 - Typical Peak Clamping Voltage at ESD
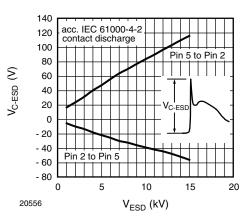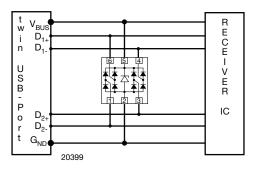Contact Discharge (acc. IEC 61000-4-2)



Fig. 10 - Typical Peak Clamping Voltage at ESD
Contact Discharge (acc. IEC 61000-4-2)

## APPLICATION NOTE

With the **VBUS054B-HSF** a double, high speed USB-port or up to 4 other high speed signal or data lines can be protected against transient voltage signals. Negative transients will be clamped close below the ground level while positive transients will be clamped close above the 5 V working range. An avalanche diode clamps the supply line ($V_{BUS}$ at pin 5) to ground (pin 2). The high speed data lines, $D_{1+}$, $D_{2+}$, $D_{1-}$ and $D_{2-}$, are connected to pin 1, 3, 4 and 6. As long as the signal voltage on the data lines is between the ground- and the $V_{BUS}$-level, the low capacitance PN-diodes offer a very high isolation to $V_{BUS}$, ground and to the other data lines. But as soon as any transient signal exceeds this working range, one of the PN-diodes starts working in the forward mode and clamps the transient to ground or to the avalanche breakthrough voltage level of the Z-diode between pin 5 and pin 2.
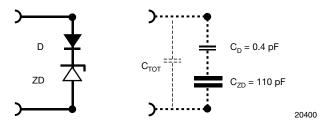
**BACKGROUND KNOWLEDGE:**

A Zener- or avalanche diode is an ideal device for "cutting" or "clamping" voltage spikes or voltage transients down to low and uncritical voltage values. The breakthrough voltage can easily be adjusted by the chip-technology to any desired value within a wide range. Up to about 6 V the "zener-effect" (tunnel-effect) is responsible for the breakthrough characteristic. Above 6 V the so-called "avalanche-effect" is responsible. This is a more abrupt breakthrough phenomenon. Because of the typical "Z-shape" of the current-voltage-curve of such diodes, these diodes are generally called "Z-diode" (= zener or avalanche diodes). An equally important parameter for a protection diode is the ESD- and surge-power that allows the diode to short current in the pulse to ground without being destroyed.

This requirement can be adjusted by the size of the silicon chip (crystal). The bigger the active area the higher the current that the diode can short to ground.
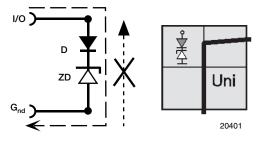
But the active area is also responsible for the diode capacitance - the bigger the area the higher the capacitance.

The dilemma is that a lot of applications require an effective protection against more then 8 kV ESD while the capacitance must be lower then 5 pF! This is well out of the normal range of a Z-diode. However, a protection diode with a low capacitance PN-diode (switching diode or junction diode) in series with a Z-diode, can fulfil both requirements simultaneously: low capacitance AND high ESD- and/or surge immunity become possible!
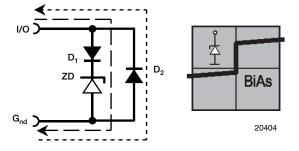
A small signal ($V_{pp} < 100$ mV) just sees the low capacitance of the PN-diode, while the big capacitance of the Z-diode in series remains "invisible".



$C_D = 0.4$ pF

$C_{ZD} = 110$ pF

20400

Such a constellation with a Z-diode and a small PN-diode (with low capacitance) in series (anti-serial) is a real unidirectional protection device. The clamping current can only flow in one direction (forward) in the PN-diode. The reverse path is blocked.



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Another PN-diode "opens" the back path so that the protection device becomes bidirectional! Because the clamping voltage levels in forward and reverse directions are different, such a protection device has a **Bi**directional and **As**ymmetrical clamping behaviour (**BiAs**) just like a single Z-diode.



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For technical questions, contact: ESDprotection@vishay.com

One mode of use is,…

in the very first moment before any pulses have arrived, all three diodes are completely discharged (so the diode capacitances are empty of charge) the first signal pulse with an amplitude > 0.5 V will drive the upper PN-diode ($D_1$) in a forward direction and "sees" the empty capacitance of the Z-diode (ZD).
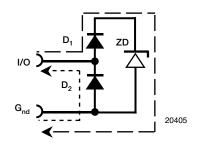
Depending on the duration of this pulse and the pause to the next one the Z-diodes capacitance can be charged up so that the next pulse "sees" a lower capacitance. After some pulses the big Z-diode could be completely charged up so that the following pulses just see the small capacitance of both PN-diodes.

For some application this can work perfectly.....
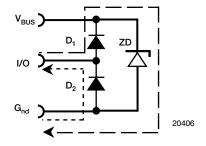


For others applications the capacitance must be the same all the time from the first till the last pulse.

For these applications the appropriate mode of use is to connect the Z-diode to the supply voltage.

In this mode the Z-diode is charged up immediately by the supply voltage and both PN-diodes are always used in reverse. This keeps their capacitance at a minimum.

**PACKAGE DIMENSIONS** in millimeters (inches): **LLP75-6L**



Heat sink

1.05 (0.041)
0.95 (0.037)

0.3 (0.012) / 0.2 (0.008)

0.3 (0.012) / 0.2 (0.008)

0.3 (0.012) / 0.2 (0.008)

1 (0.039)

0.55 (0.022) / 0.45 (0.018)

0.5 (0.020)

0.6 (0.024)

0.25 (0.010)

0.60 (0.023) / 0.54 (0.021)

0.05 (0.002) / 0 (0.000)

0.15 (0.006)

Pin 1 marking

1.65 (0.065)
1.55 (0.061)

1.65 (0.065)
1.55 (0.061)

Foot print recommendation:

0.5 (0.020)     0.5 (0.020)

0.3 (0.012)     0.3 (0.012)

0.15 (0.006)     0.15 (0.006)

0.25 (0.010)

1 (0.039)

0.5 (0.020)

1 (0.039)

0.5 (0.020)

Solder resist mask

Solder pad

Document no.:S8-V-3906.02-010 (4)
Created - Date: 04. MAY 2005
Rev. 4 - Date: 21. March 2006
20454

LLP75-6x

Pad layout - view from top / seen at bottom side

S8-V-3906.02-004 (4)
10.01.2005

Pin 1 - location

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