NB632

High Effeciency 4A, 24V, 500kHz Synchronous Step-down Converter

The Future of Analog IC Technology

DESCRIPTION

The NB632 is a high frequency synchronous rectified step-down switch mode converter with built-in internal power MOSFETs. It offers a very compact solution to achieve 4A continuous output current over a wide input supply range with excellent load and line regulation. The NB632 operates at high efficiency over a wide output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include latch-off OCP and thermal shut down.

The NB632 requires a minimum number of readily available standard external components and is available in a space saving 3mm x 4mm 14-pin QFN package.

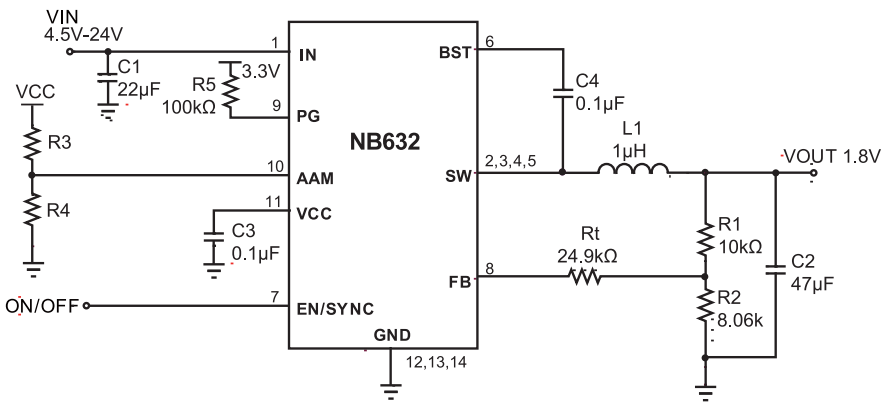
FEATURES

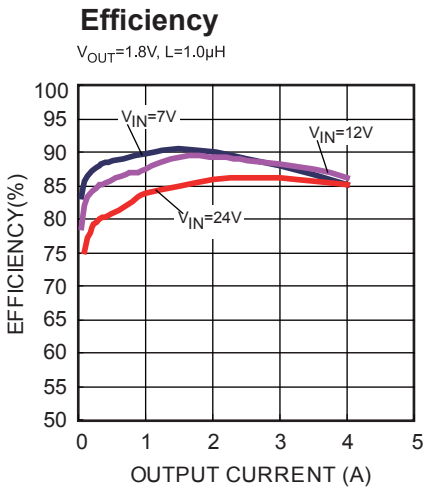
- Wide 4.5V to 24V Operating Input Range
- 4A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Fixed 500kHz Switching Frequency
- Sync from 300kHz to 2MHz External Clock
- Internal Compensation
- Latch-off OCP Protection and Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a 14-pin, QFN 3x4mm Package

APPLICATIONS

- Notebook Systems and I/O Power
- Networking Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION （FOR NOTEBOOK）



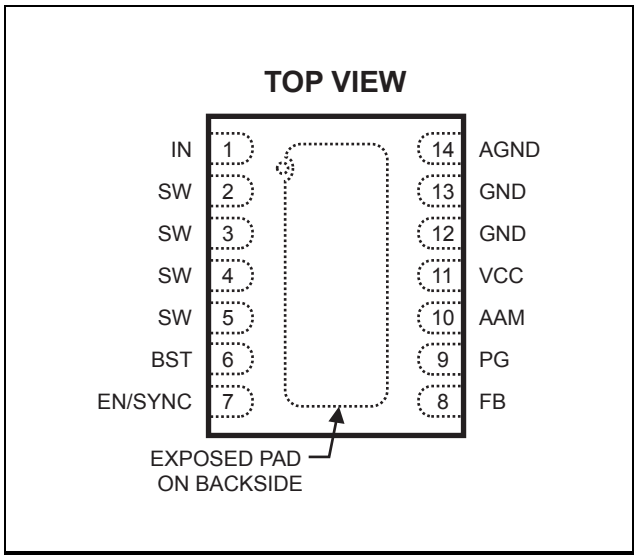


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
NB632EL	QFN14 (3mm x 4mm)	632E	–20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. NB632EL–Z);
For RoHS compliant packaging, add suffix –LF; (e.g. NB632EL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 28V
V_{SW} .....–0.3V (-5V for 10ns) to 28V
V_{BS} ..... V_{SW} + 6V
All Other Pins .....–0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.6W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 24V
Operating Junct. Temp. (T_J).... –20°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
QFN14 (3mm x 4mm)	48	11 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\ (MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\ (MAX)} = (T_{J\ (MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0		μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V		1		mA
HS Switch On Resistance (5)	HS_{RDS-ON}			120		mΩ
LS Switch On Resistance (5)	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current Limit	I_{LIMIT}			7		A
Oscillator Frequency	F_{SW}	V_{FB} = 0.75V	350	500	650	kHz
Fold-back Frequency	F_{FB}	V_{FB} = 100mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB} = 700mV	85	90		%
Sync Frequency Range	F_{SYNC}		0.3		2	MHz
Feedback Voltage	V_{FB}		785	805	825	mV
Feedback Current	I_{FB}	V_{FB} = 800mV		10	50	nA
EN/SYNC Input Low Voltage	VIL_{EN}				0.4	V
EN/SYNC Input High Voltage	VIH_{EN}		2			V
EN Input Current	I_{EN}	V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
EN Turn Off Delay	EN_{Td-Off}			5		μsec
Power Good Rising Threshold	PG_{Vth-Hi}			0.9		V_{FB}
Power Good Falling Threshold	PG_{Vth-Lo}			0.7		V_{FB}
Power Good Delay	PG_{Td}			250		μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			10	nA
V_{IN} Under Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.8	4.0	4.2	V
V_{IN} Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		5		%
Thermal Shutdown	T_{SD}			150		°C

Notes:

5) Guaranteed by design.

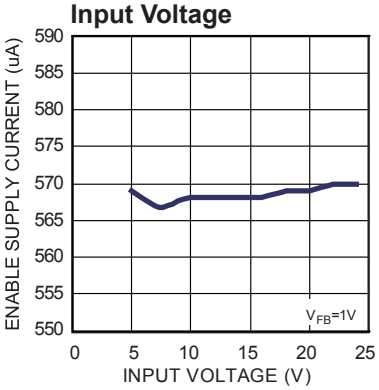
PIN FUNCTIONS

Pin #	Name	Description
1	IN	Supply Voltage. The NB632 operates from a +4.5V to +24V input rail. C1 is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2, 3, 4, 5	SW	Switch Output. Use wide PCB traces and multiple vias to make the connection.
6	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
7	EN/SYNC	EN=1 to enable the NB632. External clock can be applied to EN pin for changing switching frequency. For automatic start-up, connect EN pin to VIN with 100kΩ resistor.
8	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 100mV.
9	PG	Power Good Output, the output of this pin is open drain. Power good threshold is 90% low to high with typical 250μs delay and 70% high to low of regulation value.
10	AAM	Connects to a voltage set by 2 resistor dividers from VCC forces NB632 into non-synchronous mode when load is small.
11	VCC	Bias Supply. Decouple with 0.1μF capacitor.
12, 13	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
14	AGND	Ground. Connect these pins with larger copper areas to the negative terminals of the input and output capacitors. Connect exposed pad to GND plane for proper thermal performance.

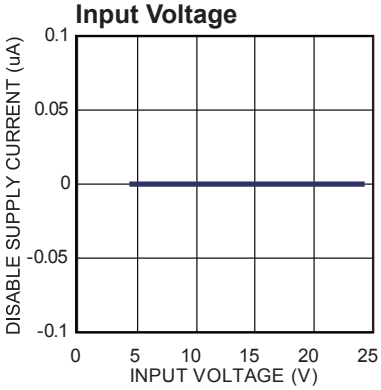
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT} =1.8V, L=1.0µH, T_A=+25°C, unless otherwise noted.

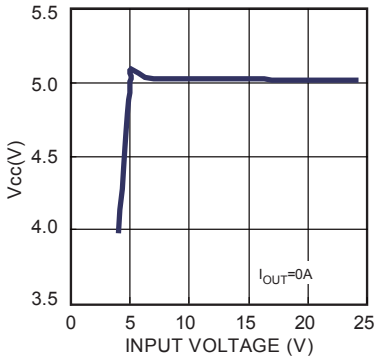
Enabled Supply Current vs. Input Voltage



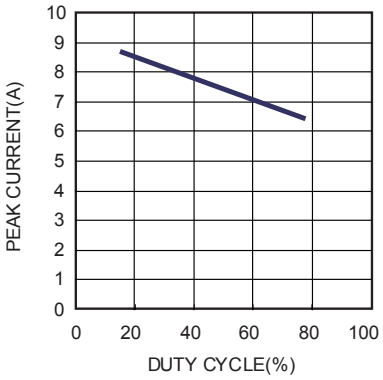
Disabled Supply Current vs. Input Voltage



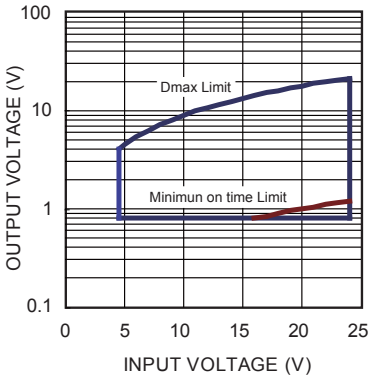
VCC Regulator Line Regulation



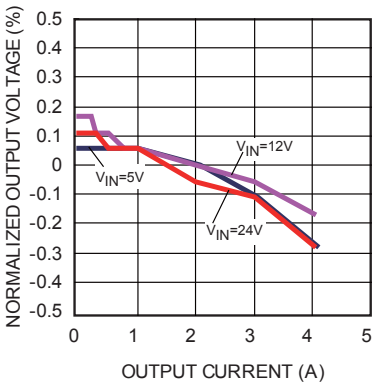
Peak Current vs. Duty Cycle



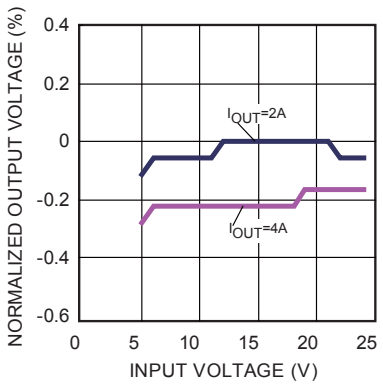
Operating Range



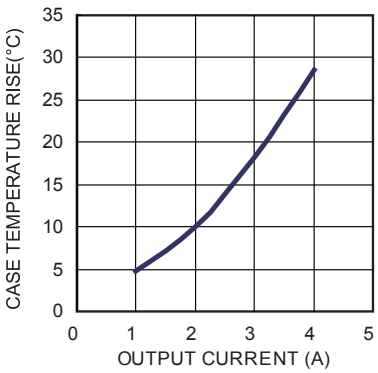
Load Regulation



Line Regulation

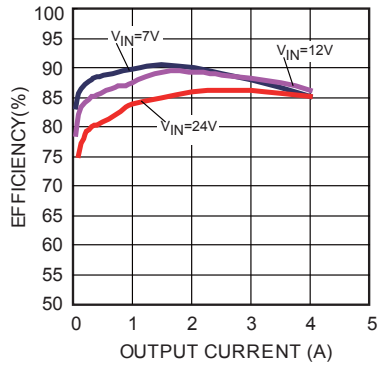


Case Temperature Rise vs. Output Current



Efficiency

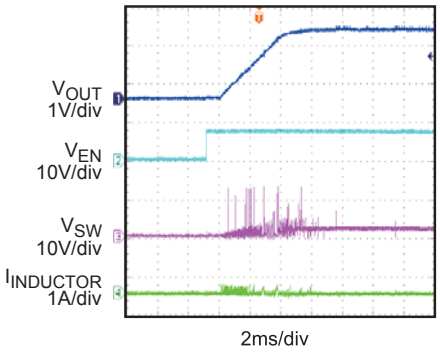
V_{OUT}=1.8V, L=1.0µH



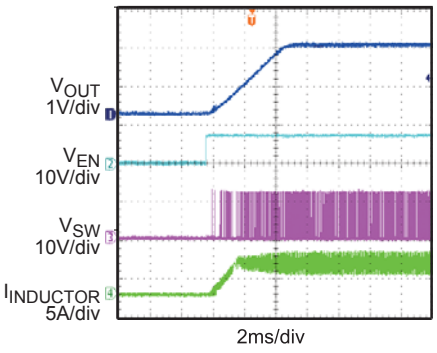
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT} =1.8V, L=1.0µH, T_A=+25°C, unless otherwise noted.

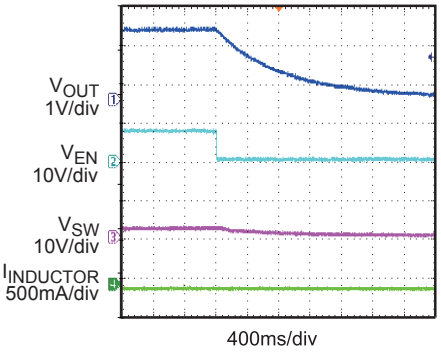
Enable Startup
I_{OUT}=0A



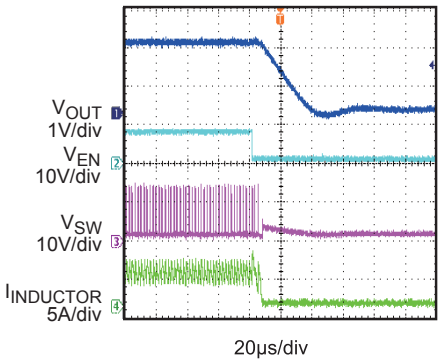
Enable Startup
I_{OUT}=4A



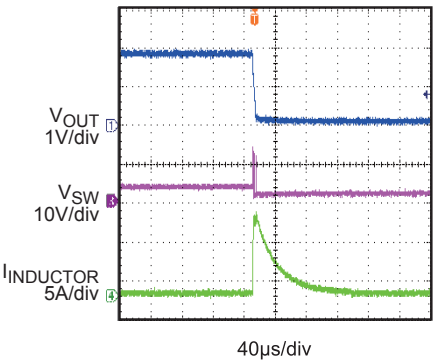
Enable Shut Down
I_{OUT}=0A



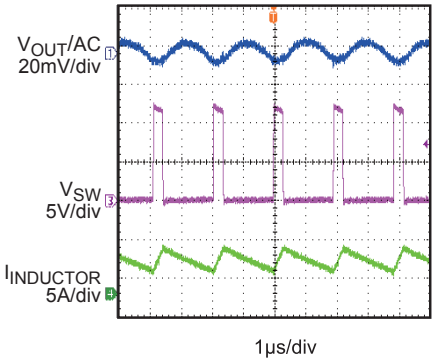
Enable Shut Down
I_{OUT}=4A



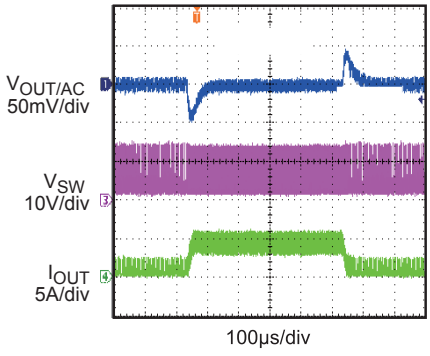
Short Circuit Protection



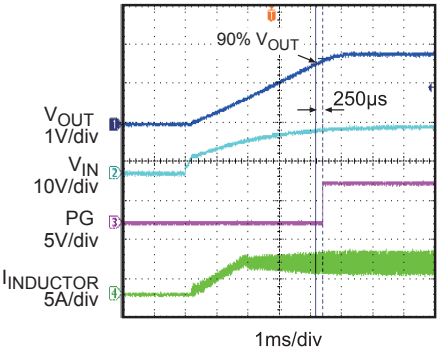
Output Ripple Voltage
I_{OUT}=4A



Load Transient Response
I_{OUT}=0.4A-4A@ 2.5A/µs



PG Delay @ Start up
I_{OUT}=4A, 250µs delay



BLOCK DIAGRAM

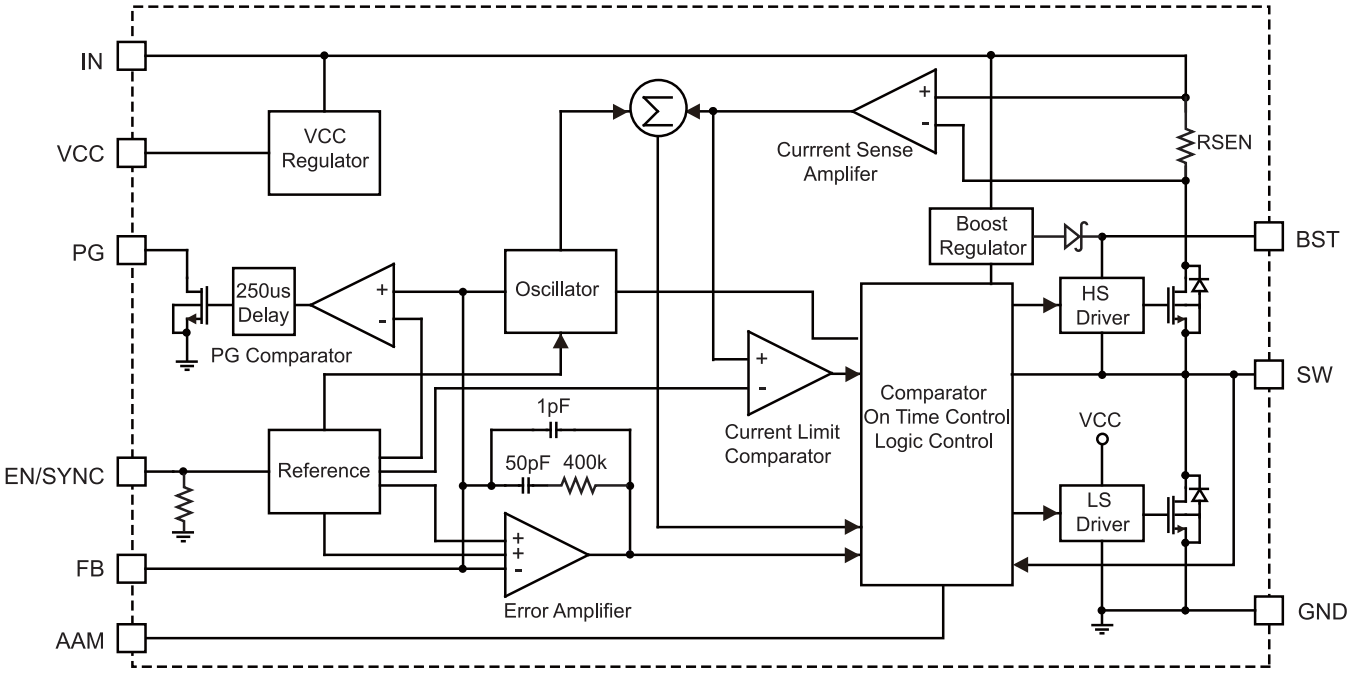


Figure 1—Function Block Diagram

OPERATION

The NB632 is a high frequency synchronous rectified step-down switch mode converter with built-in internal power MOSFETs. It offers a very compact solution to achieve more than 4A continuous output current over a wide input supply range with excellent load and line regulation.

The NB632 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases, a 0.1uF ceramic capacitor for decoupling purpose is required.

Enable/Sync Control

The NB632 has a dedicated Enable/Sync control pin (EN/SYNC). By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN through a resistor for automatic start up. To disable the part, EN must be pulled low for at least 5μs.

The NB632 can be synchronized to an external clock ranging from 300 kHz to 2MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The NB632 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Over-Current-Protection and Latch off

The NB632 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold.

When output voltage drops below 70% of the reference, and inductor current exceeds the current limit at the meantime, NB632 will be latched off. This is especially useful to ensure system safety under fault condition. The NB632 clears the latch once the EN or input power is recycled.

The latch-off function is disabled during soft-start duration.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1 and C2 (Figure 2). If (VIN-VSW) is more than 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

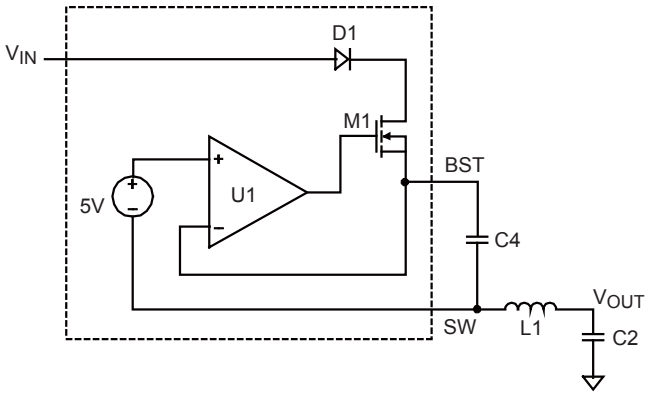


Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 to be around 10kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

The T-type network is highly recommended when Vo is low, as Figure 3 shows.

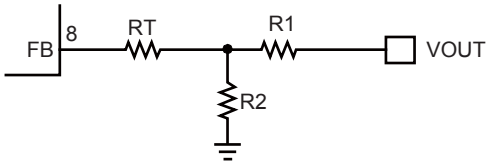


Figure 3— T-type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.05	3.09(1%)	10(1%)	24.9(1%)
1.2	4.99(1%)	10(1%)	24.9(1%)
1.8	10(1%)	8.06(1%)	24.9(1%)
2.5	10(1%)	4.75(1%)	24.9(1%)
3.3	10(1%)	3.16(1%)	24.9(1%)
5	10(1%)	1.91(1%)	24.9(1%)

Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Setting the AAM Voltage

The AAM voltage is used for setting the transition point from AAM to CCM. It should be chosen to provide the best combination of efficiency, stability, ripple, and transient.

If the AAM voltage is set lower, then stability and ripple improve, but efficiency during AAM mode and transient degrades. Likewise, if the AAM voltage is set higher, then the efficiency during AAM and transient improves, but stability and ripple degrade. Therefore the optimal balance point of AAM voltage for good efficiency, stability, ripple and transient should be selected.

As figure 4 shows, AAM voltage can be set by using a resistor divider.

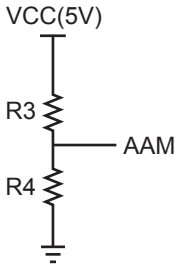


Figure 4— AAM Network

The optimized AAM voltage can be set according to Figure 5. Generally, choose R4 to be around 10 kΩ, R3 is then determined by the following equation:

$$R3 = R4\left(\frac{VCC}{AAM} - 1\right)$$

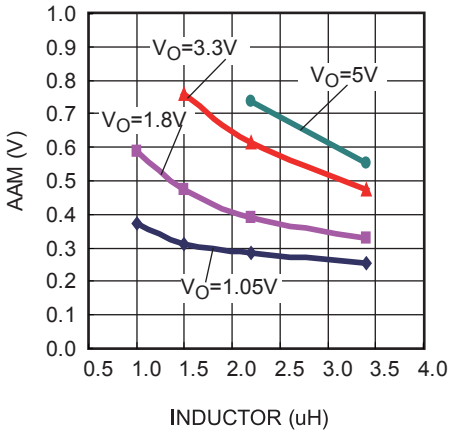


Figure 5— AAM Selection for Common Output Voltages (V_{IN}=5V-24V)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = 2VOUT, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The NB632 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 6.

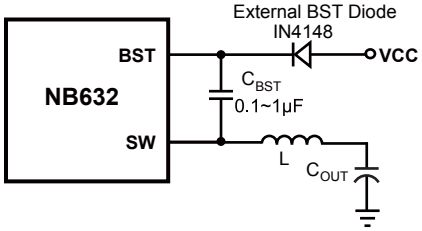
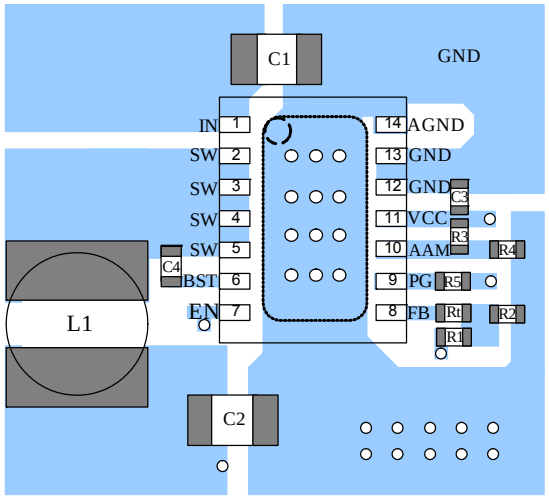


Figure 6—Add Optional External Bootstrap Diode to Enhance Efficiency

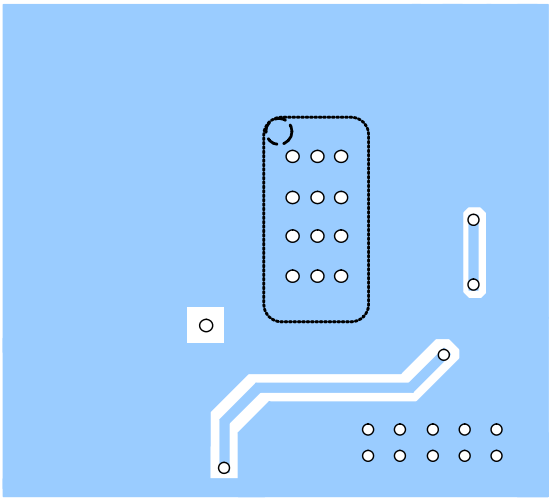
The recommended external BST diode is IN4148, and the BST cap is 0.1~1uF.

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.



Top Layer

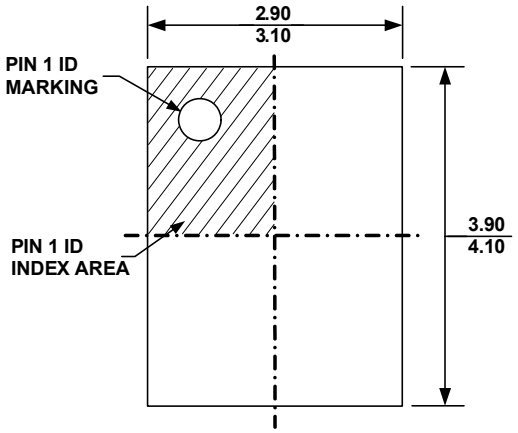


Bottom Layer

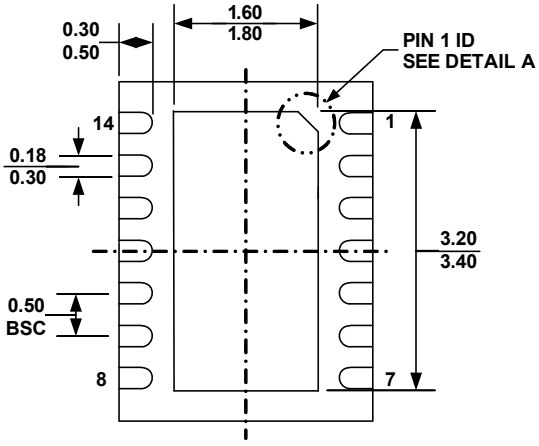
Figure 7—PCB Layout

PACKAGE INFORMATION

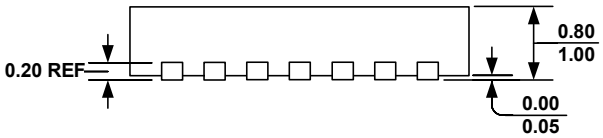
3mm x 4mm QFN14



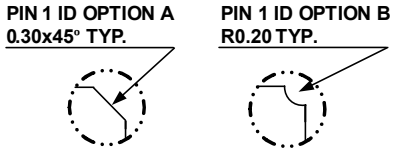
TOP VIEW



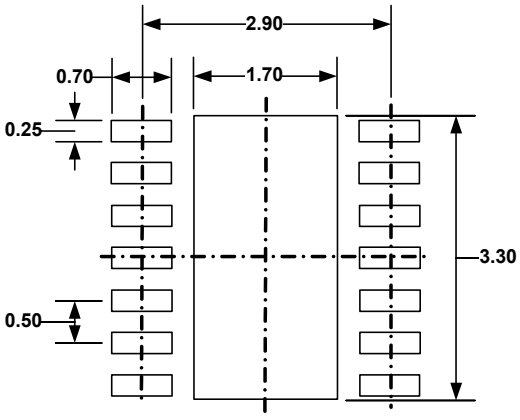
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE