

High Performance Differential Fanout Buffer

Features

- 6 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFP-32 package

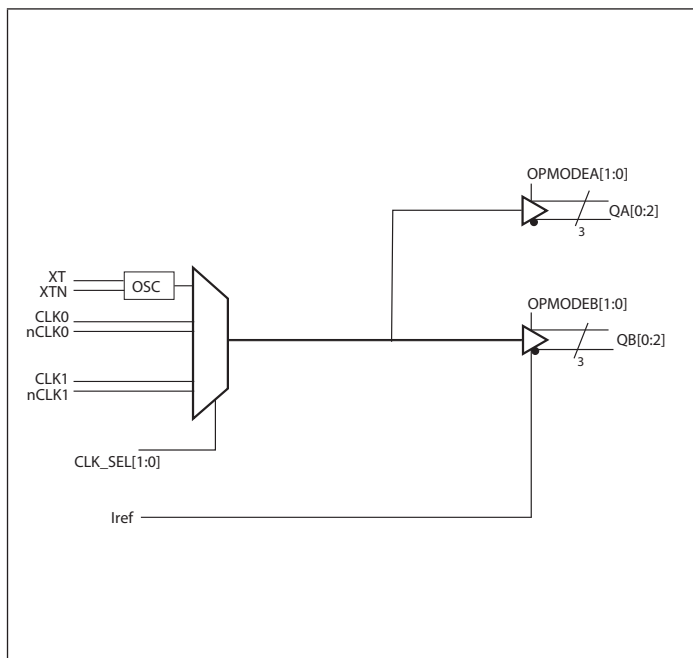
Description

The PI6C49S1506 is a high performance fanout buffer device which supports up to 1.5GHz frequency. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibilities to users. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

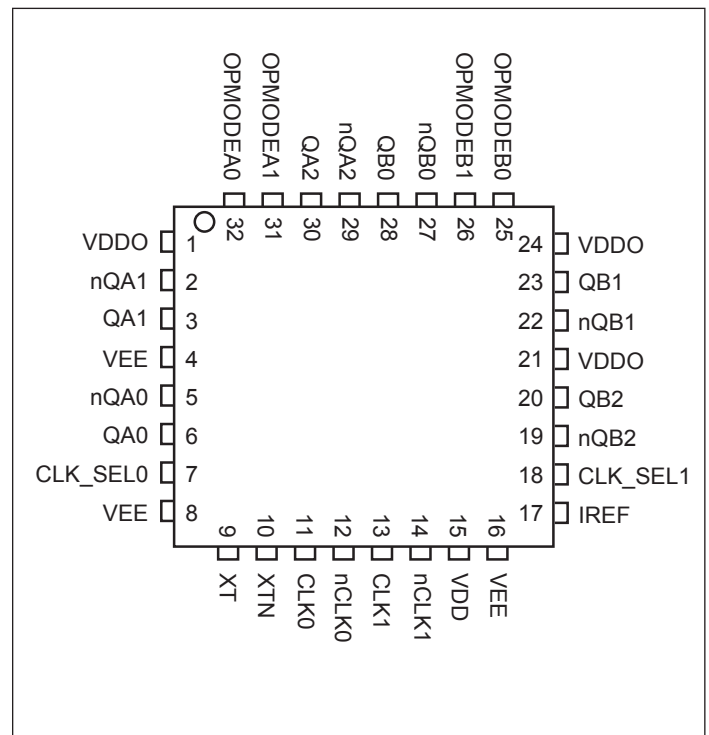
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (32-Pin TQFP)



Pinout Table

| Pin # | Pin Name | Type | Description |
|-----------|------------------|--------|--|
| 1, 21, 24 | V _{DDO} | Power | Power supply pins for outputs |
| 2,3 | nQA1 QA1 | Output | Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 4, 16 | V _{EE} | Power | Connect to Negative power supply |
| 5, 6 | nQA0 QA0 | Output | Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 7 | CLK_SEL0 | Input | Input clock source selection |
| 8 | V _{EE} | Power | Negative power supply |
| 9 | XT | Input | XTAL input |
| 10 | XTN | Output | XTAL output |
| 11, 12 | CLK0 | Input | Differential clock input |
| | nCLK0 | Input | Differential clock input |
| 13, 14 | CLK1 | Input | Differential clock input |
| | nCLK1 | Input | Differential clock input |
| 15 | V _{DD} | Power | Power supply pins for device core |
| 17 | IREF | Input | Reference current |
| 18 | CLK_SEL1 | Input | Input clock source selection |
| 19, 20 | QB2 nQB2 | Output | Bank B differential output pair 5. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 22, 23 | nQB1 QB1 | Output | Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 25 | OPMODEB0 | Input | Bank B output selection pin |
| 26 | OPMODEB1 | Input | Bank B output selection pin |
| 27, 28 | nQB0 QB0 | Output | Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 29, 30 | nQA2 QA2 | Output | Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels. |
| 31 | OPMODEA1 | Input | Bank A output selection pin |
| 32 | OPMODEA0 | Input | Bank A output selection pin |

Function Table

Table 1: Input select function

| CLK_SEL [1] | CLK_SEL [0] | Function |
|-------------|-------------|--------------------------------------|
| 0 | 0 | XTAL is the selected input |
| 0 | 1 | CLK0 is the selected reference input |
| 1 | X | CLK1 is the selected reference input |

Table 2: Output Mode select function

| OPMODEA/B [1] | OPMODEA/B [0] | Output Bank A / Bank B Mode |
|---------------|---------------|-----------------------------|
| 0 | 0 | LVPECL |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | Hi-Z |

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

| | |
|---|------------------|
| Storage temperature..... | -55 to +150°C |
| Supply Voltage to Ground Potential (VDD) | -0.5 to +4.6V |
| Inputs (Referenced to GND) | -0.5 to VDD+0.5V |
| Clock Output (Referenced to GND)..... | -0.5 to VDD+0.5V |
| Soldering Temperature (Max of 10 seconds) | +260°C |
| Latch up | 200mA |
| ESD Protection (Input) | 2000 V min (HBM) |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|------------------|-------------------------------|-----------------------------|-------|------|-------|-------|
| V _{DD} | Core Supply Voltage | | 3.135 | | 3.465 | V |
| | | | 2.375 | | 2.625 | V |
| V _{DDO} | Output Supply Voltage | | 3.135 | | 3.465 | V |
| | | | 2.375 | | 2.625 | V |
| I _{DD} | Core Power Supply Current | | | | 70 | mA |
| I _{DDO} | Output Power Supply Current | All LVPECL outputs unloaded | | | 75 | |
| | | All LVDS outputs loaded | | | 85 | |
| | | All HCSL outputs unloaded | | | 55 | |
| T _A | Ambient Operating Temperature | | -40 | | 85 | °C |

DC Electrical Specifications - Differential Inputs

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|--------------------|------------------------------------|-------------------------|-----------|------|-----------------------|-------|
| I _{IH} | Input High current | Input = V _{DD} | | | 150 | uA |
| I _{IL} | Input Low current | Input = GND | -150 | | | uA |
| C _{IN} | Input capacitance | | | 3 | | PF |
| V _{IH} | Input high voltage | | | | V _{DD} +0.3 | V |
| V _{IL} | Input low voltage | | -0.3 | | | V |
| V _{PK-PK} | Input Differential Amplitude PK-PK | | 0.15 | | 1.3 | V |
| V _{CM} | Common mode input voltage | | GND + 0.5 | | V _{DD} -0.85 | V |

DC Electrical Specifications - LVCMOS Inputs

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------|--------------------|-------------------------|------|------|----------------------|-------|
| I _{IH} | Input High current | Input = V _{DD} | | | 150 | uA |
| I _{IL} | Input Low current | Input = GND | -150 | | | uA |
| V _{IH} | Input high voltage | V _{DD} =3.3V | 2.0 | | V _{DD} +0.3 | V |
| V _{IL} | Input low voltage | V _{DD} =3.3V | -0.3 | | 0.8 | V |
| V _{IH} | Input high voltage | V _{DD} =2.5V | 1.7 | | V _{DD} +0.3 | V |
| V _{IL} | Input low voltage | V _{DD} =2.5V | -0.3 | | 0.7 | V |

DC Electrical Specifications- LVPECL Outputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|-----------------|---------------------|-----------------------|------|------|------|-------|
| V _{OH} | Output High voltage | V _{DD} =3.3V | 2.1 | | 2.6 | V |
| | | V _{DD} =2.5V | 1.3 | | 1.6 | |
| V _{OL} | Output Low voltage | V _{DD} =3.3V | 1.3 | | 1.8 | V |
| | | V _{DD} =2.5V | 0.5 | | 0.8 | |

DC Electrical Specifications- LVDS Outputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|-------------------|--|------------|------|-------|------|-------|
| V _{OH} | Output High voltage | | | 1.433 | | V |
| V _{OL} | Output Low voltage | | | 1.064 | | V |
| V _{ocm} | Output common mode voltage | | | 1.25 | | V |
| DV _{ocm} | Change in V _{ocm} between output states | | | | 55 | mV |
| R _o | Output impedance | | 85 | | 140 | Ω |

DC Electrical Specifications- HCSL Outputs

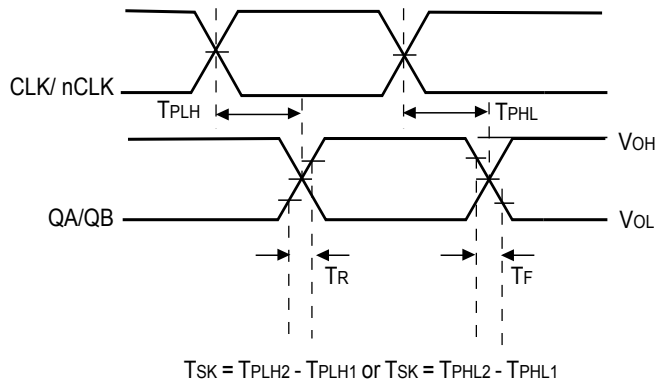
| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|-----------------|---------------------|------------|------|------|------|-------|
| V _{OH} | Output High voltage | | 520 | 800 | | mV |
| V _{OL} | Output Low voltage | | | 0 | 150 | mV |

AC Electrical Specifications – Differential Outputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---------------------|-------------------------------------|--|------|------|------|-------|
| F _{OUT} | Clock output frequency | LVPECL, LVDS | | | 1500 | MHz |
| | | HCSL | | | 250 | |
| T _r | Output rise time | From 20% to 80% | | 150 | | ps |
| T _f | Output fall time | From 80% to 20% | | 150 | | ps |
| T _{ODC} | Output duty cycle | Frequency<650MHz, LVPECL input | 48 | | 52 | % |
| V _{PP} | Output swing Single-ended | LVPECL outputs | 400 | | | mV |
| | | LVDS outputs, <650MHz | 250 | | | |
| | | HCSL outputs | 520 | | | |
| T _j | Buffer additive jitter RMS | | | 0.03 | | ps |
| V _{CROSS} | Absolute crossing voltage | HCSL | 160 | | 460 | mV |
| DV _{CROSS} | Total variation of crossing voltage | HCSL | | | 140 | mV |
| T _{SK} | Output Skew | 6 outputs devices, outputs in same bank, with same load, at DUT. | | 40 | | ps |
| T _{PD} | Propagation Delay | | | 1500 | | ps |
| T _{OD} | Valid to HiZ | | 200 | | | ns |
| T _{OE} | HiZ to valid | | 200 | | | ns |

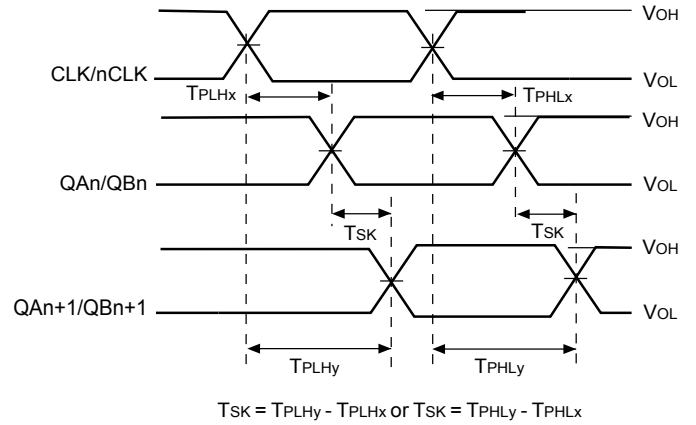
Propagation Delay

Propagation Delay T_{PD}

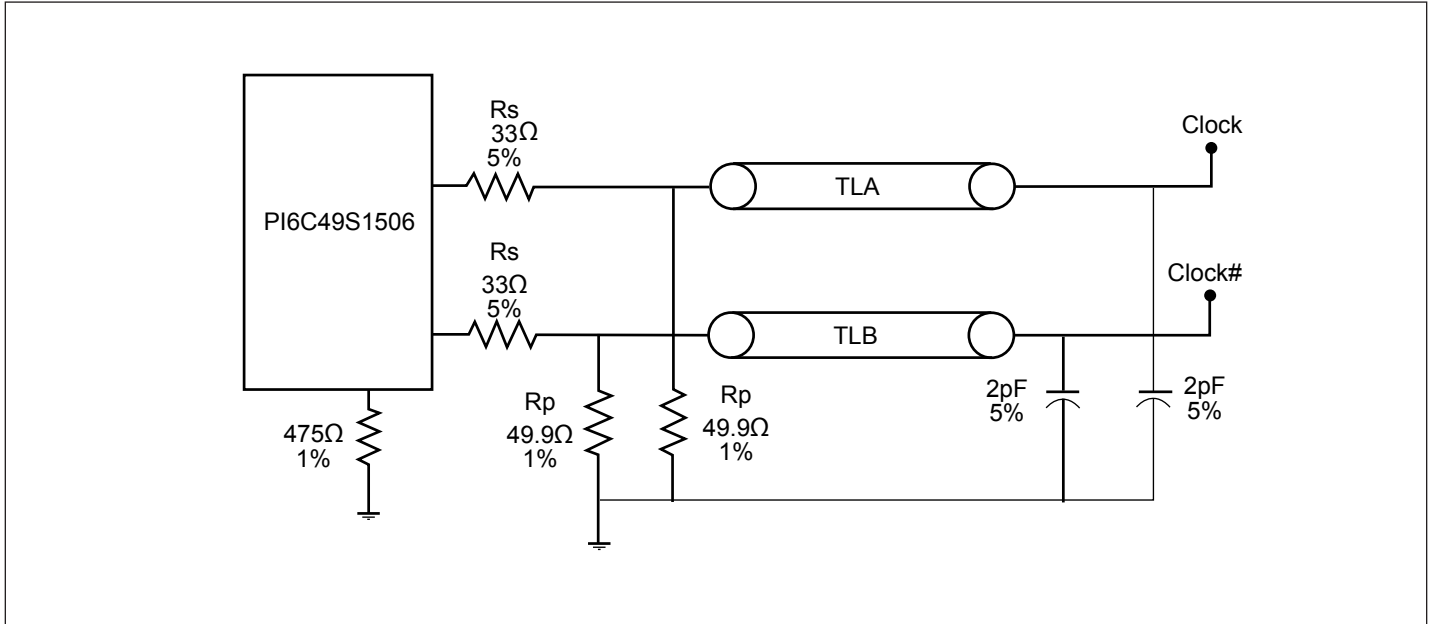


Output Skew

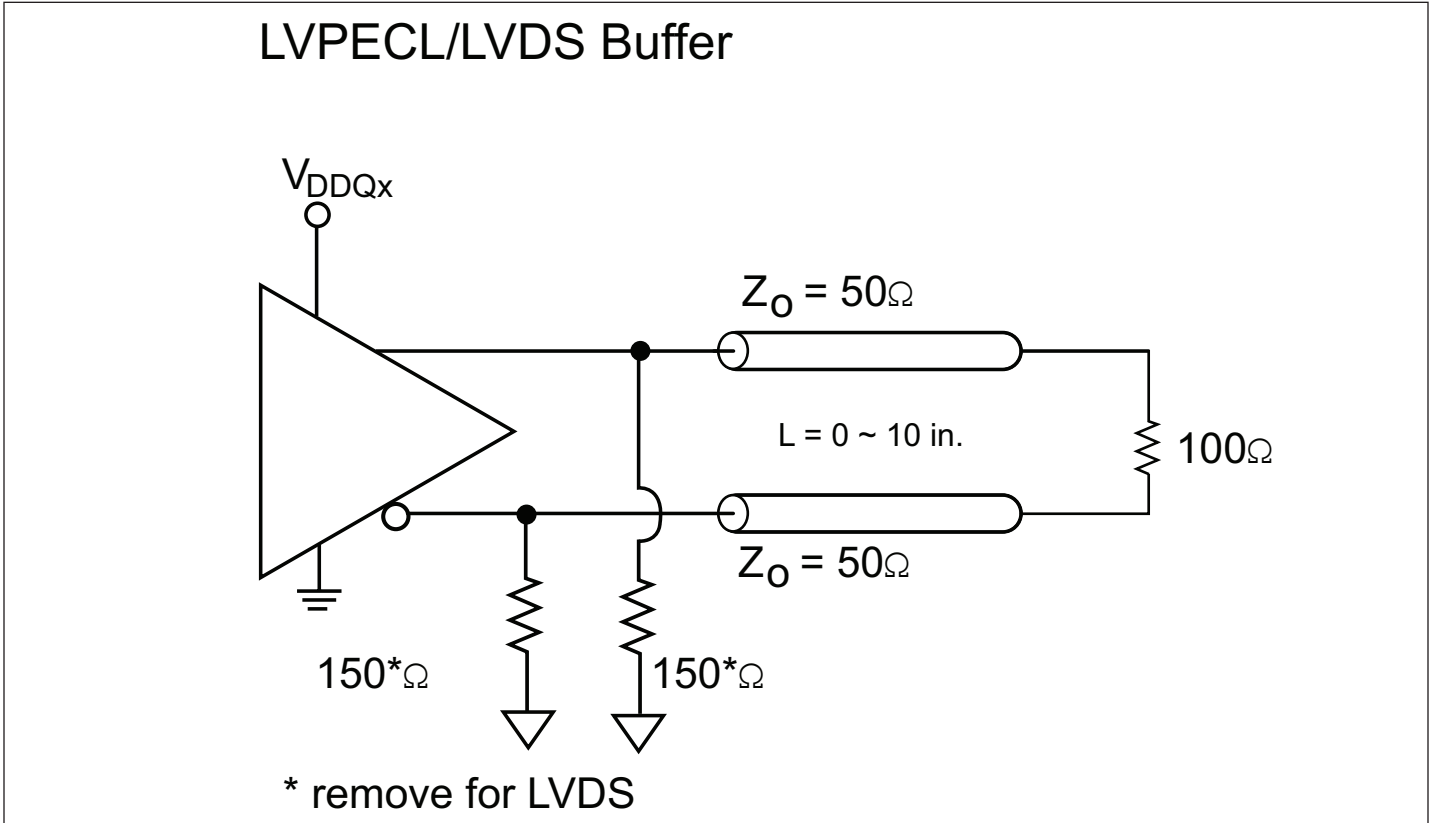
Output Skew T_{SK}



Configuration Test Load Board Termination for HCSL outputs



Configuration Test Load Board Termination for LVPECL/ LVDS



Packaging Mechanical:

DOCUMENT CONTROL NO.
PD - 1814

REVISION: C
DATE: 03/09/05

Notes:

- Controlling dimensions in millimeters
- Ref.: JEDEC MS-026D/ABA
- Package Outline Exclusive of Mold Flash and Metal Burr

Pericom Semiconductor Corporation
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1-800-435-2335 • www.pericom.com

DESCRIPTION: 32-Pin, Thin Quad Flat Package, TQFP

PACKAGE CODE: FA

| Ordering Code | Package Code | Package Type | Operating Temperature |
|-----------------|--------------|------------------------------|-----------------------|
| PI6C49S1506FAIE | FA | Pb-free & Green, 32-pin TQFP | -40 °C to 85 °C |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- “E” denotes Pb-free and Green
- Adding an “X” at the end of the ordering code denotes tape and Reel packaging