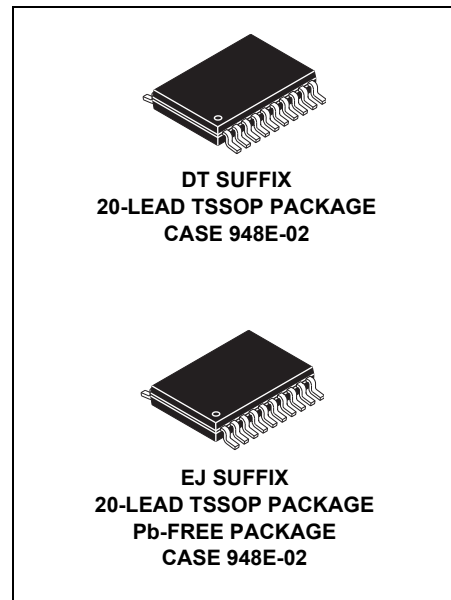


The MC100ES6535 is a low skew, high performance 3.3 V 1-to-4 LVCMOS to LVPECL fanout buffer. The ES6535 has two selectable inputs that allow LVCMOS or LVTTTL input levels which translate to LVPECL outputs. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The ES6535 is ideal for high performance clock distribution applications.

Features

- 4 differential LVPECL outputs
- 2 selectable LVCMOS/LVTTTL inputs
- 1 GHz maximum output frequency
- Translates LVCMOS/LVTTTL levels to LVPECL levels
- 30 ps maximum output skew
- 190 ps part-to-part skew
- 3.3 V operating range
- 20-lead TSSOP package
- Ambient temperature range –40°C to +85°C
- 20-lead Pb-free package available
- **Use replacement part: ICS8535I-01**



ORDERING INFORMATION	
Device	Package
MC100ES6535DT	TSSOP-20
MC100ES6535DTR2	TSSOP-20
MC100ES6535EJ	TSSOP-20 (Pb-Free)
MC100ES6535EJR2	TSSOP-20 (Pb-Free)

Table 1. Pin Description

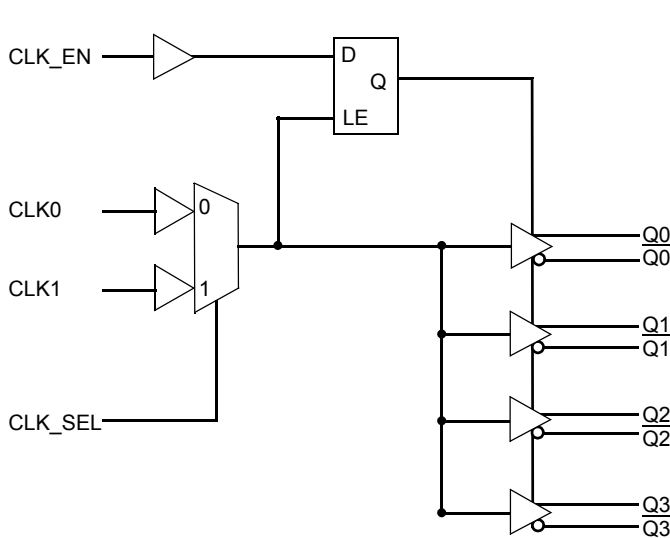
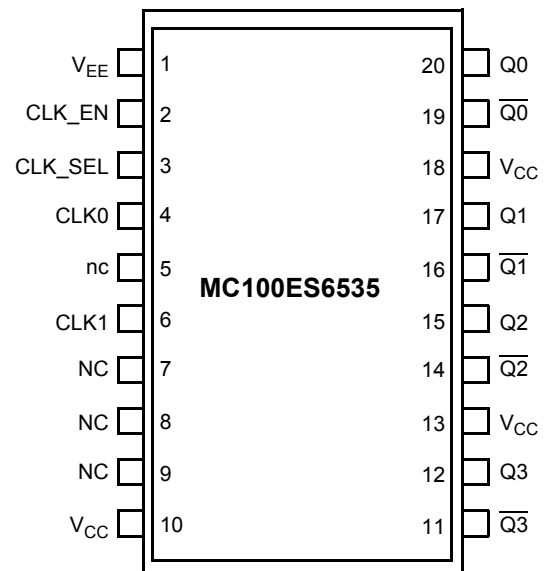
Number	Name	Type		Description
1	V _{EE}	Power		Negative supply pin
2	CLK_EN	Input	Pullup ⁽¹⁾	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, \bar{Q} outputs are forced high. LVCMOS/LVTTL interface levels
3	CLK_SEL	Input	Pulldown ⁽¹⁾	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels
4	CLK0	Input	Pulldown ⁽¹⁾	LVCMOS/LVTTL clock input
6	CLK1	Input	Pulldown ⁽¹⁾	LVCMOS/LVTTL clock input
5, 7, 8, 9	NC	Unused		No connect
10, 13, 18	V _{CC}	Power		Positive supply pin
11, 12	Q3, \bar{Q} ₃	Output		LVPECL differential output pair
14, 15	Q2, \bar{Q} ₂	Output		LVPECL differential output pair
16, 17	Q1, \bar{Q} ₁	Output		LVPECL differential output pair
19, 20	Q0, \bar{Q} ₀	Output		LVPECL differential output pair

1. Pullup and Pulldown refer to internal input resistors.

Table 2. Control Input Function Table⁽¹⁾

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	\bar{Q} 0:Q3
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in .

**Figure 1. Logic Diagram****Figure 2. 20-Lead Pinout (Top View)**

. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	Q0:Q3	Q0:Q3
0	LOW	HIGH
1	HIGH	LOW

Table 3. General Specifications

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	75 k Ω
ESD Protection	Human Body Model Machine Model 4000 V 200 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP 140°C/W 100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	$V_{CC} + 0.3$ $V_{EE} - 0.3$	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{store}	Storage Temperature Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics ($V_{CC} = 3.135$ V to 3.8 V; $V_{EE} = 0$ V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			35			45	mA
$V_{OH}^{(1)}$	Output HIGH Voltage	$V_{CC} - 1150$	$V_{CC} - 1020$	$V_{CC} - 800$	$V_{CC} - 1200$	$V_{CC} - 970$	$V_{CC} - 750$	mV
V_{OL}	Output LOW Voltage	$V_{CC} - 1950$	$V_{CC} - 1620$	$V_{CC} - 1250$	$V_{CC} - 2000$	$V_{CC} - 1680$	$V_{CC} - 1300$	mV

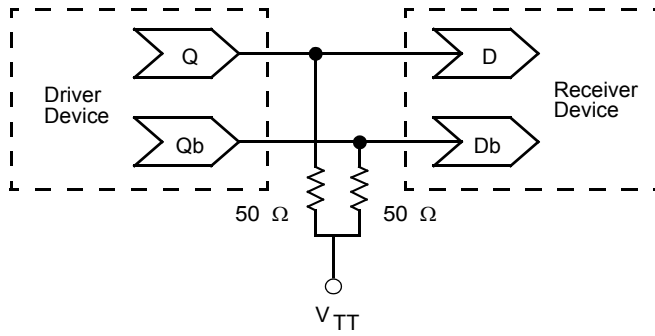
1. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2$ volts.

Table 6. LVTTTL / LVCMOS Input DC Characteristics ($V_{CC} = 3.135$ V to 3.8 V)

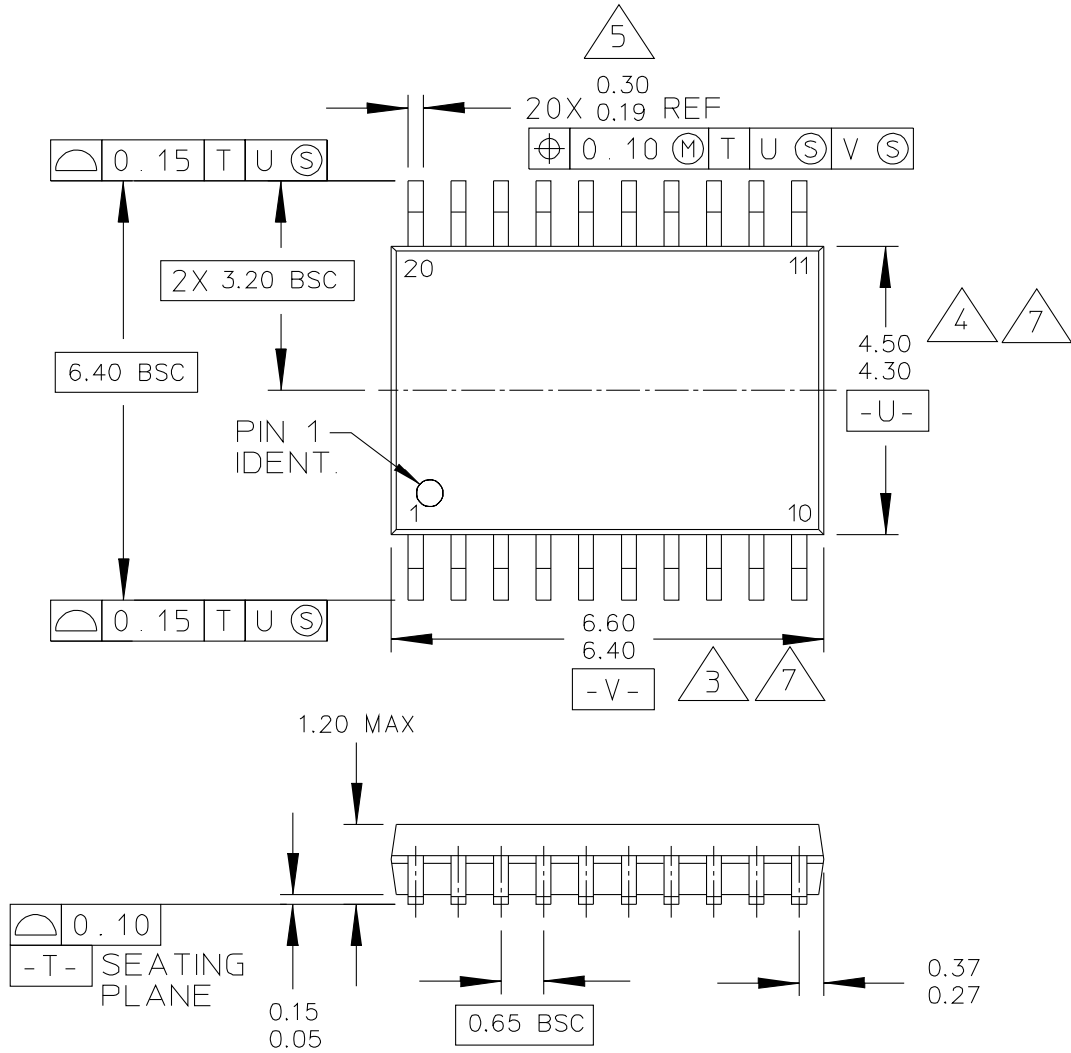
Symbol	Characteristic	Condition	-40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current	$V_{IN} = V_{CC}$			± 150			± 150	μ A
V_{IK}	Input Clamp Voltage	$I_{IN} = -18$ mA			-1.2			-1.2	V
V_{IH}	Input HIGH Voltage		2.0		$V_{CC} + 0.3$	2.0		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage				0.8			0.8	V

Table 7. AC Characteristics ($V_{CC} = 3.135\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			1			1			1	GHz
t_{PD}	Propagation Delay to Output Differential	150	350	500	175	360	550	200	380	600	ps
t_{SKEW}	Skew		20	30		20	30		20	30	ps
	Output-to-Output Part-to-Part			190			190			190	ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{outPP}	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t_r/t_f	Output Rise/Fall Time (20%–80% @ 50 MHz)	50		400	50		400	50		400	ps

**Figure 3. Typical Termination for Output Driver and Device Evaluation**

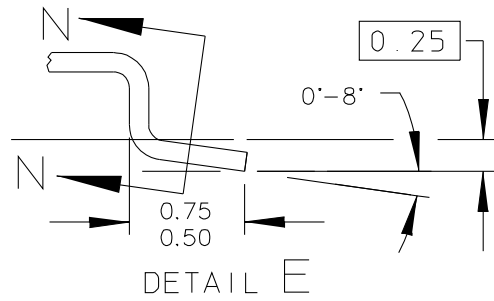
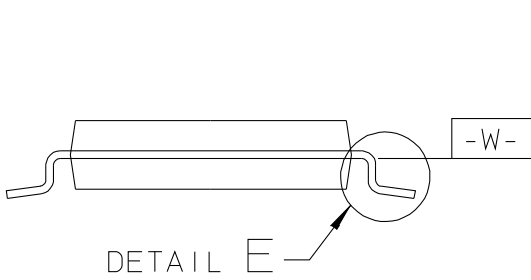
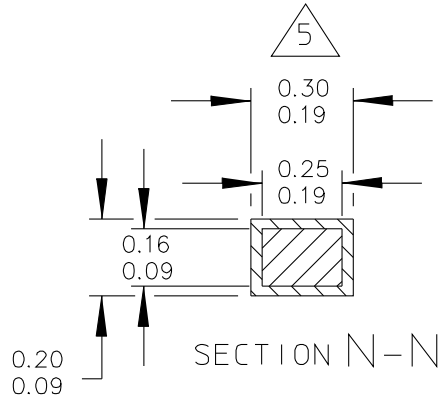
PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A		REV: C
	CASE NUMBER: 948E-02		25 MAY 2005
	STANDARD: JEDEC		

**CASE 948E-02
ISSUE C
20-LEAD TSSOP PACKAGE**

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: C
	CASE NUMBER: 948E-02	25 MAY 2005
	STANDARD: JEDEC	

**CASE 948E-02
ISSUE C
20-LEAD TSSOP PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70169A	REV: C	
	CASE NUMBER: 948E-02	25 MAY 2005	
	STANDARD: JEDEC		

PAGE 3 OF 3

**CASE 948E-02
ISSUE C
20-LEAD TSSOP PACKAGE**

Revision History Sheet

Rev	Table	Page	Description of Change	Date
4		1	Product Discontinuance Notice - Last Time Buy Expires on (11/18/13) Use replacement part: ICS8535I-01	12/14/2012



www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2009. All rights reserved.