

MC74LVXU04

Hex Inverter (Unbuffered)

The MC74LVX04 is an advanced high speed CMOS unbuffered hex inverter. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

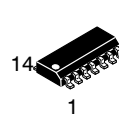
- High Speed: $t_{PD} = 4.1$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.5$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- These Devices are Pb-Free and are RoHS Compliant



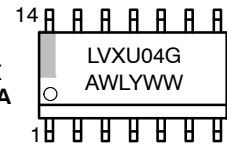
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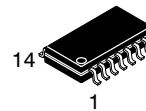
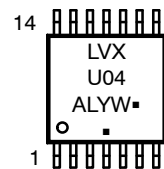
MARKING DIAGRAMS



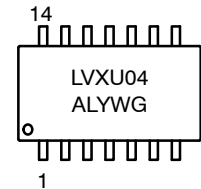
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOEIAJ-14
M SUFFIX
CASE 965



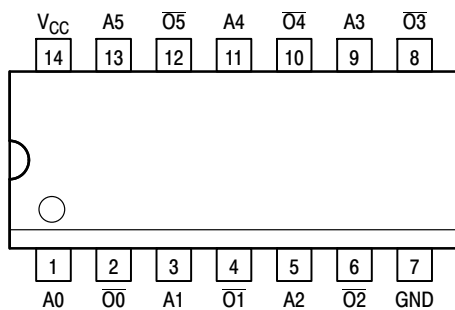
LVXU04 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74LVXU04



14-Lead Pinout (Top View)

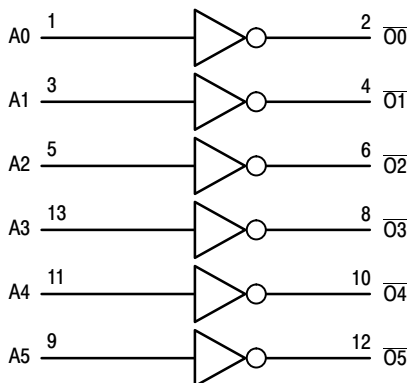


Figure 1. Logic Diagram

PIN NAMES

Pins	Function
A_n	Data Inputs
$\overline{O_n}$	Outputs

FUNCTION TABLE

A_n	$\overline{O_n}$
L	H
H	L

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVXU04DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LVXU04DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LVXU04DTG	TSSOP-14*	96 Units / Rail
MC74LVXU04DTR2G	TSSOP-14*	2500 Tape & Reel
MC74LVXU04MG	SOEIAJ-14 (Pb-Free)	50 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74LVXU04

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _I < GND	-20	mA
I _{OK}	DC Output Diode Current V _O < GND	±20	mA
I _{OUT}	DC Output Sink Current	±25	mA
I _{CC}	DC Supply Current per Supply Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance SOIC TSSOP	250	°C/W
P _D	Power Dissipation in Still Air at 85°C SOIC TSSOP	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% - 35%	UL 94-V0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 2000	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 85°C (Note 4)	±300	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2.0	3.6	V
V _I	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 3.0 V ± 0.3 V	0	100	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

MC74LVXU04

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OH} = -50 μA I _{OH} = -50 μA I _{OH} = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND	3.6			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	3.6			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	V _{CC} = 2.7V C _L = 15 pF C _L = 50 pF V _{CC} = 3.3 ± 0.3V C _L = 15 pF C _L = 50 pF		5.4 7.9	10.1 13.6	1.0 1.0	12.5 16.0	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 6)	V _{CC} = 2.7V C _L = 50 pF V _{CC} = 3.3 ± 0.3V C _L = 50 pF			1.5 1.5		1.5 1.5	ns

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T _A = 25°C			T _A = -40 to 85°C		Unit
		Min	Typ	Max	Min	Max	
C _{in}	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 7)		18				pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/6 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 3.3 V, Measured in SOIC Package)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.5	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.5	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

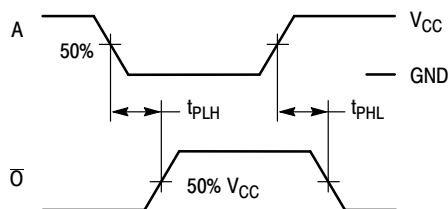
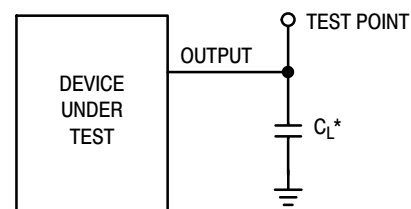


Figure 2. Switching Waveforms



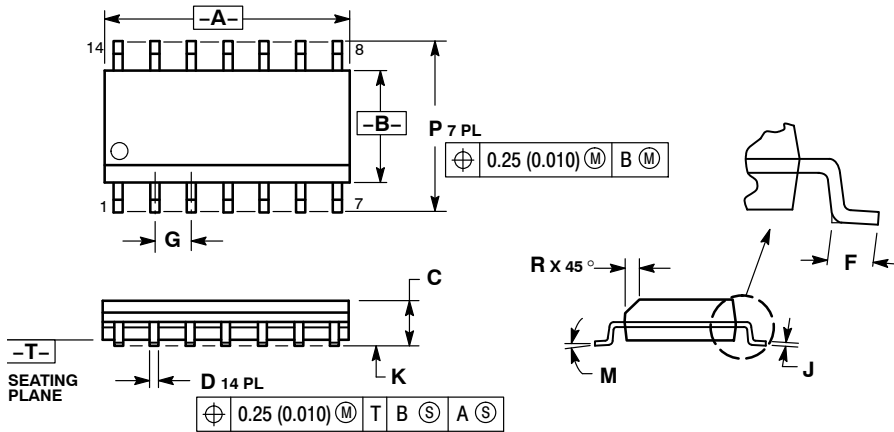
*Includes all probe and jig capacitance

Figure 3. Test Circuit

MC74LVXU04

PACKAGE DIMENSIONS

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE J

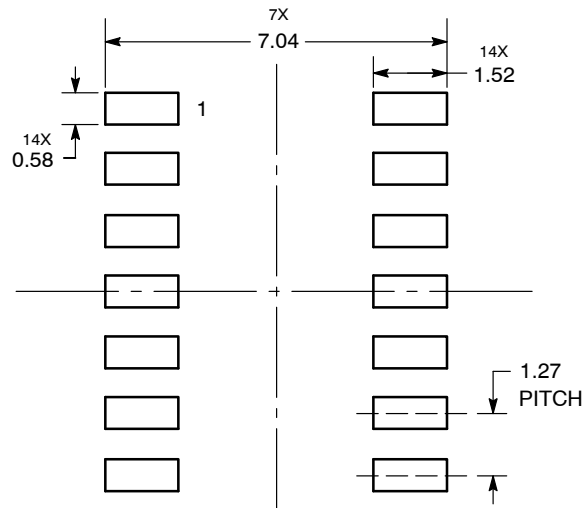


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

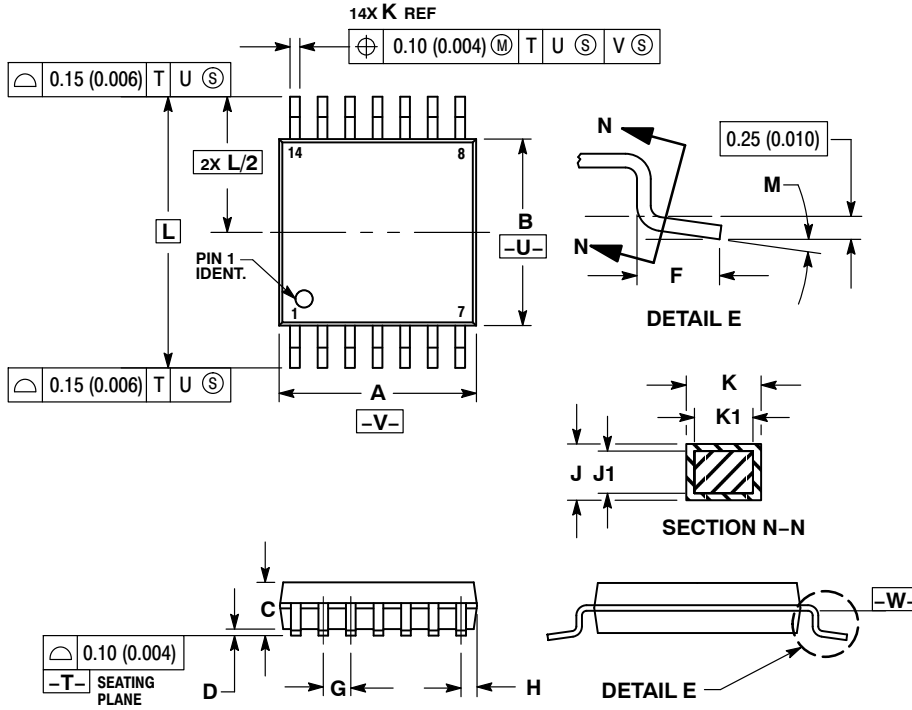


DIMENSIONS: MILLIMETERS

MC74LVXU04

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE B

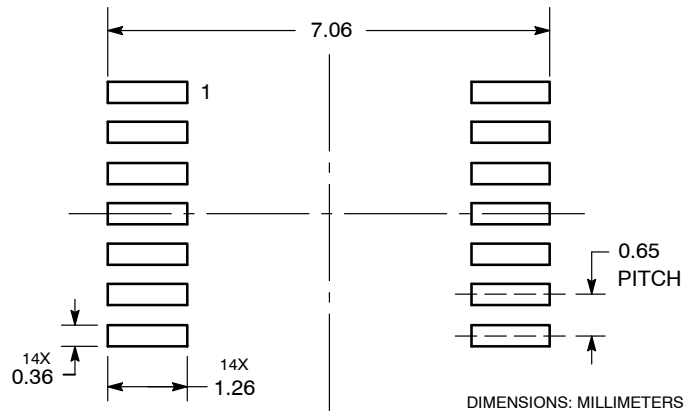


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

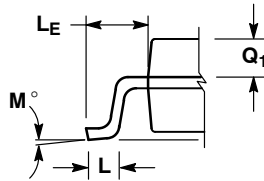
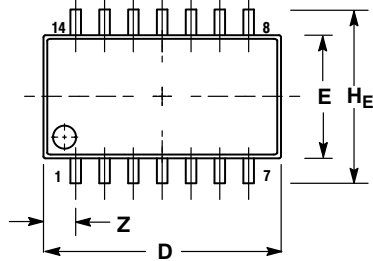
SOLDERING FOOTPRINT



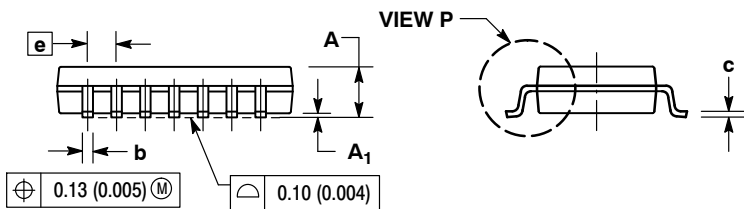
MC74LVXU04

PACKAGE DIMENSIONS

SOEIAJ-14
M SUFFIX
CASE 965-01
ISSUE B



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC 0.050 BSC			
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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