PM7744

Single phase controller with digital interface

VFQFPN16 3 x 3 mm
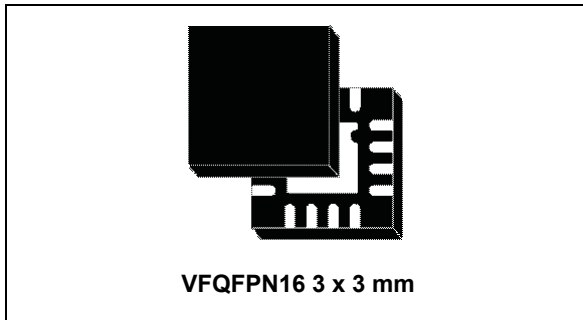
Features

- 3.3 V to 6 V operating supply voltage
- 0.5% internal reference voltage accuracy
- Up to 1 MHz switching frequency
- Remote voltage sense
- Dedicated EN pin
- Power Good output
- VREF input and voltage tracking
- Light-load efficiency optimization
- Output voltage protections
  - Overvoltage
  - Undervoltage
  - Overcurrent
- PMBus compliant serial interface to program controller operating parameter settings and for telemetry
  - Switching frequency
  - Soft-start time
  - Margin mode
  - Output voltage, current and temperature reporting
  - Status register
- Pre-biased output management
- Current monitor input
- Temperature monitor input
- VFQFPN16, 3 x 3 mm package

Applications

- Point of load (PoL) DC-DC conversion
- DC-DC modules

Description

The PM7744 is a single phase step-down controller with complete control logic and protection to realize in a simple way general DC-DC converters by using a compact 3 x 3 mm QFN package.

The PMBus™ interface allows device configuration and output voltage, current and controller temperature monitoring.

The PM7744 device features a dedicated control loop managing high frequency repetitive load transients maintaining the regulation in all operative conditions.

Remote sensing for the regulated voltage allows maintaining 0.5% accuracy on the regulated voltage overload and line variations.

The PM7744 device is available in a VFQFPN16, 3 x 3 mm package.

Table 1. Order codes

Order code	Package	Packing
PM7744TR	VFQFPN16	Tape and reel

Contents

1 Typical application circuit and block diagram

1.1 Application circuit

Figure 1. Typical application circuit
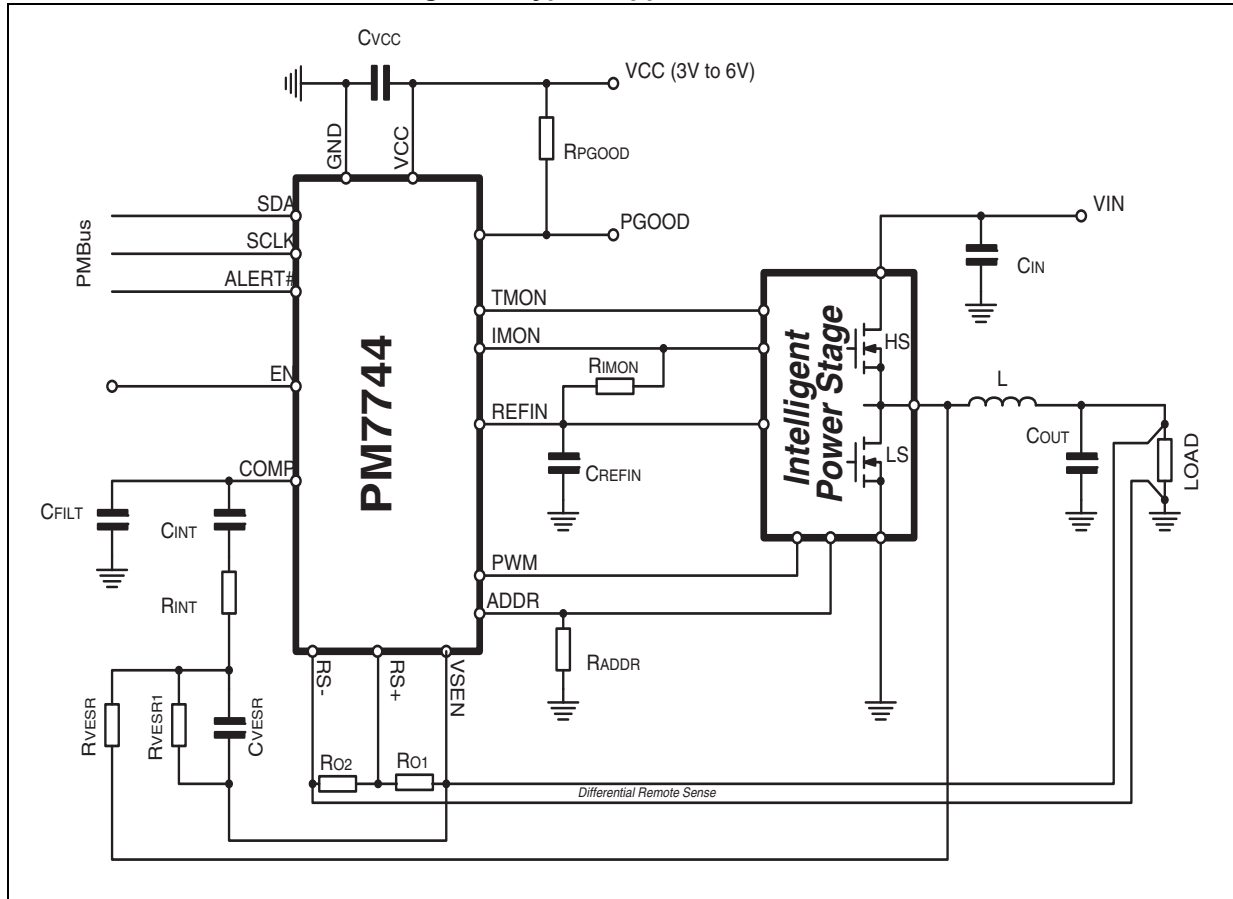
1.2 Block diagram

Figure 2. Block diagram (preliminary)
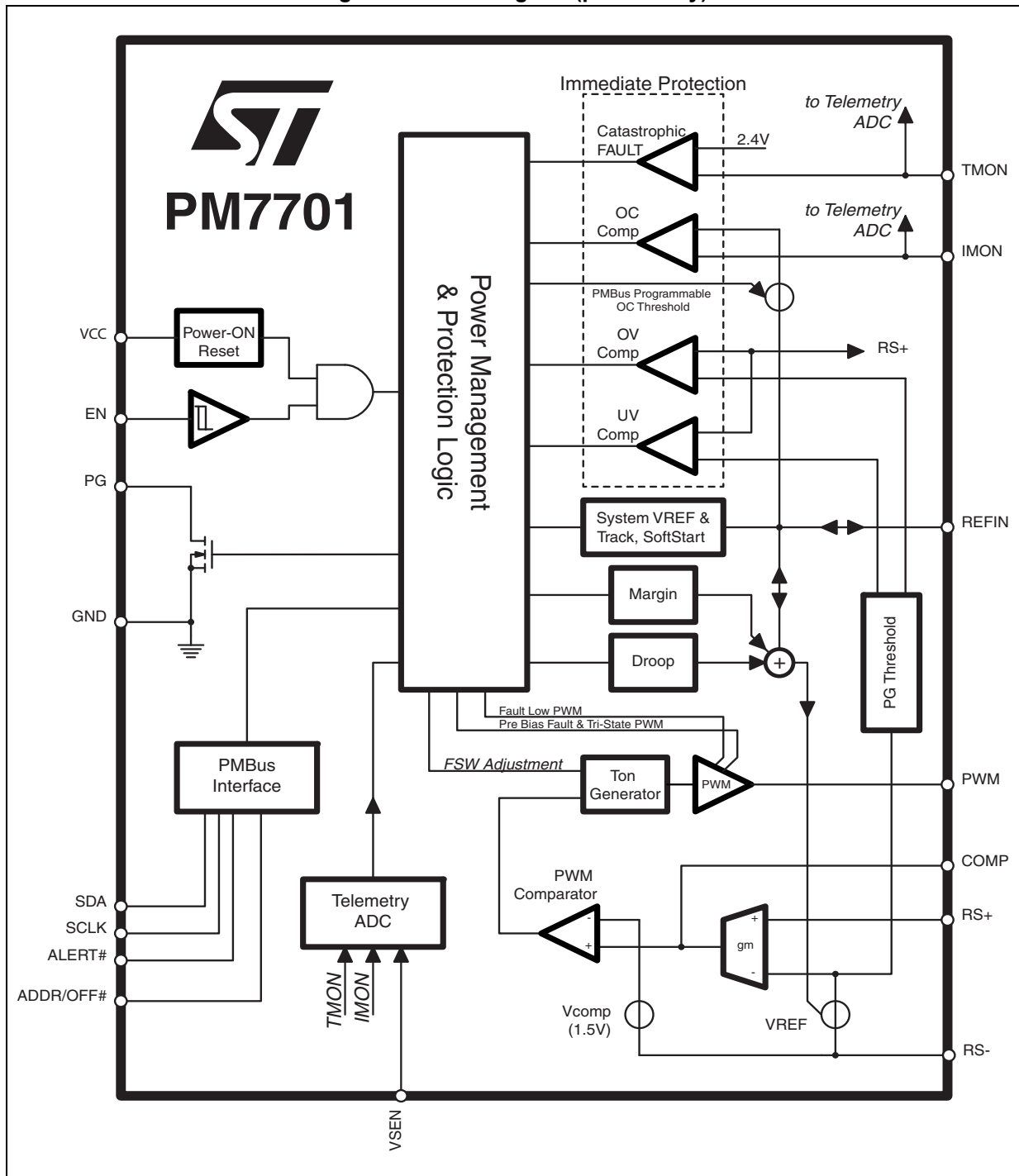
2 Pin description and connection diagrams

Figure 3. Pin connections (top view - preliminary)
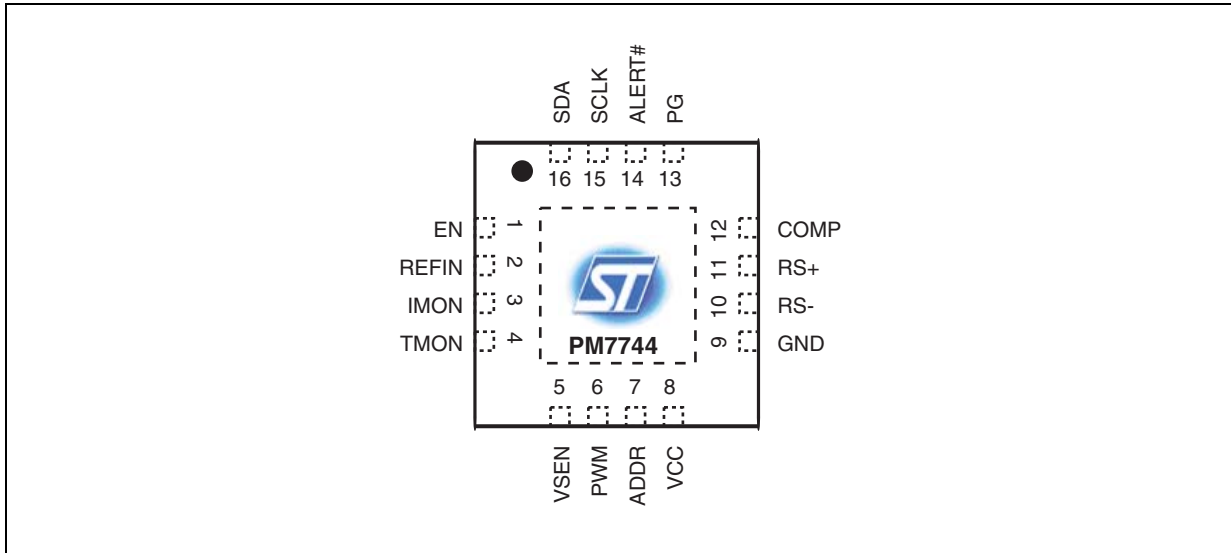
2.1 Pin description

Table 2. Pin description

Pin no.	Name	Description
1	EN	Enable the signal to turn ON/OFF the controller. It is typically connected to VIN through a resistor divider to set the V_{IN_ON} threshold based on the V_{EN_ON} internal threshold. When low, the controller is disabled and PWM is set in HiZ. Even if EN is low, the PMBus is still active. It is recommended to configure the device with EN low.
2	REFIN	REFIN is the reference voltage offset for IMON. A resistor R_{IMON} can be connected between REFIN and IMON pins. The REFIN setting is programmable: by default it is the buffered system VREF but for application requiring external voltage tracking, an external voltage reference greater than the system reference can be applied (must be < 2 V - divide by two option supported). This mode can be programmed via the PMBus using the command MFR_SETTINGS corresponding to DAh, the R/W byte would the code external reference mode. See the PMBus command list for a thorough description of the command.
3	IMON	IMON to REFIN differential voltage is used for load current monitoring and the overcurrent with a conversion ratio k_{IMON} equal to 5 mV/A. A resistor R_{IMON} can be connected between the IMON and REFIN to set a proper gain to current information coming from the power stage. When a negative current is detected, diode emulation is enabled by driving the ADDR/OFF# pin properly. The overcurrent is monitored through IMON-REFIN differential voltage.

Table 2. Pin description (continued)

Pin no.	Name	Description
4	TMON / FAULT	TMON reads a voltage proportional to the power stage temperature with a conversion ratio k_{TMON} equal to 8 mV/°C. It is used for reporting temperature and overtemperature with the adjustable threshold V_{OTH}. Drive the pin to VCC to report an external FAULT condition, the controller will immediately shutdown.
5	VSEN	Directly connect to the regulated voltage V_{OUT}.
6	PWM	Pulse width modulator output. Connect to the external power stage to modulate the duty cycle for the VOUT regulation. It is driven LOW when OV is detected and HiZ to force the power stage to stay OFF.
7	ADDR / OFF#	Sets the I^{2}C address of the device by connecting the proper R_{ADDR} resistor to GND. When the controller detects a negative current through the IMON-REFIN differential information, the pin is driven low to drive HiZ on the power stage properly.
8	VCC	The controller power source. Operating voltages ranging from 3.3 V to 5 V buses. Filter to GND with 1 µF MLCC decoupling.
9	GND	Controller logic and supply ground. Connect solidly to the GND plane on the system board.
10	RSN	Return path for a remote sense. Route differentially with RSP to the point of load system ground.
11	RSP	VOUT remote sense path. Connect through the proper resistor divider to RSN and route differentially with RSN to the point of load regulated voltage. The capacitor C_{INT} is required to be connected to the COMP pin to setup integrator.
12	COMP	Integrator output. Connect through C_{VESR}-C_{INT} to the RSP pin.
13	PG	Open drain Power Good signal. Pulled low when VOUT falls out of regulation limits.
14	ALERT#	I^{2}C ALERT#. Open drain pulled low to indicate that a fault has occurred.
15	SCLK	I^{2}C clock.
16	SDA	I^{2}C data.
-	ePAD	Electrically connected to GND, to be solidly connected with the system board GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction to ambient (device soldered on 2s2p PC board)	45	°C/W
R_{THJC}	Thermal resistance junction to case	1	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-20 to 125	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings[1]

Symbol	Notes	Value	Unit
VCC		-0.3 to 7	V
SCLK, SDA, ALERT#, EN, PG, VSEN		-0.3 to 7	V
ADDR/OFF#, PWM		-0.3 to VCC	V
RSP/FB, RSN, COMP, IMON, TMON, REFIN		-0.3 to 4.6	V

1. All voltages referenced to GND unless otherwise specified.

Table 5. Recommended operative conditions[1]

Symbol	Parameter	Value	Unit
VCC	To GND	3.15 to 6	V
Vout (max)[2]	Programmed through divider	6	V

1. All voltages referenced to GND unless otherwise specified.

2. VOUT_SCALE_MONITOR needs to be properly set so that regulated voltage does not exceed VOUT(max) as stated in *Table 8 on page 21* and *Table 9 on page 26*.

Note: *Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for extended periods of time may impact product reliability and result in device failures.*

3.2 Electrical characteristics

Table 6. Electrical characteristics (V_{CC} = 5 V; T_a = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	EN = HIGH		3.8		mA
		EN = GND		3.2		mA
$UVLO_{VCC,}$	Turn-ON threshold	VCC rising	2.95		3.15	V
	Turn-OFF threshold	VCC falling	2.60		2.85	V
OTA						
g_m				270		μS
f_T	-3 dB bandwidth	[1]		3		MHz

Table 6. Electrical characteristics (V_{CC} = 5 V; T_a = 25 °C unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillator enable and soft-start						
F_{SW}	Main oscillator accuracy	F_{SW} = 800 KHz	-10		+10	%
Tss	Soft-start time accuracy	Slope 200 mV/ms	-15		+15	%
Tssdelay	SS delay 500 μs		450	500	550	μs
EN	Input logic high	EN rising	1.1	1.2	1.3	V
	Input logic low	EN falling	0.9	1	1.1	V
Current sense amplifier						
k_{IMON}	IMON gain			5		mV/A
V_{OCTH}	OC current threshold	IOC = 42 A	189	210	231	mV
PGOOD and protection						
k_{TMON}	TMON gain			8		mV/°C
PGOOD	OVP threshold	RS + rising	0.750	0.790	0.830	V
		Unlatch, RS+ falling		0.3		V
	UVP threshold	RS+ falling	0.551	0.560	0.571	V
		RS+ rising	0.562	0.573	0.584	V
V_{OTH}	Default OTP threshold	TMON rising		1.528		V
	Fault threshold accuracy	± 3 °C	-24		+24	mV
	Warn threshold accuracy	± 3 °C	-24		+24	mV

1. Data guaranteed by design.

4 Device description and operation

The PM7744 is a single phase PWM controller that provides complete control logic and protections to realize a general DC-DC step-down converter. With its high level of integration, this 16-pin device allows a reduction of the cost and size of the power supply solution and also provides real-time Power Good in a compact VFQFPN16 - 3 x 3 mm package.

The PM7744 device is designed to operate from a 3.3 V to 5 V supply. The output voltage can be precisely regulated to as low as 0.6 V with the ± 0.5% accuracy overline and temperature variations. The controller performs remote GND recovery to prevent losses and GND drops to affect the regulation.

The device can be configured through the dedicated PMBus^{TM} interface which allows also to monitor real-time data for the regulated voltage, delivered current and monitored temperature.

The IC can be disabled by pulling the EN pin low.

Configuration data can be stored in the internal NVM avoiding to reconfigure the IC at any power up.

To avoid load damages, the PM7744 device provides overcurrent protection, overvoltage and undervoltage protection. The overcurrent trip threshold is monitored through the I_MON pin. The output voltage is monitored through the dedicated remote sense pins.

The device implements the soft-start by increasing the internal reference in the closed loop regulation managing pre-biased output avoiding high current return through the output inductor and dangerous negative spikes at the load side.

The PM7744 is available in a compact VFQFPN16 - 3 x 3 mm package with an exposed pad.

5 Device configuration

5.1 Address definition

After UVLO, prior to any switching activity, the PM7744 keeps PWM HiZ and decodes the PMBus address according to *Table 7* by sourcing a 5 μA probe current on the ADDR pin. As long as PWM is driven Hi-Z, ADDR/OFF# level does not have an effect on the external power stage behavior.

Table 7. ADDR pinstrapping settings

R_{ADDR} [KΩ]	PMBus slave address
7.5	0x60
30	0x64
59	0x68
91	0x6C
130	0x70
169	0x74
205	0x78
240	0x7C

Caution: Pay attention to an eventual pull-up/pull-down current and/or input impedance of the connected external power stage (See *Figure 1 on page 4*) as it might interfere in the address detection phase.

5.2 External reference operation

The REFIN pin is usually the buffered version of the internal reference used for the regulation. When external reference is set through MFR_SETTINGS command, the REFIN becomes an input (direct or divided by 2). The external reference voltage connected is then used as a reference for the control loop feedback, the soft-start ramp, the margining magnitude, and all the output voltage related thresholds (PG, UV, OV).

When the external reference is selected, the remote ground compensation is disabled. It is assumed that the external reference is referred to the remote feedback.

When the REFIN < 0.4 V (direct) or < 0.8 V (divided by 2), the UV protection is disabled.

After EN = 1, SS is performed anyway, and PG may be asserted at SS end, even if the REFIN = 0.

If EN = 1 and the REFIN is already present SS is performed linearly increasing the internal system reference from 0 V to the connected REFIN.

Caution: Internal or external reference selection have to be performed with EN = 0.

6 Operative settings

6.1 Current reading

The PM7744 reads the information related to the current delivered between IMON and REFIN pins differentially. IMON to REFIN voltage is supposed to be directly proportional to the inductor current with a 5 mV/A ratio. Based on this reference the device performs ZCD, OCP and voltage positioning (load-line). Full scale range for the read information is 60 A or 300 mV. (i.e.: V(IMON-REFIN) = 300 mV).

6.2 Defining load-line (R_{LL})

The load-line resistance R_{LL} is the linear dependence of V_{OUT} on the load current I_{OUT}. It is sometimes requested that V_{OUT} decreases linearly with the increase of the load current. The ratio between decrease in V_{OUT} and increase in I_{OUT} is normally referred as load-line resistance R_{LL}.
The PMBus^{TM} can program up to 8 levels of the droop gain (Kd = 0%, 3.75%, 5.625%, 7.5%, 9.375%, 11.25%, 13.125%, 15%) which express the V_{OUT} total variation at the IMON current reading FSR.

The resulting V_{OUT} variation is then expressed as:

Equation 1

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{o2}}{R_{o1}}\right) \cdot \left(1 - \left(k_D \cdot \frac{I_{OUT}}{FSR}\right)\right)$$

where *FSR* is the IMON full scale range (60 A, i.e.: 300 mV) and R_{o1}, R_{o2} the external resistor divider (See *Figure 1 on page 4*).

The equivalent R_{LL} can be expressed then as:

Equation 2

$$R_{LL} = \left(1 + \frac{R_{o2}}{R_{o1}}\right) \cdot \frac{V_{REF} \cdot k_D}{FSR}$$

6.3 Pulse skipping

The PM7744 performs PSKIP to optimize efficiency in light-load conditions. Zero crossing detection (ZCD) detects when the inductor current is zero by monitoring IMON-to_REFIN voltage. When ZCD is detected, PWM is driven HiZ (or OFF# pin low according to configuration of the device) to keep the power stage in high impedance.

This avoids the inductor current to reverse, increasing the overall system efficiency. The PM7744 features proprietary PSKIP function monitoring voltage level of the COMP pin (as if in continuous current mode, CCM) detecting ZCD and driving HiZ accordingly and managing T_{ON} generation in order to keep a constant ripple level transitioning from CCM to PSKIP and vice-versa.

6.4 Soft-start

The soft-start (SS) is performed on the selected reference after EN and VCC UVLO. During this delay time, COMP pre-charge assures correct startup sequence with any applicative configuration. PWM out is set to HiZ until the RS+ is greater than the internal SS ramp, for pre-biased output start-up without any oscillation or disturbance of the output. At SS end, if the RS+ is greater than the voltage reference, OFF# is deasserted to drive the low-side MOSFET anyway.

UV protection is disabled during the SS.

OT, OV, OC protections are active also during the SS.

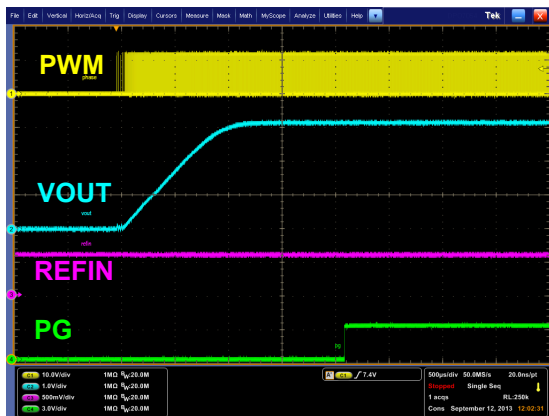**Figure 4. Soft-start using internal reference**
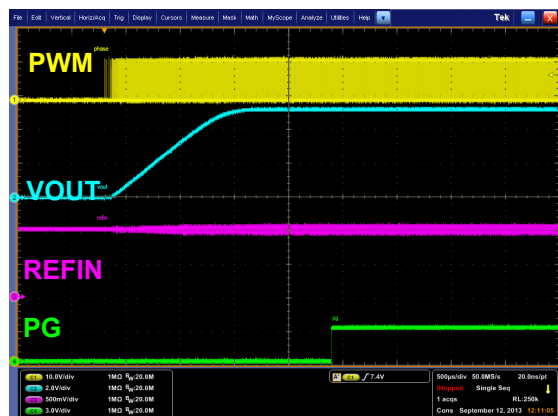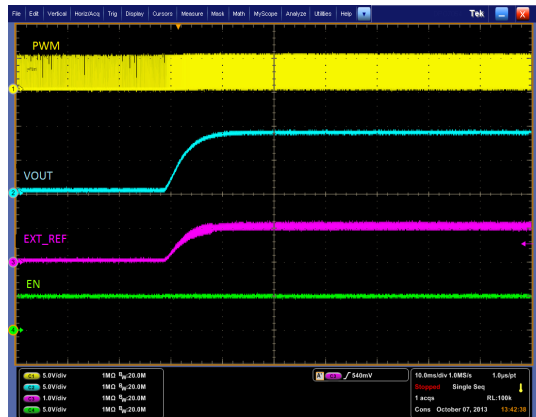

Figure 5. Soft-start with ext. ref. = 1 V

Figure 6. Soft-start with ext. ref. div. 2

Figure 7. Ext. ref. rising after EN

7 Output voltage monitoring and protection

7.1 Overvoltage (OVP)

OVP is operative after UVLO and is always active, even with EN low. It monitors the RS+ pin and triggers when the RS+ is 30% greater than the REFIN. In case the REFIN is below 400 mV, the overvoltage threshold is set to 500 mV fixed.

When OVP triggers, the PM7744 sets PWM = 0, OFF# = 1 in order to turn the LS MOSFET on to protect the load. When the RS+ signal drops below 50% of the REFIN the LS MOSFET is turned off (PWM = HiZ, OFF# = 0). If RS+ voltage returns higher than the OVP threshold, the PM7744 sets back PWM = 0, OFF# = 1 and the process continues. The condition is latched, toggle VCC or EN to restart operations.

When overvoltage protection is triggered, PG is instantaneously forced and kept low and updates STATUS_BYE, STATUS_WORD and STATUS_VOUT accordingly.

7.2 Undervoltage (UVP)

UVP is operative when EN is high. It monitors the RS+ pin and triggers when the RS+ is below 93.5% of the REFIN.

When triggered, the PM7744 continues working and updates STATUS_BYTE, STATUS_WORD and STATUS_VOUT accordingly

When the REFIN < 400 mV, the undervoltage protection is disabled regardless of internal or external reference is used.

7.3 Overcurrent (OCP)

The PM7744 monitors the inductor current through differential information IMON-to-REFIN. IMON-to-REFIN voltage is supposed to be directly proportional to the delivered current with a 5 mV/C ratio. When this information exceeds the OCP threshold V_{OCTH}, the PWM pulse is reset until IMON-to-REFIN falls below V_{OCTH}. V_{OCTH} is programmable by the PMBus^{TM}.

In OC condition, T_{ON} can be delayed by an OC event. After any Ton delayed by OC, an OC warning condition is set in the status register and the ALERT# pin is forced low. After 16 consecutive cycles of Ton generation "delayed" by OC, the PM7744 stops switching. A fault condition is set in the status register. The fault behavior is: PWM = 0, OFF# = 0.

OC is a latched protection; toggle VCC or EN to restart the operation.

7.4 Temperature sense and overtemperature (OTP)

The PM7744 monitors the system temperature through differential information TMON-to-REFIN. TMON-to-REFIN voltage is supposed to be directly proportional to the sensed temperature with a 8 mV/C ratio.

When this information exceeds the OTP threshold V_{OTP}, PWM is set HiZ and OFF# = 0 (latched protection, toggle VCC or EN to the restart operation) and PG is forced low while the OT Fault register is set.

In case V_{TMON} exceeds the warning OTW threshold V_{OTW}, the OT warning status register is set and ALERT# is driven low.

8 Closing the loop

8.1 T_{ON} and switching frequency definition

The PM7744 switching frequency is set by MFR_TSW (D2h) PMBus[TM] command. The device automatically identifies the proper T_{ON} duration in order to maintain the desired output voltage and programmed FSW. T_{ON} can be derived with the following equation:

Equation 3

$$T_{ON} = \frac{(R_{o1} + R_{o2}) \cdot V_{REF}}{R_{o2} \cdot V_{IN} \cdot F_{SW}}$$

Where R_{o1} and R_{o2} compose the external divider (See *Figure 1 on page 4*):

Equation 4

$$V_{OUT} = \frac{V_{REF} \cdot (R_{o1} + R_{o2})}{R_{o2}}$$

The range for resistor values is recommended to be between 10 kΩ and 500 kΩ.

8.2 Compensation network design

The control loop is a voltage mode constant on time control revised with integrator to null the regulation error and to provide a fast AC transient response behavior. In this control scheme, the output of the comparator is used to trigger the T_{ON} generator on the PWM pin. *Figure 8* shows the structure of the control loop in case high ESR capacitors are used, which is the basic operation mode.

Figure 8. Control loop simplified reference schematic
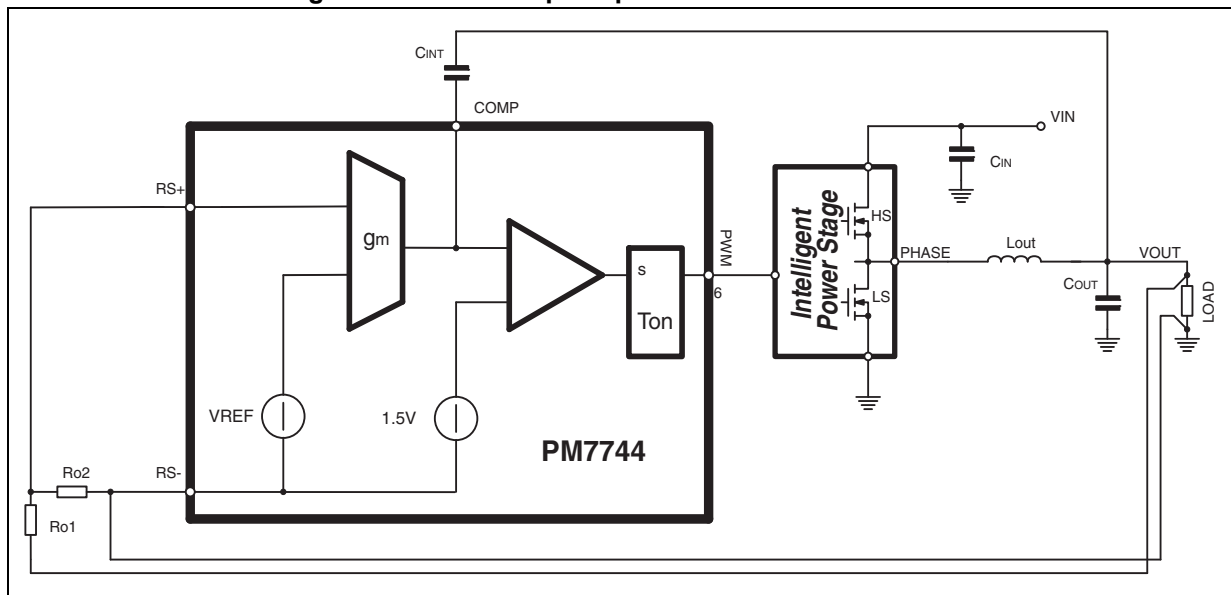
The compensation network is composed by the Gm error amplifier, the capacitor C_{INT} and the resistor R_{o1}, R_{o2}.

The transfer function from the output voltage to the COMP pin can be calculated as:

Equation 5

$$V_{COMP} = V_{OUT} \cdot \left(1 + \frac{1}{s} \cdot \frac{g_m}{C_{INT}} \cdot \frac{R_{o2}}{R_{o2} + R_{o1}} \right)$$

The transfer function is a PI type (proportional/integral) with a zero at frequency f_Z:

Equation 6

$$f_z = \frac{1}{2\pi} \cdot \frac{g_m}{C_{INT}} \cdot \frac{V_{REF}}{V_{OUT}}$$

Basic compensation network where MLCC capacitors are not used in the output filter defines C_{INT} so that f_Z is placed at F_{LC} or lower.

Equation 7

$$C_{INT} = \frac{g_m \cdot V_{REF}}{2\pi f_{LC} \cdot V_{OUT}}$$

In case that the output capacitors are of MLCC type, it is required to add a virtual ESR network (R_{VESR}, C_{VESR}). See *Figure 9* for details.

Figure 9. Control loop with virtual ESR reference schematic
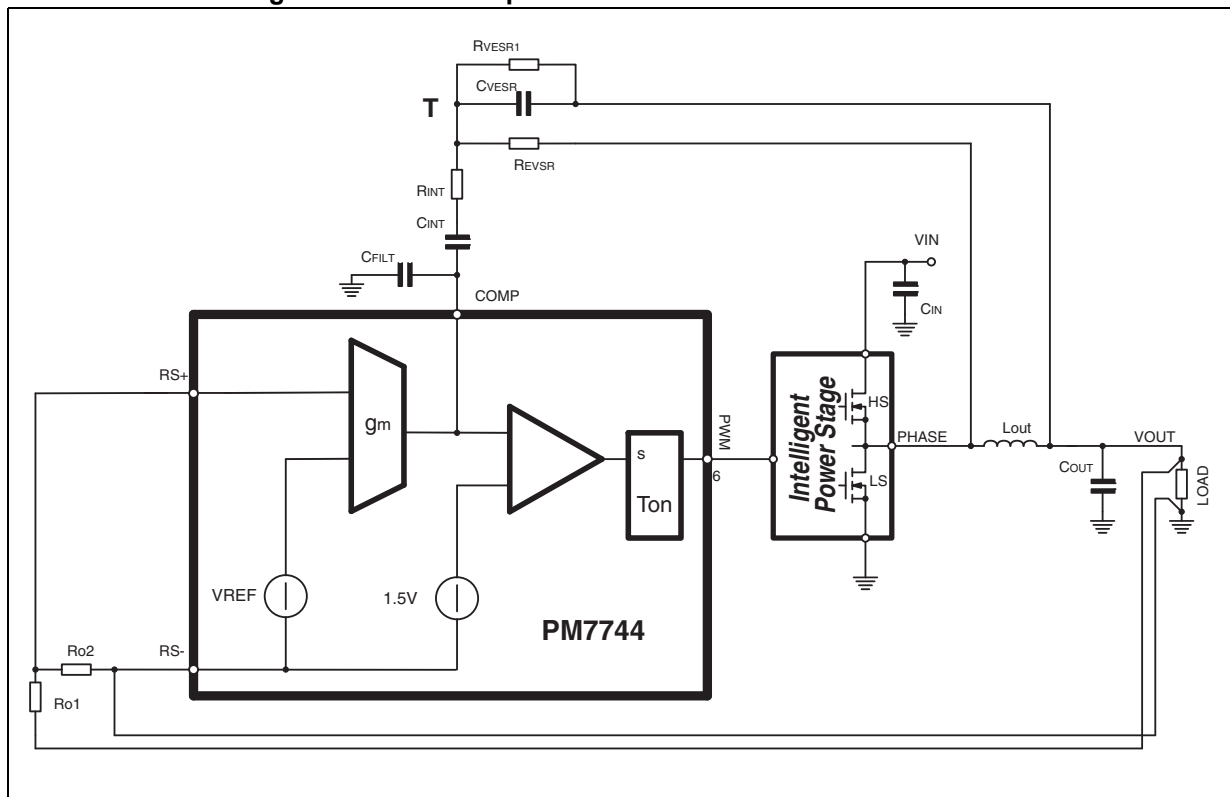
To make the control loop stable, it is important that the ripple fed back to the compensator has the component in phase which is dominant with respect to the in quadrature component. This is achieved by:

Equation 8

$$C_{VESR} = 10 \cdot C_{INT}$$

$$R_{VESR} = \frac{L}{C_{VESR} \cdot R_{CM}}$$

with:

Equation 9

$$R_{CM} = R_{TOT} - ESR$$

where R_{TOT} is to be evaluated as:

Equation 10

$$R_{TOT} = \frac{V_{Tnodepp}}{I_{pp}}$$

where $V_{Tnodepp}$ is the peak-to-peak voltage ripple on steady-state condition at the T node in *Figure 9* and I_{pp} is the peak-to-peak current ripple on the inductor.
The usual working range for $V_{Tnodepp}$ is between 30 mV and 100 mV.
A smaller value of $V_{Tnodepp}$ improves transient response, while a bigger value of $V_{Tnodepp}$ is a condition that ensures the phase component to be prevalent on the quadrature component that means that the system would work in a stable condition.

8.3   Compensation network design example

Considering a typical application where F_{SW} = 1067 KHz, V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 320 nH, C_{OUT} = 5 x 22 μF MLCC (3 mΩ ESR).

The output filter resonance f_{LC} results 26.8 KHz.

Equation 11

$$C_{INT} = \frac{g_m \cdot V_{REF}}{2\pi f_{LC} \cdot V_{OUT}} = 0.34 \, nF$$

Oversizing C_{INT} = 1 nF, makes f_Z to have lower frequency giving evidence of better stability due to a bigger phase margin. As a consequence C_{VESR} would be chosen equal to 10 nF. Considering $V_{Tnodepp}$ = 100 mV, it results:

Equation 12

$$R_{CM} = \left(\frac{V_{Tnodepp}}{I_{pp}} - ESR\right) = \left(\frac{0.1}{9.6} - (0.6 \cdot 10^{-3})\right) = 9.8 \cdot 10^{-3}\Omega$$

then:

Equation 13

$$R_{VESR} = \frac{L}{C_{VESR} \cdot R_{CM}} = 3.3K\Omega$$

R_{VESR1} can then be introduced to have a good transient response and it can be designed according to the following:

Equation 14

$$R_{VESR1} = \frac{R_{VESR}}{\pi \cdot f_{Z1} \cdot C_{VESR} \cdot \left(R_{VESR} - \frac{1}{\pi \cdot f_{Z1} \cdot C_{VESR}}\right)}$$

where:

Equation 15

$$f_{Z1} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot R_{CM}}$$

Finally R_{INT} can be initially set to 0 Ω. For better noise immunity a trial and error procedure can be followed afterwards reaching the best possible configuration of the compensation network. The same for C_{FILT} if needed.

9   PMBus support

The device is compatible with the PMBus[TM] standard revision 1.2, for further information refer to PMBus[TM] standard documentation (www.pmbus.org).

Table 8. Supported commands

Command	Code [Hex]	Mode	Comments
OPERATION	01h	R/W Byte	Turns ON and OFF the unit in conjunction with its ENABLE input signal and also initiates VOUT margining with the values set in VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW.
ON_OFF_CONFIG	02h	R/W Byte	Configures combination of bus commands with ENABLE input to turn ON and OFF the device.
CLEAR_FAULTS	03h	Send Byte	Clears all FAULT bits that have been set in the status registers simultaneously. Clearing fault bits does not allow the unit to restart.
WRITE_PROTECT	10h	R/W Byte	Used to control writing to the PMBus device to provide protection against unintended configuration changes.
STORE_USER_ALL	11h	Send Byte	Instructs the device to copy the configuration registers to NVM.
RESTORE_USER_ALL	12h	Send Byte	Instructs the device to copy the entire contents of NVM to the configuration registers.
CAPABILITY	19h	Read Byte	Provides the host system a way to determine the capabilities of the PMBus device like PEC support, maximum supported speed, etc.
VOUT_SCALE_MONITOR	2Ah	R/W word	Instructs the device on which ratio to apply at the VSEN pin. Data format is linear: – 0xE808; no divider; VOUT(max) = 1 V – 0xE804; divider 1/2; VOUT(max) = 2 V – 0xE802; divider 1/4; VOUT(max) = 4 V – 0xE801; divider 1/8; VOUT(max) = 6 V
VOUT_MODE	20h	Read Byte	Provides the mode of representation of the exponent, and the exponent itself to be used during the READ_VOUT conversion. It may vary according to the programmed value for VOUT_SCALE_MONITOR.
VOUT_OV_FAULT_RESPONSE	41h	R Byte	Reads from the device the action to take in response to an output OV fault (LATCH OFF).
VOUT_UV_FAULT_RESPONSE	45h	R Byte	Read from the device the action to take in response to an output UV fault (CONTINUE).
IOUT_OC_FAULT_LIMIT	46h	R/W word	Sets the output overcurrent fault limit. LSB = 2 A.
IOUT_OC_FAULT_RESPONSE	47h	R Byte	Reads from the device the action to take in response to an output OC fault (LATCH OFF).

Table 8. Supported commands (continued)

Command	Code [Hex]	Mode	Comments
OT_FAULT_LIMIT	4Fh	R/W word	Sets the temperature, in °C, of the unit at which it should indicate an overtemperature fault. LSB = 4 °C.
OT_FAULT_RESPONSE	50h	R Byte	Reads from the device the action to take in response to an overtemperature fault (LATCH OFF).
OW_WARN_LIMIT	51h	R/W word	Sets the temperature, in °C of the unit at which it should indicate an overtemperature warning. LSB = 4 °C.
STATUS_BYTE	78h	R/W Byte	Returns 1 byte where the bit meanings are: Bit<7> BUSY: device busy or unable to respond. Bit<6> OFF: output OFF due to fault or EN Bit<5> VOUT_OV_FAULT: Bit<4> IOUT_OC_FAULT Bit<2> TEMPERATURE: temperature fault or warning Bit<1> CML: communication / memory / logic fault
STATUS_WORD	79h	R/W word	Returns 2 bytes of information where the low Byte is the same as the STATUS_BYTE data. The high Byte bit meanings are: Bit<15> VOUT: output voltage fault or warning has occurred Bit<14> IOUT/POUT: output current fault or warning Bit<12> MFR_SPECIFIC: fault from the power stage Bit<11> POWER_GOOD#: PG signal is deasserted.
STATUS_VOUT	7Ah	Read Byte	Returns 1 data byte with contents as follows: Bit<7> VOUT_OV_FAULT Bit<4> VOUT_UV_FAULT
STATUS_IOUT	7Bh	Read Byte	Returns 1 data byte with contents as follows: Bit<7> IOUT_OC_FAULT
STATUS_TEMPERATURE	7Dh	Read Byte	Returns 1 data byte with contents as follows: Bit<7> OT_FAULT Bit<6> OT_WARNING
STATUS_CML	7Eh	Read Byte	Returns 1 data byte with contents as follows: Bit<7> invalid or unsupported command received Bit<6> host has sent too many bytes Bit<5> packet error check failed Bit<4> memory fault detected Bit<1> other communication fault detected
STATUS MFR_SPECIFIC	80h	Read Byte	Bit<1> reserved Bit<0> TMON fault has been asserted

Table 8. Supported commands (continued)

Command	Code [Hex]	Mode	Comments
READ_VOUT	8Bh	R word	Returns the output voltage in Volts. Linear format. The voltage read between the RS+ and RS- pins is multiplied by the appropriate scaling factor (voltage divider) as defined in MFR_VOUT_SCALE. The exponent for the read-back is found in VOUT_MODE. See *Section 9.2.2*.
READ_IOUT	8Ch	R word	Returns the measured output current in Amperes. Linear format. See *Section 9.2.1*.
READ_TEMPERATURE_1	8Dh	R word	Returns the temperature in °C. Linear format. See *Section 9.2.3*.
PMBUS_REVISION	98h	Read Byte	Returns the revision of the PMBus™ to which the device is compliant.
MFR_ID	99h	Block R	Read the manufacturer's ID.
MFR_MODEL	9Ah	Block R	Read the manufacturer's model or part number.
MFR_REVISION	9Bh	Block R	Read the device and configuration code revisions.
MFR_DATE	9Dh	Block R	Read the date when the device was manufactured.
MFR_SPECIFIC_01 [MFR_SS_TIME]	D1h	R/W Byte	Sets or reads the VOUT rise time. Bits<7:0> unsigned integer N = 0 to 63 with LSB = 200 μs Trise = 200 μs + N * 200 μs 5 V case: dVOUT/Trise ranges from 0.4 V/ms (5 V/12.6 msec, N = 63) to 25 V/ms (5 V/0.2 ms, N = 0) 0.6 V case: dVOUT/Trise ranges from 48 mV/ms to 3 V/ms.
MFR_SPECIFIC_02 [MFR_TSW]	D2h	R/W Byte	Sets or read the device controller switching frequency in KHz. Bits <7:0> 8-bit N (unsigned integer). Accepted range is 6 to 60. Fsw = 9.6 MHz/N so ranges from 160 kHz (N = 60) to 1.6 MHz (N = 6).
MFR_SPECIFIC_06 [MFR_VOUT_MARGIN_HIGH]	D4h	R/W word	Loads the unit with the voltage to which VOUT is to be changed when the OPERATION command is set to "margin high". See *Section 9.1*.
MFR_SPECIFIC_07 [MFR_VOUT_MARGIN_LOW]	D5h	R/W word	Loads the unit with the voltage to which VOUT is to be changed when the OPERATION command is set to "margin low". See *Section 9.1*.

Command	Code [Hex]	Mode	Comments

MFR_SPECIFIC_08 [MFR_SETTINGS]	DAh	R/W Byte	Sets or read the REFIN operation mode, PWM logic state and the pulse skipping mode (PSK).
			– REFIN mode, Bits<4:3>
			  00 - Internal REF (REFIN buffers internal ref.)
			  10 - External REF with internal divide/2 (REFIN = input)
			  11 - External REF with no divider (REFIN = input)
			– PWM logic state, Bits<2:1>
			  01 - HiZ forced by OFF# (low) signal
			  10 - HiZ forced by PWM tristate voltage level
			  11 - HiZ forced either by both OFF# (low) and PWM tristate
			– PSK mode, Bit<0>
			  0 - pulse skipping enabled
			  1 - pulse skipping disabled

IC_DEVICE_REV	AEh	Block R	Read the revision of the device (1 byte).

9.1 Margining

Margining is activated using OPERATION command properly. It can be either positive or negative.

The accepted values for programming MFR_VOUT_MARGIN_HIGH are the integer numbers between 0 and 7. The adjusted Vout results:

Equation 16

$$V_{OUT_h} = V_{OUT_{Nominal}} \cdot (1 + N \cdot 0.005)$$

V_{OUT} will be equal to the nominal value increased by N * 0.5%. The command code is D4h, and it's argument N is a 16-bit integer number in the two's complement.

The accepted values for programming MFR_VOUT_MARGIN_LOW are the integer numbers between 0 and 7. The adjusted Vout results:

Equation 17

$$V_{OUT_l} = V_{OUT_{Nominal}} \cdot (1 - N \cdot 0.005)$$

V_{OUT} will be equal to the nominal value decreased by N * 0.5%. The command code is D5h, and it's argument N is a 16-bit integer number in the two's complement.

9.2 Monitoring

A 8-bit resolution ADC is used to perform monitoring of IMON-to-REFIN, TMON-to-REFIN and VSEN voltages.

9.2.1 Current monitoring

Current monitoring is obtained sensing the voltage difference between the IMON and REFIN, and converting the signal by means of the internal ADC available. The conversion ratio is 5 mV/A. The 0 A value of the inductor current corresponds to a reported difference between the IMON and REFIN of 0 mV, so that, if REFIN voltage is 0.6 V, the IMON will be 0.6 V when I_{OUT} is 0 A.

Through the PMBus command READ_IOUT it is possible to retrieve the current being sensed. The result is a word representing I_{OUT} in the LINEAR DATA format.

X = Y * 2 ^ N (where *N* is a 5-bit two's complement notation of the exponent and *Y* is a 11-bit two's complement notation of the mantissa). N is always -1 so that LSB is 0.5 A.

Figure 10. Representation of the current value in linear data format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

9.2.2 Voltage monitoring

The voltage on VSEN, can be monitored through the usage of 2 PMBus commands: READ_VOUT and VOUT_MODE.

VOUT_MODE (R only) retrieves the exponent to be used in the conversion of the number. This number N is represented on the 5-bit two's complement notation and corresponds to bits [4 … 0] of the VOUT_MODE command (see PMBus Rev 1.2 specification).

READ_VOUT returns the 16-bit two's complement notation number, namely X, which is the mantissa so that:

Equation 18

$$V_{SEN} = X \cdot 2^N$$

Figure 11. Representation of the mantissa of Vout in linear data format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Note: *VOUT_MODE contents change according to VOUT_SCALE_MONITOR value. As a consequence, the maximum VOUT that can be read (EOS) changes accordingly. See Table 9 for details.*

Table 9. VOUT_MODE and VOUT_SCALE_MONITOR

VOUT_SCALE_MONITOR	VOUT_MODE	N for VOUT reading [dec]	End of scale (VOUT)
1	0x18	-8	1
1/2	0x19	-7	2
1/4	0x1A	-6	4
1/8	0x1B	-5	8 (limited by VSEN AMR)

9.2.3 Temperature monitoring

In a similar way as current monitoring, temperature monitoring is achieved through READ_TEMPERATURE_1 command, the result is a couple of bytes where 5 bits represent the two's complement notation of the exponent and the remaining 11 bits are the two's complement notation of the mantissa. The exponent N is fixed and equal to 0, so the LSB will be always 1 °C. The result can be given by:

Equation 19

$$X = Y * 2 ^ N$$

The scale of the conversion is 8 mV/°C ± 2.5%/°C, while the 0 °C temperature is corresponding to a value of 0.6 V as TMON-to-GND voltage.

Figure 12. Representation of the temperature in linear data format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	Y_{10}	Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

9.3 Advanced configuration

9.3.1 Overcurrent fault limit

The overcurrent threshold can be configured with the PMBus command IOUT_OC_FAULT_LIMIT (see PMBus Rev1.2 specification for more details). The value to be written in the register is to be formatted in the linear data format. Stated Y as the value to be written, it is valid the following condition:

Equation 20

$$Y = M \cdot 2^N$$

Where *M* is the mantissa as a signed integer on 11 bits, precisely the bits[10 … 0], while *N* is the exponent as a signed integer and has to be set to 1 so that LSB is set to 2 A. In *Figure 7 on page 14* it is possible to have a view of the representation of the number in the linear data format.

Figure 13. Representation of the current limit in linear data format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	m_{10}	m_9	m_8	m_7	m_6	m_5	m_4	m_3	m_2	m_1	m_0

9.3.2 Overtemperature fault and warn limit

The overtemperature threshold can be configured with the PMBus command OT_FAULT_LIMIT. The value to be written in the register is to be formatted in the linear data format. Stated Y as the value to be written, it is valid the following condition:

Equation 21

$$Y = M \cdot 2^N$$

Where *M* is the mantissa as a signed integer on 11 bits, precisely the bits [10.0], while *N* is the exponent as a signed integer and has to be set to 2 so that LSB is set to 4 °C. The default value for OT_FAULT_LIMIT is 120 °C, while the default value for OT_WARN_LIMIT is 100 °C.

Figure 14. Representation of the temperature fault limit in linear data format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	m_{10}	m_9	m_8	m_7	m_6	m_5	m_4	m_3	m_2	m_1	m_0

9.4 Non-volatile memory (NVM)

The PM7744 has an on-board non-volatile memory that allows storing the actual configuration of the device. Storing/restoring the configuration data to/from the memory is performed by the single standard PMBus[TM] command `STORE/RESTORE_DEFAULT_ALL`. Any unintended writing can be prevented using the write protection capability through WRITE_PROTECT command.
Memory cells are qualified for 1000 read/erase/write cycles.

9.4.1 Default configuration

At device power up, the content of the NVM is read and configures the device accordingly. The PM6744 is programmed in factory with the following default values into NVM. The These default values can be read (written) from (into) the registers through the corresponding PMBus command.

By means of the STORE_USER_ALL PMBus command, it is possible to overwrite NVM default values reported in *Table 10*.

Table 10. Default configuration values of PMBus R/W commands

PMBus command	Command code	Type	Default value	Notes
OPERATION	0x01	R/W Byte	0x80	Operation ON, nominal V_{OUT}
ON_OFF_CONFIG	0x02	R/W Byte	0x14	ON/OFF commanded by EN only
WRITE_PROTECT	0x10	R/W Byte	0x00	Register write enabled
MFR_VOUT_MARGIN_HIGH	0xD4	R/W word	0x0000	Margin high = 0%
MFR_VOUT_MARGIN_LOW	0xD5	R/W word	0x0000	Margin low = 0%
VOUT_SCALE_NMONITOR	0x2A	R/W word	0xE801	VSEN ratio 1/8
IOUT_OC_FAULT_LIMIT	0x46	R/W word	0x0815	42 A
OT_FAULT_LIMIT	0x4F	R/W word	0x101D	116 °C
OT_WARN_LIMIT	0x51	R/W word	0x101A	104 °C
MFR_SS_TIME	0xD1	R/W Byte	0x0E	SS time 3 ms
MFR_TSW	0xD2	R/W Byte	0x0C	F_{SW} = 800 KHz
MFR_SETTINGS	0xDA	R/W Byte	0x05	Use internal reference, HiZ commanded by PWM, PSK disabled.

10 Application information

10.1 Inductor design

The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost and the size. The inductor has to be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ.). The inductance value can be calculated by *Equation 22*:

Equation 22

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{F_{SW} \cdot \Delta I_L \cdot V_{IN}}$$

Where F_{SW} is the switching frequency, V_{IN} is the input voltage and V_{OUT} is the output voltage. *Figure 15* shows the ripple current versus the output voltage for different values of the inductor, with V_{OUT} = 5 V and V_{IN} = 12 V.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamics load change. The response time is the time required by the inductor to change its current from its initial value to its final value. Until the inductor has finished its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well designed, during a load variation the device is able to set the duty cycle very different (0% to 80%) from a steady-state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

Figure 15. Inductor current versus output voltage
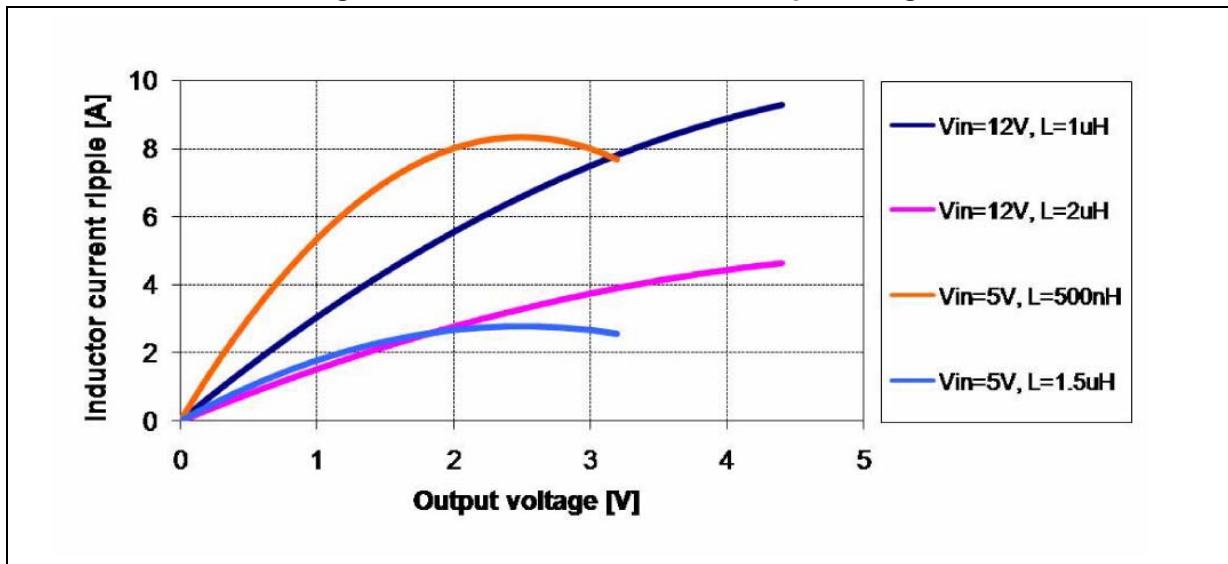
10.2   Output capacitor(s)

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During the steady-state conditions, the output voltage ripple is influenced by both ESR and capacitive value of the output capacitors as follows:

Equation 23

$$\Delta V_{OUTESR} = \Delta I_L \cdot ESR$$

Equation 24

$$\Delta V_{OUTC} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

Where (ΔI_L) is the inductor current ripple. In particular the expression that defines ΔV_{OUT_C} takes into consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitor supplies the current to the load or absorbs the current stored in the inductor until the converter reacts. In facts, even if the controller immediately recognizes the load transient and sets the duty cycle at 80% or 0%, the current slope is limited by the inductor value. The output voltage has a drop that, in this case also, depends on the ESR and capacitive charge/discharge as follows:

Equation 25

$$\Delta V_{OUTESR} = \Delta I_L \cdot ESR$$

Equation 26

$$\Delta V_{OUTC} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

Where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitances that do not minimize the voltage deviation during dynamic load variations. On the contrary electrolytic capacitors have big capacitances to minimize the voltage deviation during load transients, while they do not show the same ESR values of the MLCC resulting then in higher ripple voltages. For these reasons, a mix between electrolytic and MLCC capacitors is suggested to minimize the ripple and reduce the voltage deviation in dynamic mode.

10.3 Input capacitors

The input capacitor bank is designed considering mainly the input RMS current, which depends on the output deliverable current (I_{OUT}) and the duty cycle (D) for the regulation as follows:

Equation 27

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

I_{rms} reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor's ESR and, in the worst case, are:

Equation 28

$$P = ESR \cdot \left(\frac{I_{OUT}}{2}\right)^2$$

11 Evaluation board 3.3 V output

The PM7744 evaluation board is constructed using an eight-layer PCB, and is designed as a step-down DC-DC converter. The board demonstrates the operation of the device in a general purpose application. The input voltage can range from 5 V to 12 V buses and the output voltage is fixed at 3.3 V. The application can deliver an output current up to 20 A. The switching frequency is programmed to be 800 KHz.
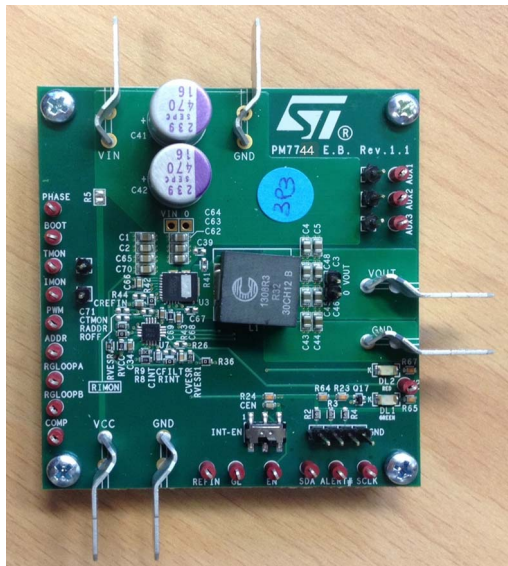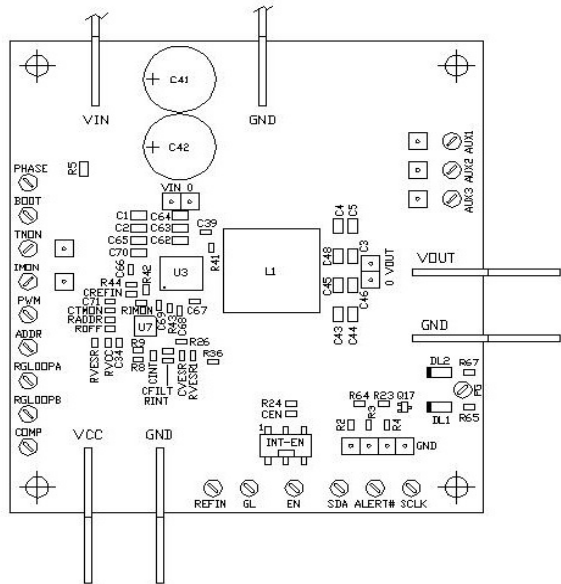

Figure 16. Evaluation board
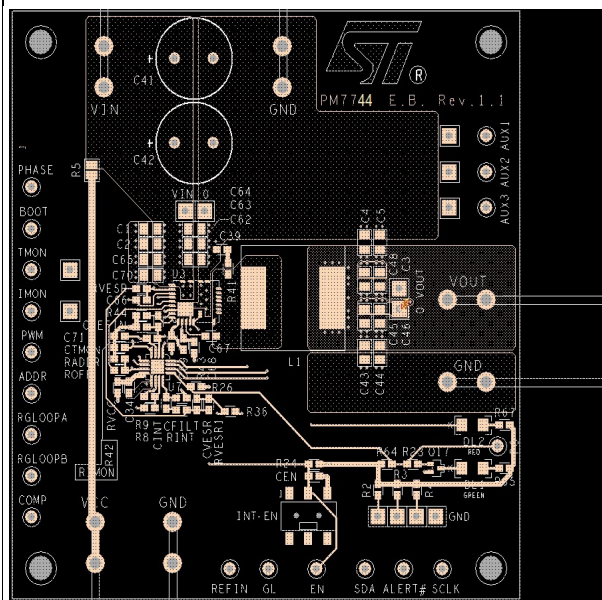

Figure 17. Placement
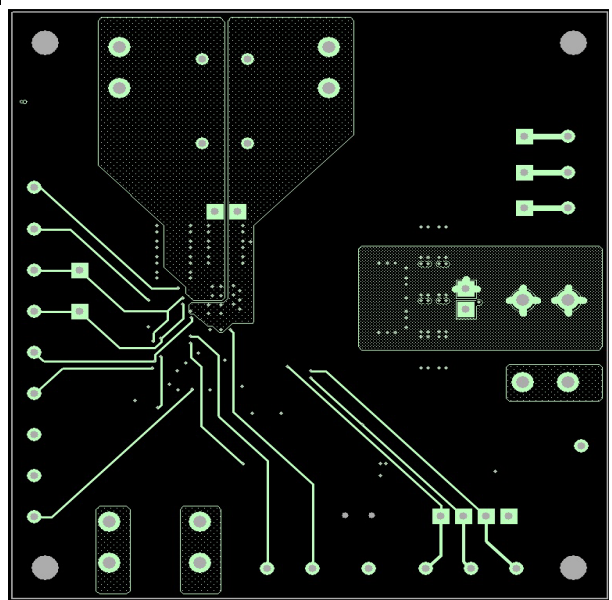

Figure 18. Top layer

Figure 19. Bottom layer

Figure 20. Evaluation board schematic
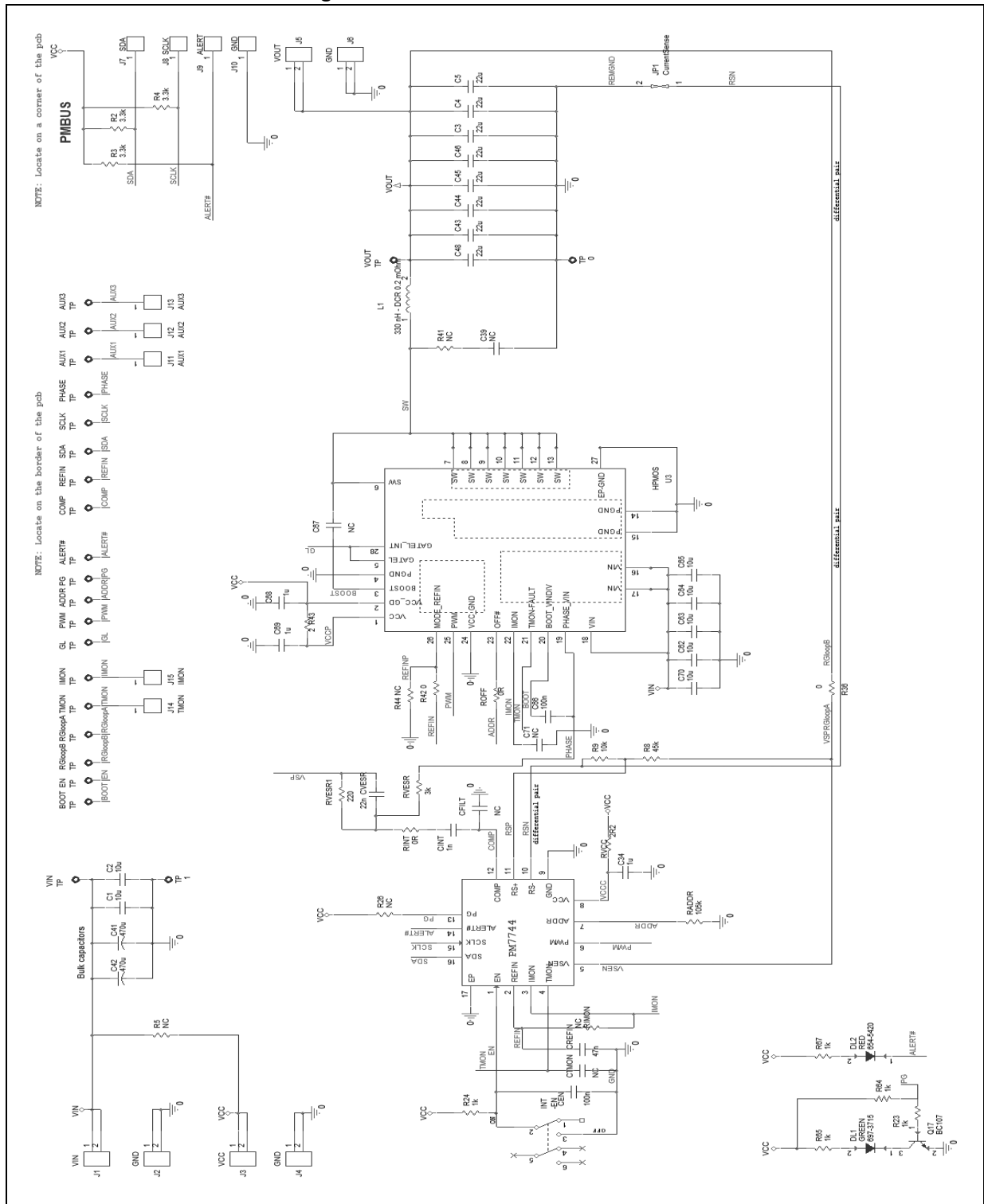
Table 11. Bill of materials (BOM)

Qty.	Reference	Description	Value
19	AUX1, AUX2, AUX3, TMON, SDA, SCLK, RGloopA, RGloopB, REFIN, PWM, PHASE, PG, IMON, GL,EN, COMP, BOOT, ALERT#, ADDR	Test point	
2	CEN,C66	Ceramic capacitors	100 nF, X5R,16 V
5	C39, C67, C71, CTMON, CFILT	Ceramic capacitors	Not mounted
1	CINT	Ceramic capacitor	1 nF, X5R, 6.3 V
1	CREFIN	Ceramic capacitor	47 nF, X5R, 6.3 V
1	CVESR	Ceramic capacitor	22 nF, X5R, 6.3 V
7	C1, C2,C62, C63, C64, C65, C70	Ceramic capacitors	10 μF, X5R,16 V
8	C3, C4, C5, C43, C44, C45, C46, C48	Ceramic capacitors	22 μF, X5R, 6.3 V
3	C34, C68, C69	Ceramic capacitors	1 μF, X5R, 6.3 V
2	C41, C42	Electrolytic capacitors	470 μF, OSCON,16 V
1	DL1	LED	Green
1	DL2	LED	Red
1	INT	Switch	EG1390 - SWITCH
1	J1	Connector	VIN
3	J2, J4, J6	Connector	GND
1	J3	Connector	VCC
1	J5	Connector	VOUT
9	J7, J8, J9, J10, J11, J12, J13, J14, J15	Connector	SDA, SCLK, ALERT#, GND, AUX1, AUX2, AUX3, TMON, IMON
1	L1	Inductor	
1	Q17	NBN BC107 transistor	MVBT3904TT1
1	RADDR	91 kΩ	1% - 0.125 W
4	R26, R41, R44, RIMON	Not mounted	
2	ROFF, RINT, R36, R42	0 Ω	
1	RVCC, R43	2.2 Ω	1% - 0.125 W
1	RVESR	3 kΩ	1% - 0.125 W
1	RVESR1	220 Ω	1% - 0.125 W
3	R2, R3, R4	3.3 kΩ	1% - 0.125 W
1	R5	Not mounted	
1	R8	45 kΩ	1% - 0.125 W
1	R9	10 kΩ	1% - 0.125 W
5	R23, R24, R64, R65, R67	1 kΩ	1% - 0.125 W
1	U7	Controller	PM7744 - STMicroelectronics

Table 11. Bill of materials (BOM) (continued)

Qty.	Reference	Description	Value
1	U3	Power stage	SPS Fairchild
1	PCM PM7744	Printed circuit board	

12 Evaluation board description

12.1 Power input (V$_{IN}$)

This is the input voltage for the power conversion. This voltage can range from 5 V to 12 V.

If this voltage is set to 5 V, it can be also the power for the V$_{CC}$ section. In this case the resistor R5 must be present and set to 0 Ω.

12.2 Output voltage (V$_{OUT}$)

The output voltage is fixed at 3.3 V but can be changed by replacing the resistors R8 and R9 which form the V$_{OUT}$ partition resistors to the 0.6 V voltage reference of the PM7744.

12.3 Input signal (V$_{CC}$)

When using the input voltage V$_{IN}$ to supply the controller, no power is required at this input. However the controller can be supplied separately from the power stage through V$_{CC}$ input (5 V) and, in this case the resistor R5 must be unstuffed.

12.4 Test points

Several test points have been provided for easy access to all the important signals that characterize the device:

- PHASE: the phase node of the inductor
- BOOT: the bootstrap diode anode
- TMON: the power stage temperature sensor output voltage
- IMON: the power stage current sensor output voltage
- PWM: the pulse width modulation driver
- ADDR/OFF#: the pinstrapping signal, and the power stage HiZ driver
- RGLOOPA: the test point for GLoop analysis
- RGLOOPB: the test point for GLoop analysis
- COMP: the error amplifier output
- REFIN: the 0.6 V reference voltage of the controller
- GL: the low-side driver signal
- EN: the signal which enables the controller
- SDA: the data pin of the PMBus
- ALERT#: the alert pin of the PMBus
- SCLK: the clock pin of the PMBus
- PG: the Power Good indicator of the power conversion

12.5 Board characterization

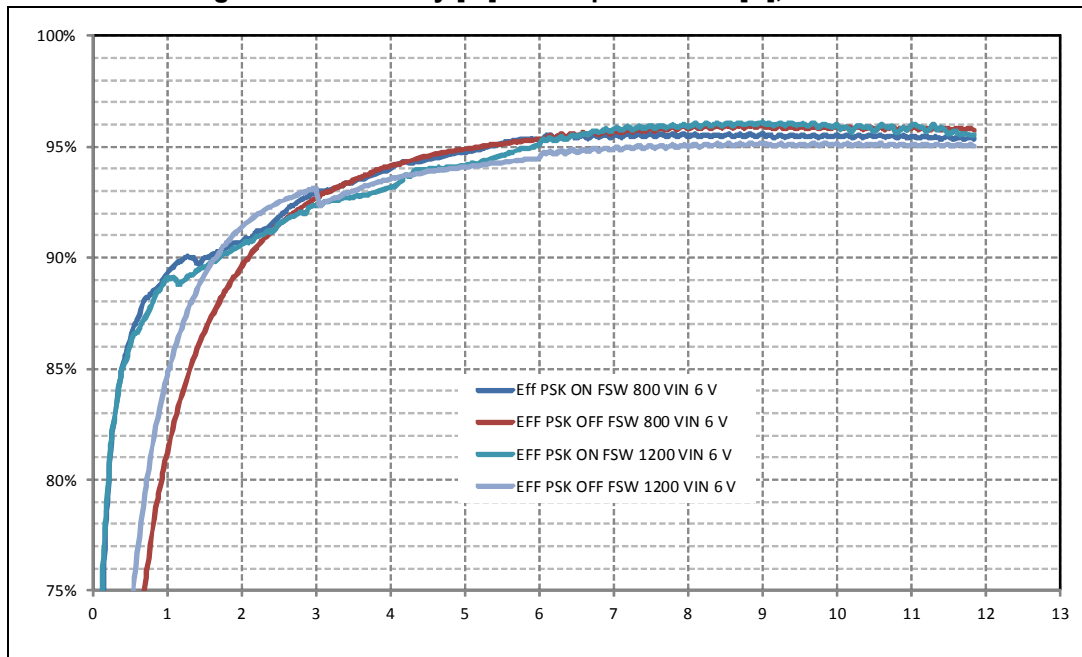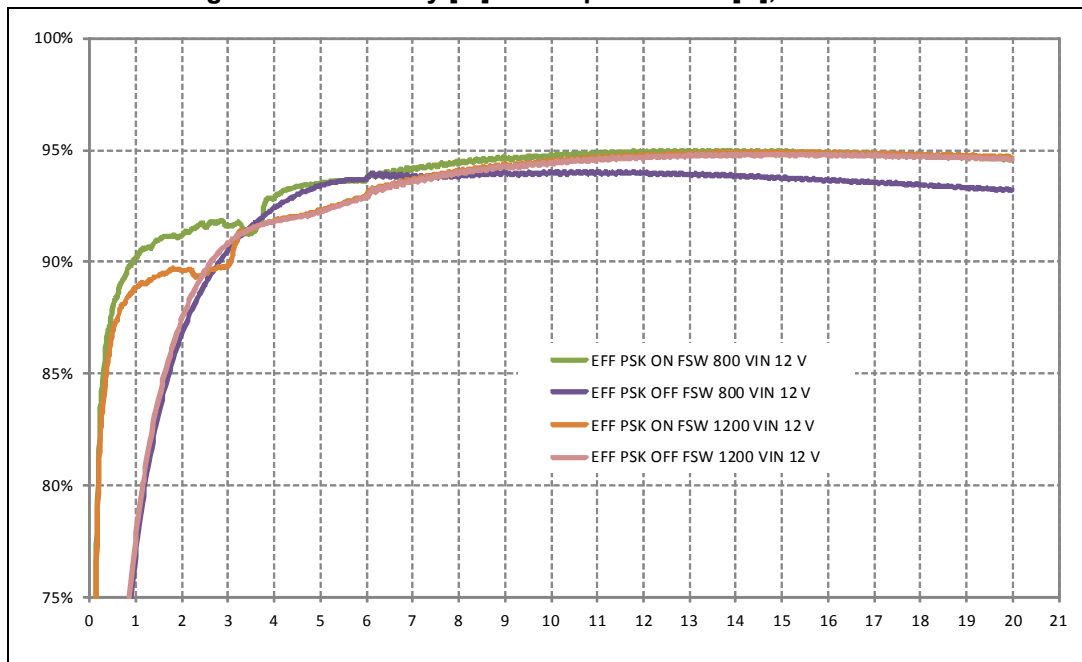**Figure 21. Efficiency [%] vs. output current [A], Vin = 6 V**

Figure 22. Efficiency [%] vs. output current [A], Vin = 12 V

In *Figure 21* and *Figure 22* it is possible to estimate the efficiency of the energy conversion from 6 - 12 V Vin to 3.3 V output either on PSK ON and PSK OFF at the 2 frequency 800 KHz and 1200 KHz.

13   Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

VFQFPN16 - 3 x 3 mm package information
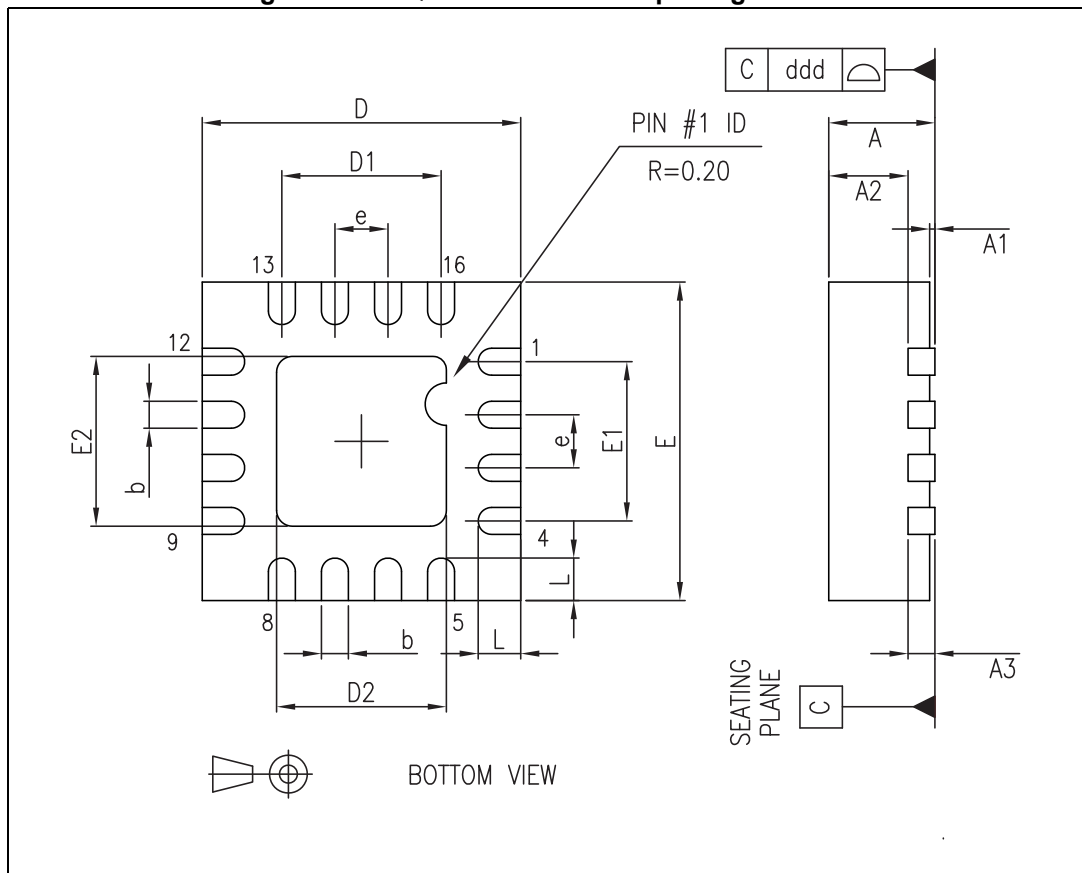
Figure 23. VFQFPN16 - 3 x 3 mm package outline

Table 12. VFQFPN16 - 3 x 3 mm package mechanical data

Symbol	Dimensions (mm)			Dimensions (mils)		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	0.80	0.90	1.00	31.49	35.43	39.37
A1		0.02	0.05		0.78	1.96
A2		0.65	1.00		25.59	39.37
A3		0.20			7.87	
b	0.18	0.25	0.30	7.08	9.84	11.81
D	2.85	3.00	3.15	112.2	118.1	124.0
D1		1.50			59.05	
D2		1.60			62.99	
E	2.85	3.00	3.15	112.2	118.1	124.0
E1		1.50			59.05	
E2		1.60			62.99	
e	0.45	0.50	0.55	17.71	19.68	21.65
L	0.30	0.40	0.50	11.81	15.74	19.68
ddd			0.08		3.15	

14 Revision history

Table 13. Document revision history

Date	Revision	Changes
20-May-2015	1	Initial release.

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