

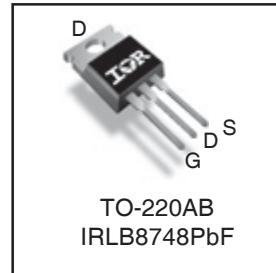
# IRLB8748PbF

HEXFET® Power MOSFET

## Applications

- Optimized for UPS/Inverter Applications
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial use

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>Qg</b>
<b>30V</b>	<b>4.8mΩ</b>	<b>15nC</b>



## Benefits

- Very Low RDS(on) at 4.5V V<sub>GS</sub>
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

	Parameter	Max.	Units
V <sub>DS</sub>	Drain-to-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	92 <sup>ⓐ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	65	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	78	
I <sub>DM</sub>	Pulsed Drain Current <sup>ⓑ</sup>	370	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation <sup>ⓐ</sup>	75	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation <sup>ⓐ</sup>	38	
	Linear Derating Factor	0.5	W/°C
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw <sup>ⓑ</sup>	10 lbf•in (1.1N•m)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case <sup>ⓐ</sup>	—	2.0	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat Greased Surface	0.5	—	
R <sub>θJA</sub>	Junction-to-Ambient <sup>ⓐ</sup>	—	62	

Notes <sup>ⓐ</sup>through <sup>ⓑ</sup> are on page 9

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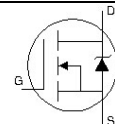
### Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

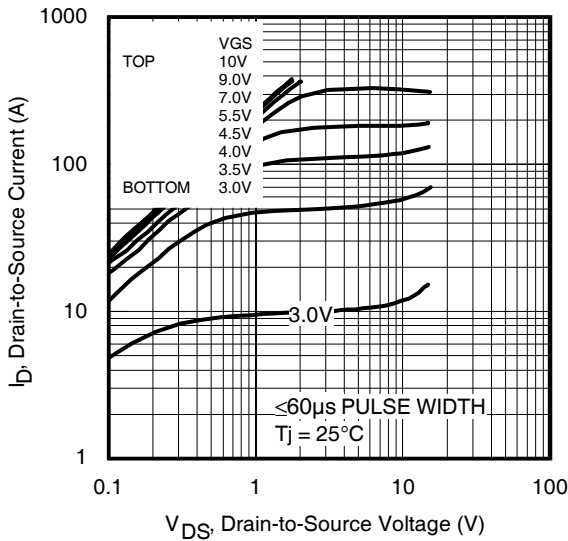
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	21	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	3.8	4.8	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 40A ③
		—	5.5	6.8		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 32A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.8	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-7.1	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	196	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 32A
Q <sub>g</sub>	Total Gate Charge	—	15	23	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 32A
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	3.6	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	2.2	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	5.9	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	3.9	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	8.1	—		
Q <sub>oss</sub>	Output Charge	—	11	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	2.0	3.5	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V ③ I <sub>D</sub> = 32A R <sub>G</sub> = 1.8Ω
t <sub>r</sub>	Rise Time	—	96	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	16	—		
t <sub>f</sub>	Fall Time	—	34	—		
C <sub>iss</sub>	Input Capacitance	—	2139	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	464	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	199	—		

### Avalanche Characteristics

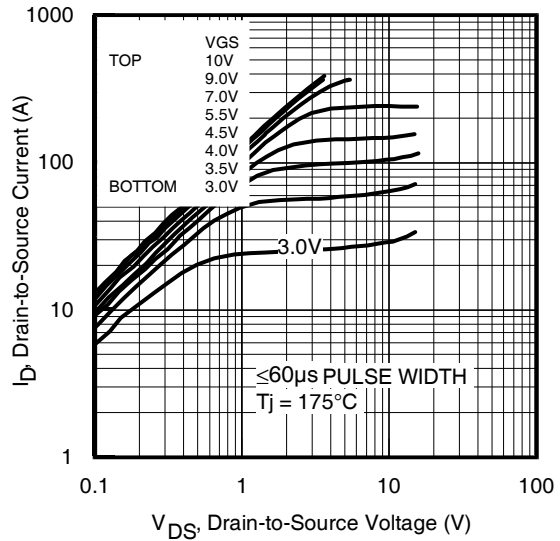
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	114	mJ
I <sub>AR</sub>	Avalanche Current ①	—	32	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	7.5	mJ

### Diode Characteristics

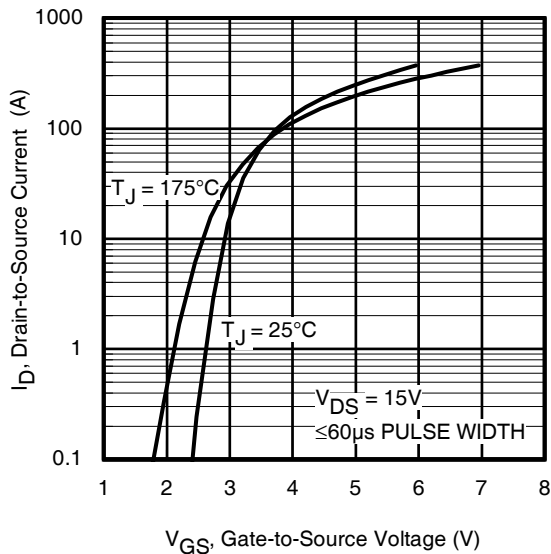
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	92 ④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	370		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 32A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	23	35	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 32A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	39	59	nC	di/dt = 200A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



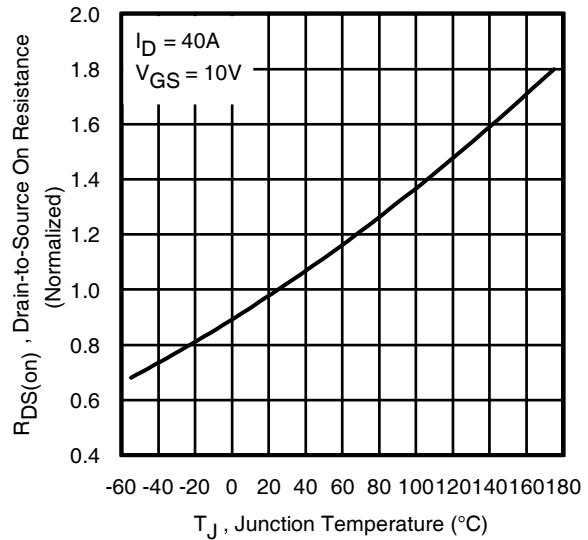
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

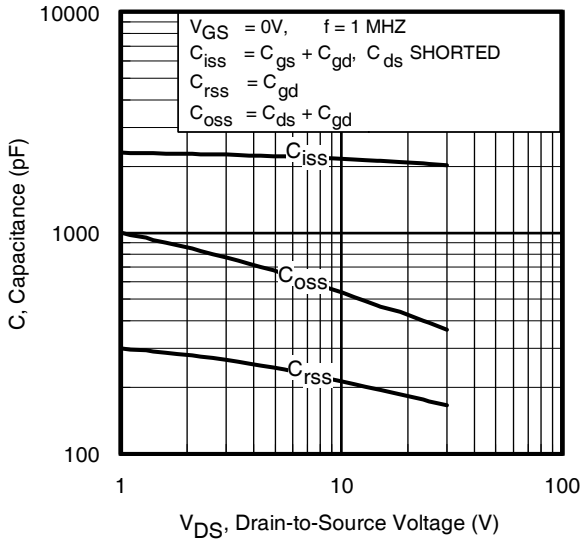


**Fig 3.** Typical Transfer Characteristics

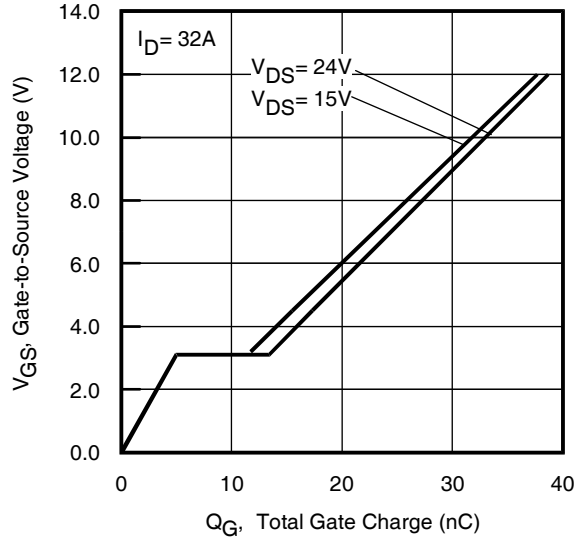


**Fig 4.** Normalized On-Resistance vs. Temperature

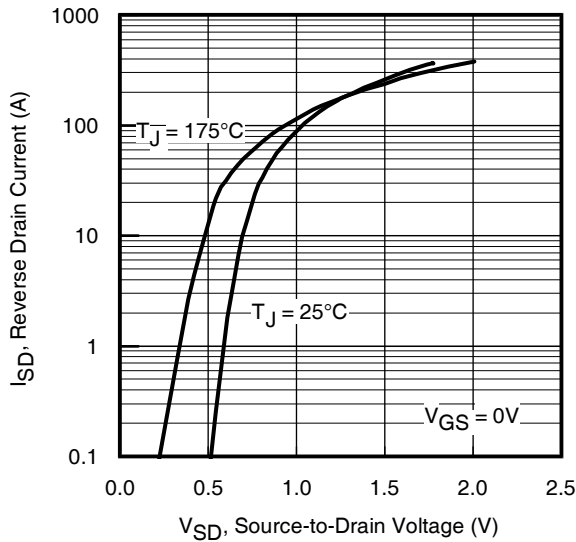
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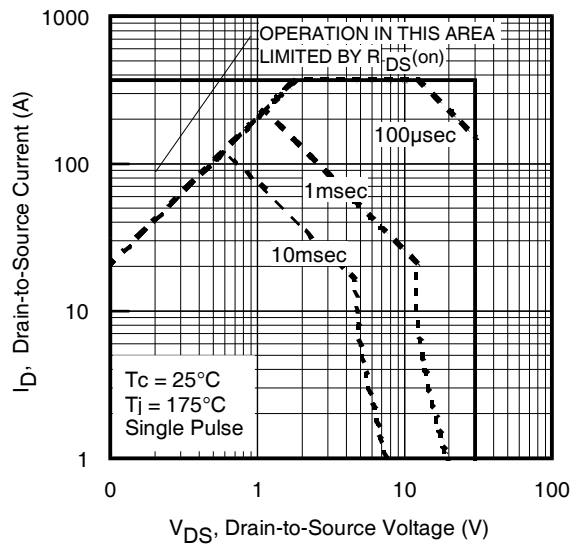
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

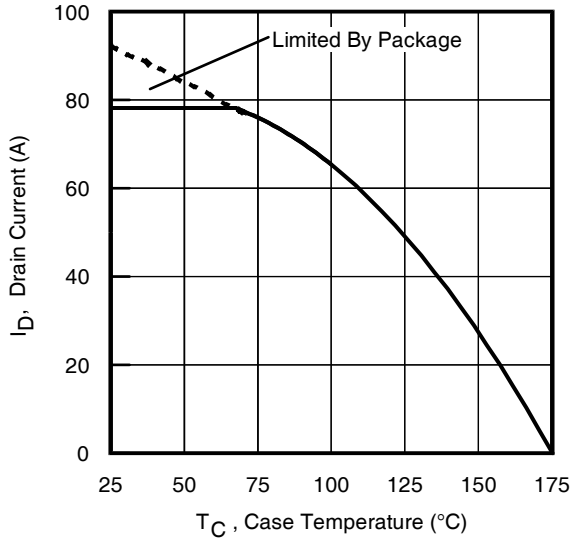


Fig 9. Maximum Drain Current vs. Case Temperature

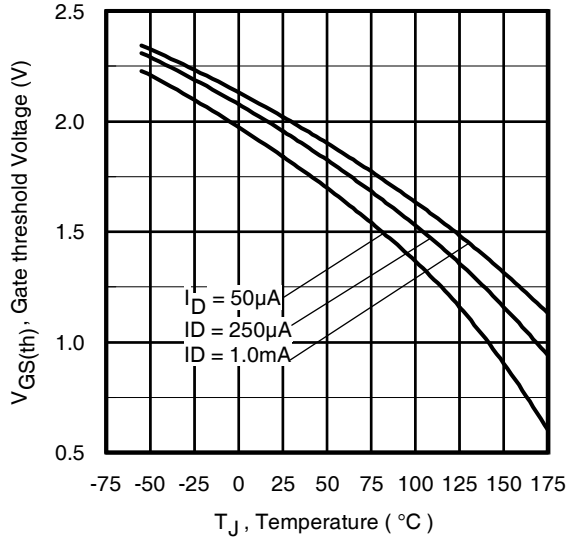


Fig 10. Threshold Voltage vs. Temperature

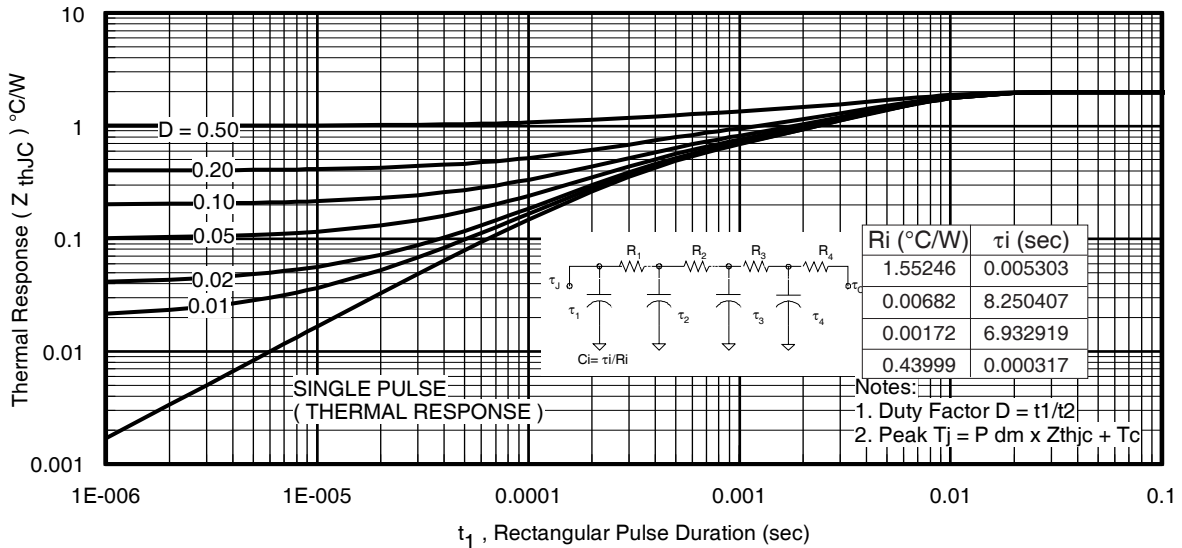
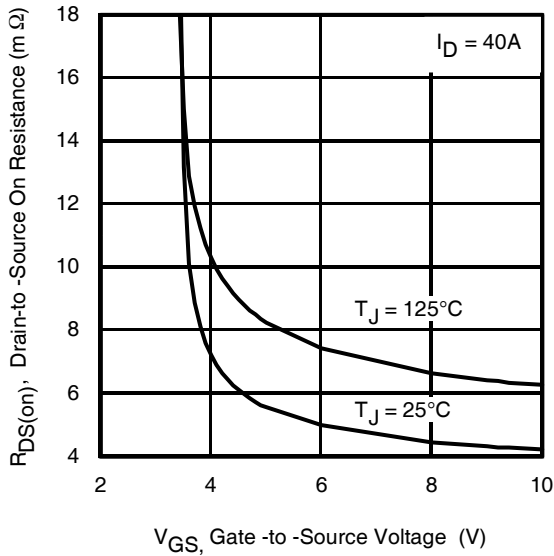
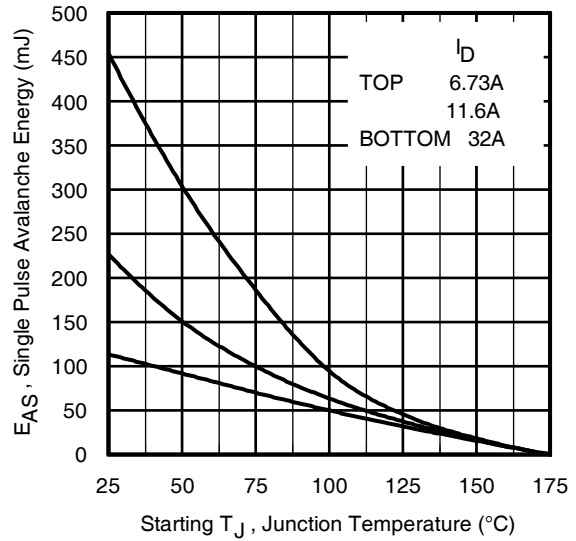


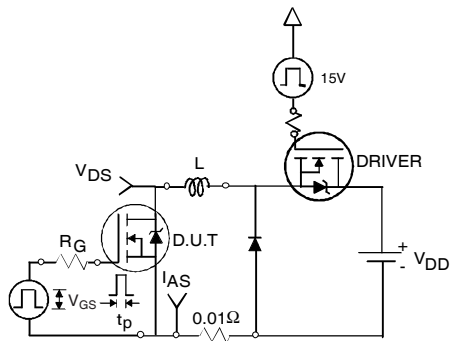
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



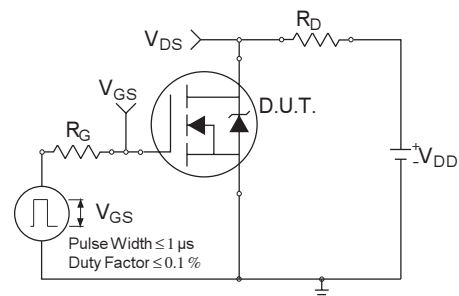
**Fig 12.** On-Resistance vs. Gate Voltage



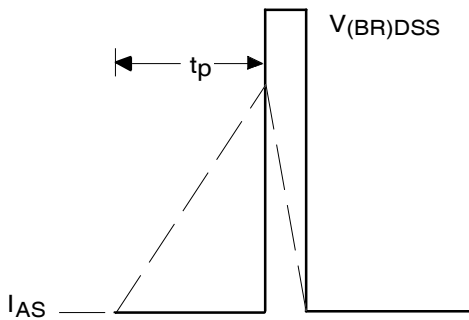
**Fig 13c.** Maximum Avalanche Energy vs. Drain Current



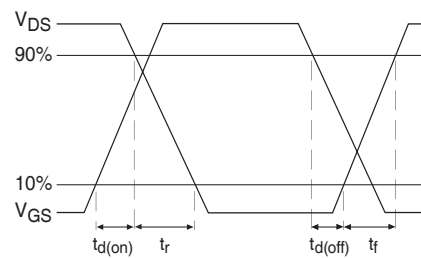
**Fig 13a.** Unclamped Inductive Test Circuit



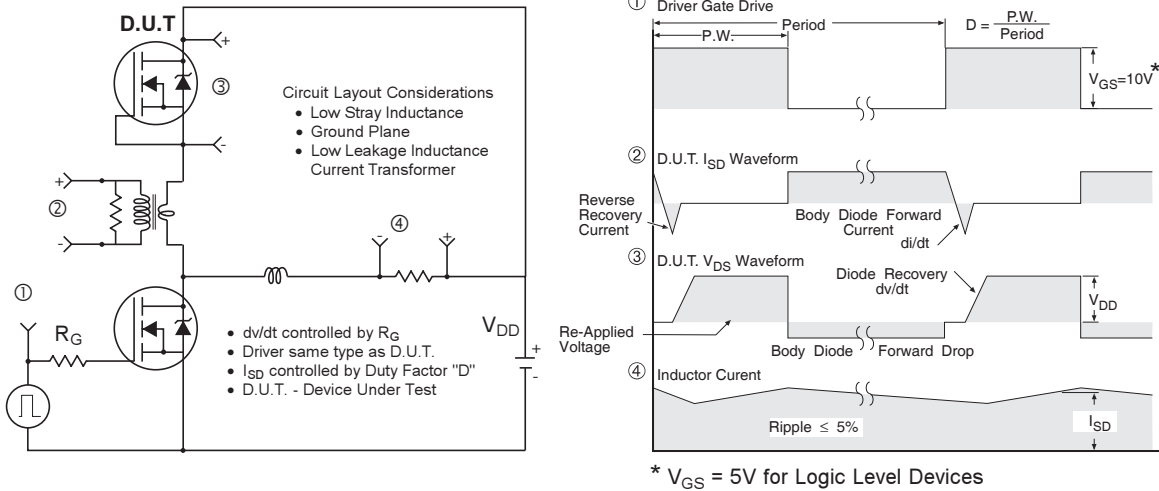
**Fig 14a.** Switching Time Test Circuit



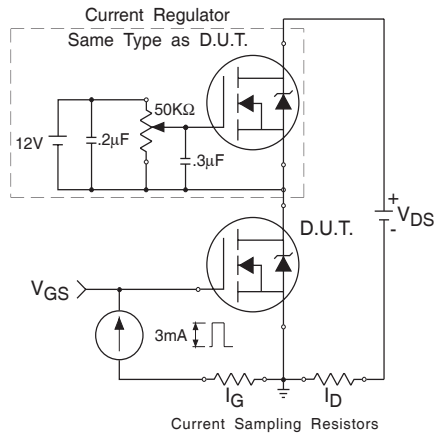
**Fig 13b.** Unclamped Inductive Waveforms



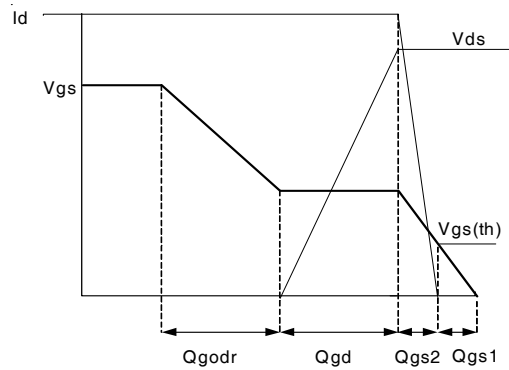
**Fig 14b.** Switching Time Waveforms



**Fig 15. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



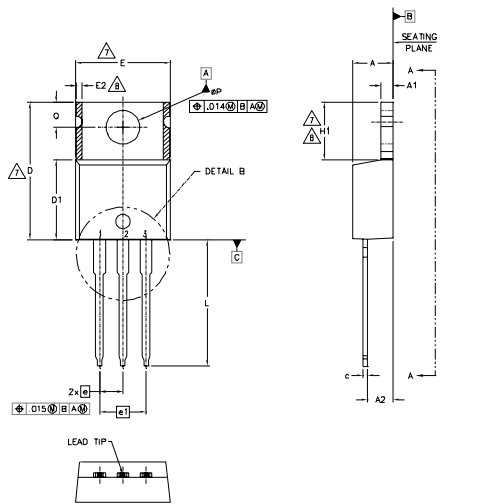
**Fig 16. Gate Charge Test Circuit**



**Fig 17. Gate Charge Waveform**

# IRLB8748PbF

## TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**

**HEXFET**

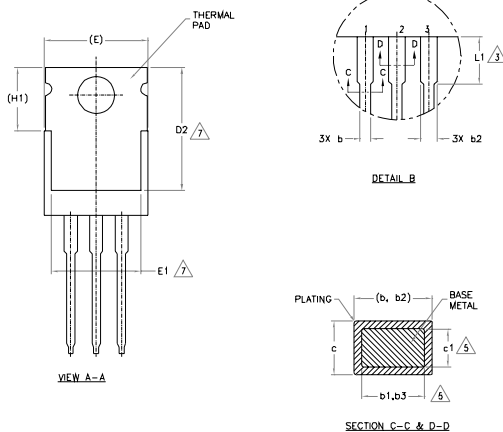
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

**DIODES**

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE



TO-220AB packages are not recommended for Surface Mount Application.

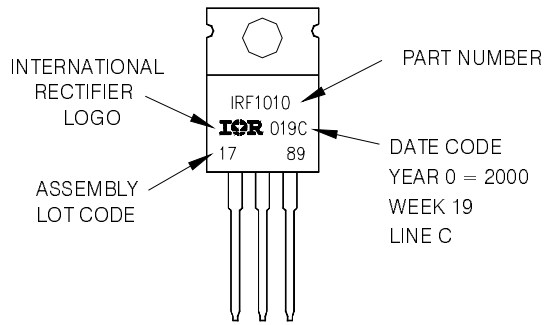
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead - Free"



**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.22\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 32\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 78A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑦ This is only applied to TO-220AB package.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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