MC74VHCT245A

Octal Bus Transceiver

The MC74VHCT245A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It is intended for two−way asynchronous communication between data buses. The direction of data transmission is determined by the level of the DIR input. The output enable pin ($\overline{OE}$) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT245A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: t_{PD} = 4.9 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.6 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Chip Complexity: 304 FETs or 76 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant
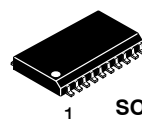
APPLICATION NOTES

- Do not force a signal on an I/O pin when it is an active output, damage may occur.
- All floating (high impedance) input or I/O pins must be fixed by means of pullup or pulldown resistors or bus terminator ICs.
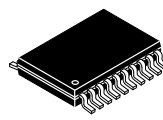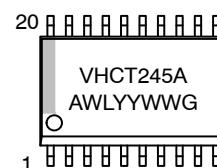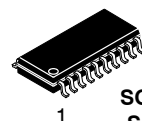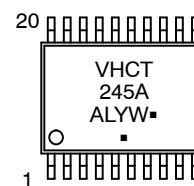
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MARKING DIAGRAMS

SOIC−20WB
SUFFIX DW
CASE 751D

VHCT245A
AWLYYWWG

TSSOP−20
SUFFIX DT
CASE 948E

VHCT
245A
ALYW■

SOEIAJ−20
SUFFIX M
CASE 967

74VHCT245
AWLYWWG
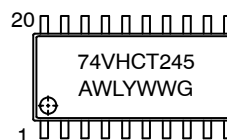
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ■	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.
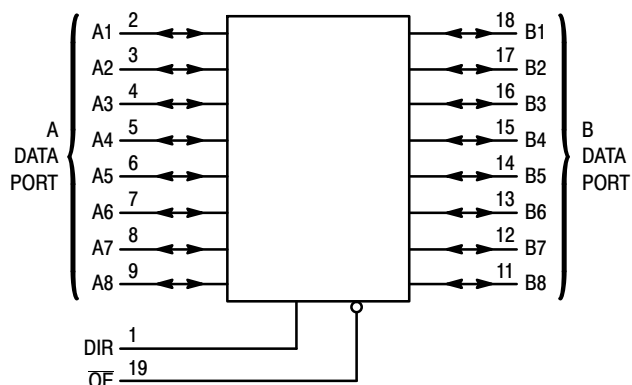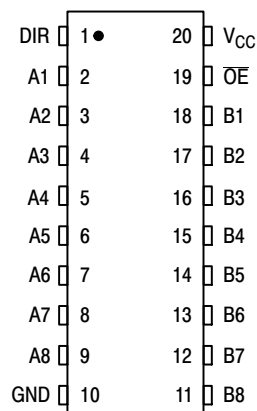
MC74VHCT245A

Figure 1. Logic Diagram

Figure 2. Pin Assignment

FUNCTION TABLE

Control Inputs		Operation
$\overline{OE}$	DIR	
L	L	Data Tx from Bus B to Bus A
L	H	Data Tx from Bus A to Bus B
H	X	Buses Isolated (High−Z State)

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		− 0.5 to + 7.0	V
V_{in}	DC Input Voltage		− 0.5 to + 7.0	V
$V_{I/O}$	DC Output Voltage	Outputs in 3−State High or Low State	− 0.5 to + 7.0 − 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		− 20	mA
I_{OK}	Output Diode Current (V_{OUT} < GND; V_{OUT} > V_{CC})		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature		− 65 to + 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
†Derating − SOIC Packages: − 7 mW/°C from 65° to 125°C
            TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
$V_{I/O}$	DC Output Voltage	Outputs in 3−State High or Low State	0 0	5.5 V_{CC}	V
T_A	Operating Temperature		− 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =5.0V ±0.5V	0	20	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low–Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High–Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	4.5	4.4	4.5		4.4		V
		$I_{OH} = -8mA$	4.5	3.94			3.80		
V_{OL}	Maximum Low–Level Output Voltage $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu A$	4.5		0.0	0.1		0.1	V
		$I_{OL} = 8mA$	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5$ V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3–State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: $V_{IN} = 3.4V$ Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5V$	0			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0ns$)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	Typ	Max	$T_A = -40$ to $85°C$ Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay A to B or B to A	$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$ $C_L = 50pF$		4.9 5.4	7.7 8.7	1.0 1.0	8.5 9.5	ns
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OE}$ to A or B	$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$	$C_L = 15pF$ $C_L = 50pF$		9.4 9.9	13.8 14.8	1.0 1.0	15.0 16.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OE}$ to A or B	$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$	$C_L = 50pF$		10.1	15.4	1.0	16.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 5.0 \pm 0.5V$ (Note 1)	$C_L = 50pF$			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum 3–State Output Capacitance (Output in High–Impedance State)				13				pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2)	16	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0ns$, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Parameter	$T_A = 25°C$ Typ	Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74VHCT245ADWG	SOIC−20WB (Pb−Free)	38 Units / Rail
MC74VHCT245ADWRG	SOIC−20WB (Pb−Free)	1000 / Tape & Reel
MC74VHCT245ADTG	TSSOP−20*	75 Units / Rail
MC74VHCT245ADTRG	TSSOP−20*	2500 / Tape & Reel
MC74VHCT245AMELG	SOEIAJ−20 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.
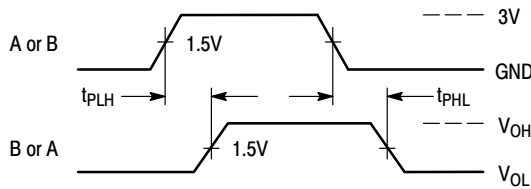
Figure 3. Switching Waveform
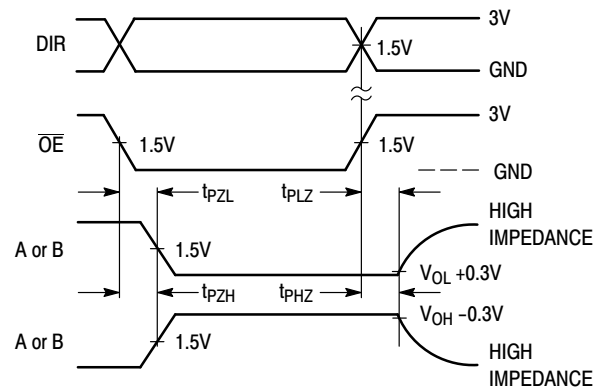
Figure 4. Switching Waveform
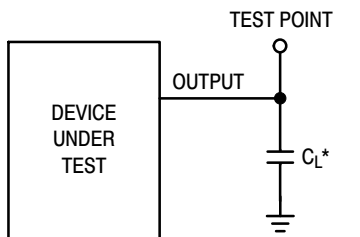
*Includes all probe and jig capacitance

Figure 5. Test Circuit
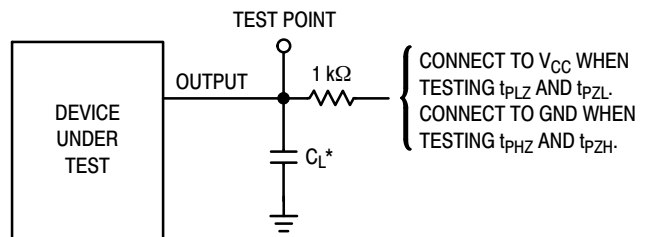
*Includes all probe and jig capacitance

Figure 6. Test Circuit

MC74VHCT245A
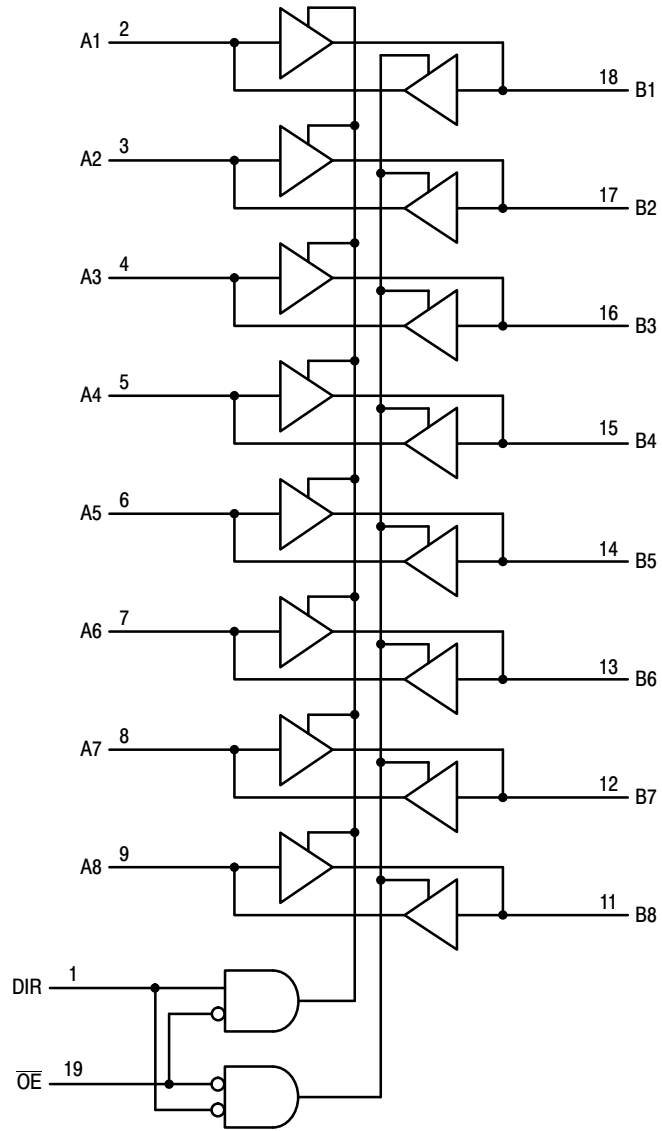
Figure 7. Expanded Logic Diagram

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PACKAGE DIMENSIONS

SOIC−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G
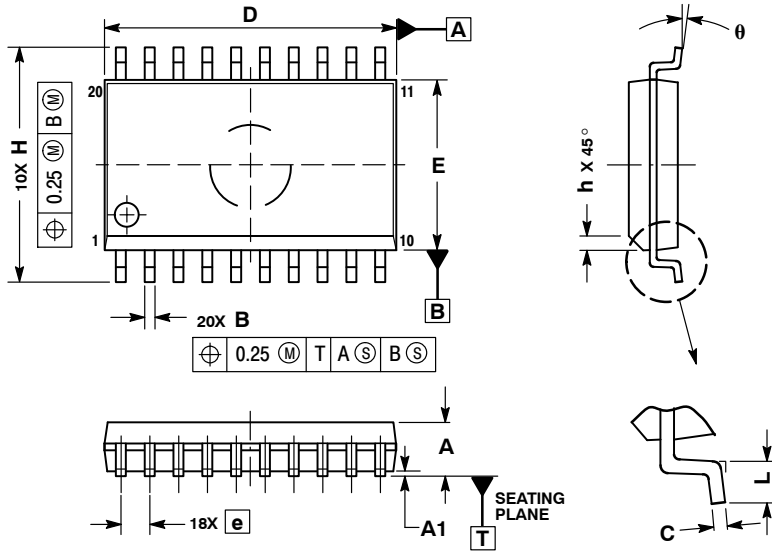
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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PACKAGE DIMENSIONS

TSSOP−20
CASE 948E−02
ISSUE C
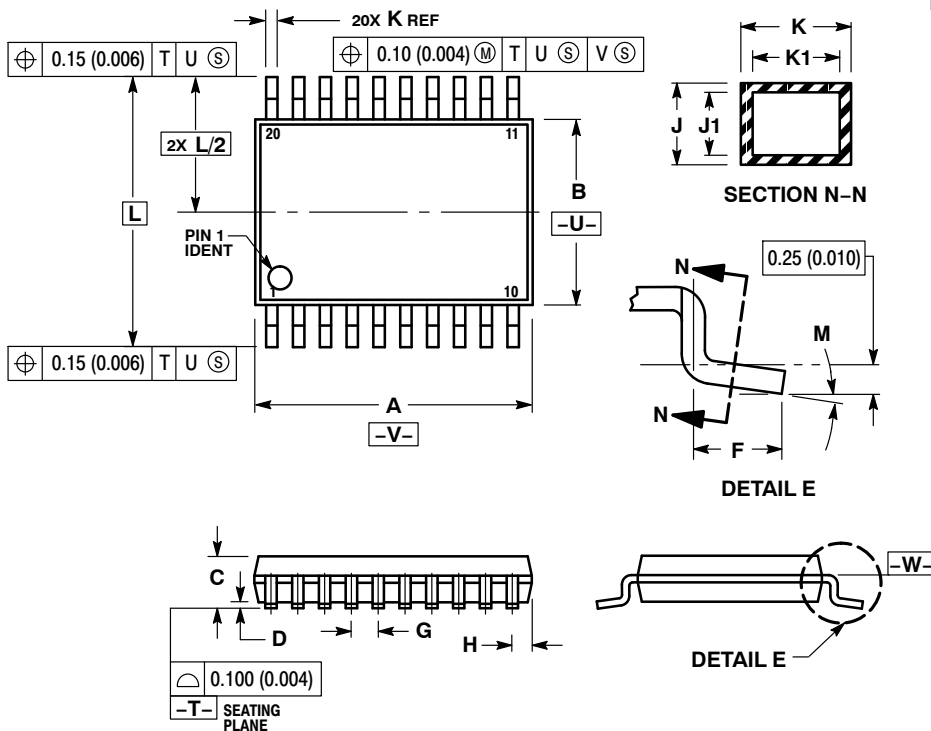
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

SECTION N−N

DETAIL E

SEATING PLANE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS
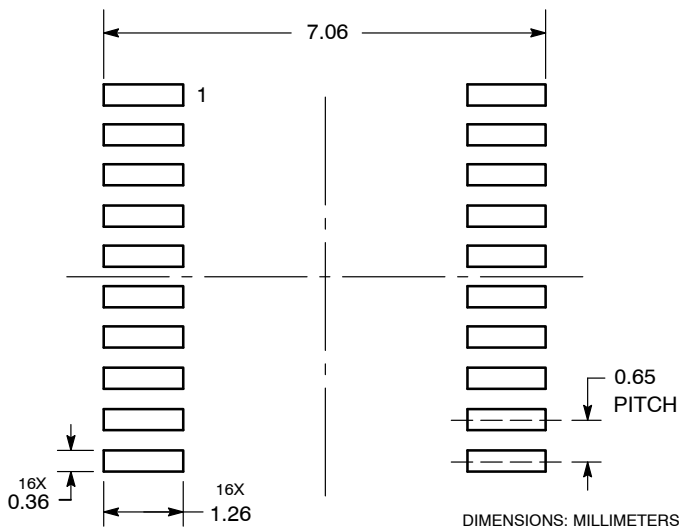
MC74VHCT245A

PACKAGE DIMENSIONS

SOEIAJ−20
M SUFFIX
CASE 967−01
ISSUE A
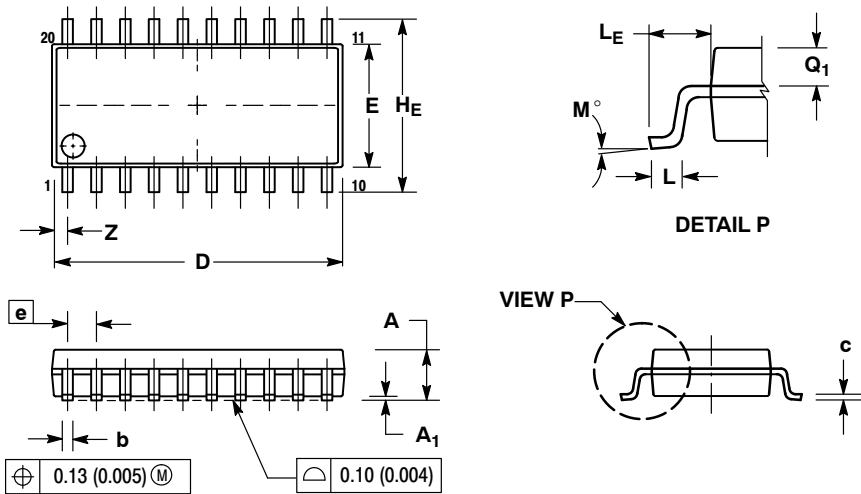
DETAIL P

VIEW P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

MC74VHCT245A/D