NLASB3157

SPDT, 3 Ω R_{ON} Switch

The NLASB3157 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and RDS_{ON} resistances while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power−supply range (from V_{CC} to GND). This device is a drop in replacement for the NC7SB3157.

The select pin has overvoltage protection that allows voltages above $V_{CC,}$ up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

Features

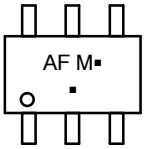
- High Speed: t_{PD} = 1.0 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2.0 μA (Max) at T_A = 25°C
- Standard CMOS Logic Levels
- High Bandwidth, Improved Linearity
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- May be used for Clock Switching, Data Multiplexing, etc.
- R_{ON} Typical = 3 Ω @ V_{CC} = 4.5 V
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- 2 Devices can Switch Balanced Signal Pairs, e.g. LVDS > 200 Mb/s
- Latchup Performance Exceeds 300 mA
- Pin for Pin Drop in for NC7SB3157
- Tiny SC88 and WDFN6 Packages
- ESD Performance:
  - Human Body Model; > 2000 V;
  - Machine Model; > 200 V
- NLVASB3157 Features Extended Automotive Temperature Range; −55°C to +125°C (See Appendix A)
- Pb−Free Packages are Available

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SC−88
DF SUFFIX
CASE 419B



WDFN6
MT SUFFIX
CASE 506AS

AF, F = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

FUNCTION TABLE

Select Input	Function
L	B0 Connected to A
H	B1 Connected to A

ORDERING INFORMATION

Device	Package	Shipping†
NLASB3157DFT2	SC−88	3000 / Tape & Reel
NLASB3157DFT2G	SC−88 (Pb−Free)	3000 / Tape & Reel
NLVASB3157DFT2	SC−88	3000 / Tape & Reel
NLVASB3157DFT2G	SC−88 (Pb−Free)	3000 / Tape & Reel
NLASB3157MTR2G	WDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

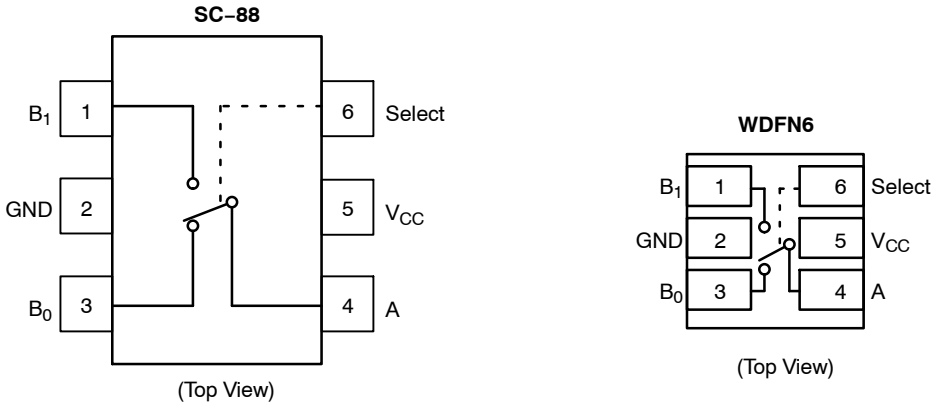


Figure 1. Pin Assignment & Logic Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
DC Switch Voltage (Note 1)	V_{IS}	−0.5 to V_{CC} + 0.5	V
DC Input Voltage (Note 1)	V_{IN}	−0.5 to + 7.0	V
DC Input Diode Current @ V_{IN} < 0 V	I_{IK}	−50	mA
DC Output Current	I_{OUT}	128	mA
DC V_{CC} or Ground Current	I_{CC}/I_{GND}	+100	mA
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Under Bias	T_J	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	T_L	260	°C
Power Dissipation @ +85°C	P_D	180	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	V_{CC}	1.65	5.5	V
Select Input Voltage	V_{IN}	0	5.5	V
Switch Input Voltage	V_{IS}	0	V_{CC}	V
Output Voltage	V_{OUT}	0	V_{CC}	V
Operating Temperature	T_A	−55	+125	°C
Input Rise and Fall Time Control Input V_{CC} = 2.3 V−3.6 V Control Input V_{CC} = 4.5 V−5.5 V	t_r, t_f	 0 0	 10 5.0	ns/V
Thermal Resistance	θ_{JA}	−	350	°C/W

2. Select input must be held HIGH or LOW, it must not float.

DC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = –40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V_{CC} 0.7 V_{CC}		V
V_{IL}	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V_{CC} 0.3 V_{CC}	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5$ V	0–5.5		±0.05	±0.1		±1	μA
I_{OFF}	OFF State Leakage Current	$0 \le A, B \le V_{CC}$	1.65–5.5		±0.05	±0.1		±1	μA
R_{ON}	Switch On Resistance (Note 3)	V_{IN} = 0 V, I_O = 30 mA V_{IN} = 2.4 V, I_O = –30 mA V_{IN} = 4.5 V, I_O = –30 mA	4.5		3.0 5.0 7.0			7.0 12 15	Ω
		V_{IN} = 0 V, I_O = 24 mA V_{IN} = 3 V, I_O = –24 mA	3.0		4.0 10			9.0 20	Ω
		V_{IN} = 0 V, I_O = 8 mA V_{IN} = 2.3 V, I_O = –8 mA	2.3		5.0 13			12 30	Ω
		V_{IN} = 0 V, I_O = 4 mA V_{IN} = 1.65 V, I_O = –4 mA	1.65		6.5 17			20 50	Ω
I_{CC}	Quiescent Supply Current All Channels ON or OFF	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0	5.5			1.0		10	μA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range (Note 3) (Note 7)	I_A = –30 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –24 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –8 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –4 mA, $0 \le V_{Bn} \le V_{CC}$	4.5 3.0 2.3 1.65					25 50 100 300	Ω
ΔR_{ON}	On Resistance Match Between Channels (Note 3) (Note 4) (Note 5)	I_A = –30 mA, V_{Bn} = 3.15 I_A = –24 mA, V_{Bn} = 2.1 I_A = –8 mA, V_{Bn} = 1.6 I_A = –4 mA, V_{Bn} = 1.15	4.5 3.0 2.3 1.65		0.15 0.2 0.5 0.5				Ω
R_{flat}	On Resistance Flatness (Note 3) (Note 4) (Note 6)	I_A = –30 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –24 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –8 mA, $0 \le V_{Bn} \le V_{CC}$ I_A = –4 mA, $0 \le V_{Bn} \le V_{CC}$	5.0 3.3 2.5 1.8		6.0 12 28 125				Ω

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized but not tested in production.
5. $\Delta R_{ON} = R_{ON}$ max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
7. Guaranteed by Design.

AC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Unit	Figure Number
				Min	Typ	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 9)	V_I = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					 1.2 0.8 0.3	ns	Figures 2, 3
t_{PZL} t_{PZH}	Output Enable Time Turn On Time (A to B_n)	V_I = 2 × V_{CC} for t_{PZL} V_I = 0 V for t_{PZH}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 7.6 5.7	ns	Figures 2, 3
t_{PLZ} t_{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V_I = 2 × V_{CC} for t_{PLZ} V_I = 0 V for t_{PHZ}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 5.3 3.8	ns	Figures 2, 3
t_{B-M}	Break Before Make Time (Note 8)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4
Q	Charge Injection (Note 8)	C_L = 0.1 nF, V_{GEN} = 0 V R_{GEN} = 0 Ω	5.0 3.3		7.0 3.0				pC	Figure 5
OIRR	Off Isolation (Note 10)	R_L = 50 Ω f = 10 MHz	1.65–5.5		–57				dB	Figure 6
Xtalk	Crosstalk	R_L = 50 Ω f = 10 MHz	1.65–5.5		–54				dB	Figure 7
BW	–3 dB Bandwidth	R_L = 50 Ω	1.65–5.5		250				MHz	Figure 10
THD	Total Harmonic Distortion (Note 8)	R_L = 600 Ω 0.5 V_{P-P} f = 600 Hz to 20 kHz	5.0		0.011				%	

CAPACITANCE – NLASB3157 (Note 11)

Symbol	Parameter	Test Conditions	Typ	Max	Unit	Figure Number
C_{IN}	Select Pin Input Capacitance	V_{CC} = 0 V	2.3		pF	
C_{IO-B}	B Port Off Capacitance	V_{CC} = 5.0 V	6.5		pF	Figure 8
C_{IOA-ON}	A Port Capacitance when Switch is Enabled	V_{CC} = 5.0 V	18.5		pF	Figure 9

8. Guaranteed by Design.
9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
10. Off Isolation = 20 $\log_{10}$ [V_A/V_{Bn}].
11. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

APPENDIX A

DC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V_{CC} 0.7 V_{CC}		V
V_{IL}	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V_{CC} 0.3 V_{CC}	V
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0–5.5		±0.05	±0.1		±1	μA
I_{OFF}	OFF State Leakage Current	0 ≤ A, B ≤ V_{CC}	1.65–5.5		±0.05	±0.1		±1	μA
R_{ON}	Switch On Resistance (Note 12)	V_{IN} = 0 V, I_O = 30 mA V_{IN} = 2.4 V, I_O = –30 mA V_{IN} = 4.5 V, I_O = –30 mA	4.5		3.0 5.0 7.0			8.5 13.0 15.0	Ω
		V_{IN} = 0 V, I_O = 24 mA V_{IN} = 3 V, I_O = –24 mA	3.0		4.0 10			11 20	
		V_{IN} = 0 V, I_O = 8 mA V_{IN} = 2.3 V, I_O = –8 mA	2.3		5.0 13			12 30	
		V_{IN} = 0 V, I_O = 4 mA V_{IN} = 1.65 V, I_O = –4 mA	1.65		6.5 17			20 50	
I_{CC}	Quiescent Supply Current All Channels ON or OFF	V_{IN} = V_{CC} or GND I_{OUT} = 0	5.5			1.0		10	μA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range (Note 12) (Note 14)	I_A = –30 mA, 0 ≤ V_{Bn} ≤ V_{CC} I_A = –24 mA, 0 ≤ V_{Bn} ≤ V_{CC} I_A = –8 mA, 0 ≤ V_{Bn} ≤ V_{CC} I_A = –4 mA, 0 ≤ V_{Bn} ≤ V_{CC}	4.5 3.0 2.3 1.65					25 50 100 300	Ω

12. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
13. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
14. Guaranteed by Design.

*** For ΔR_{ON}, R_{FLAT}, Q, OIRR, Xtalk, BW, THD, and CIN see −40°C to 85°C section.**

APPENDIX A

AC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = +25°C			T_A = −55°C to +125°C		Unit	Figure Number
				Min	Typ	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 16)	V_I = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					 1.2 0.8 0.3	ns	Figures 2, 3
t_{PZL} t_{PZH}	Output Enable Time Turn On Time (A to B_n)	V_I = 2 × V_{CC} for t_{PZL} V_I = 0 V for t_{PZH}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 9.0 7.0	ns	Figures 2, 3
t_{PLZ} t_{PHZ}	Output Disable Time Turn Off Time (A Port to B Port)	V_I = 2 × V_{CC} for t_{PLZ} V_I = 0 V for t_{PHZ}	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 6.5 5.0	ns	Figures 2, 3
t_{B-M}	Break Before Make Time (Note 15)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4

15. Guaranteed by Design.
16. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

*** For ΔR_{ON}, R_{FLAT}, Q, OIRR, Xtalk, BW, THD, and CIN see −40°C to 85°C section.**

AC LOADING AND WAVEFORMS

NOTE: Input driven by 50 Ω source terminated in 50 Ω
NOTE: C_L includes load and stray capacitance
NOTE: Input PRR = 1.0 MHz; t_W = 500 ns

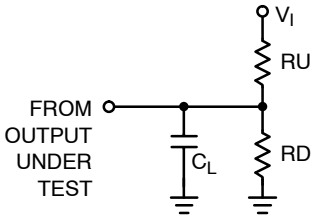


Figure 2. AC Test Circuit

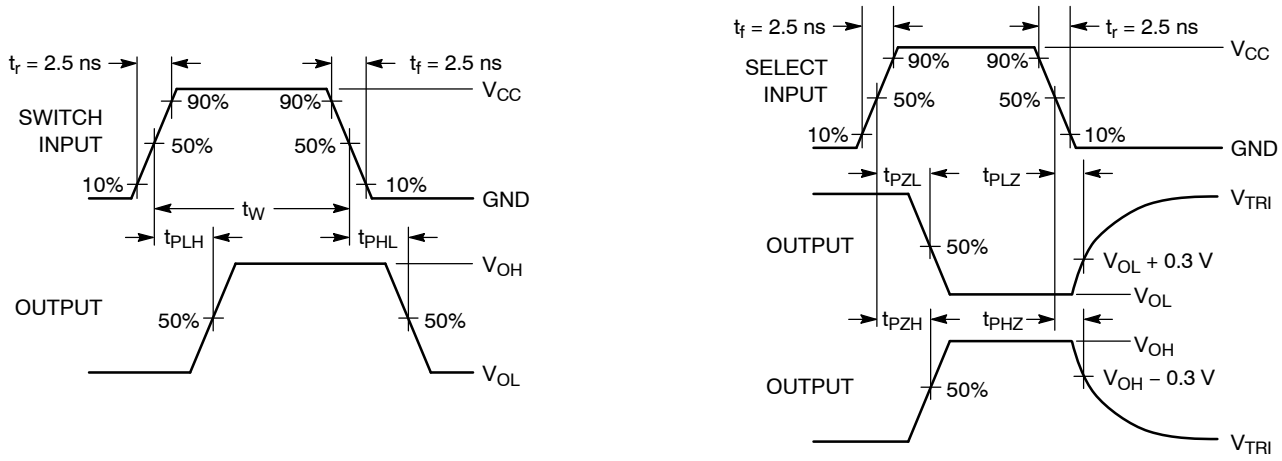


Figure 3. AC Waveforms

Figure 4. Break Before Make Interval Timing

AC LOADING AND WAVEFORMS

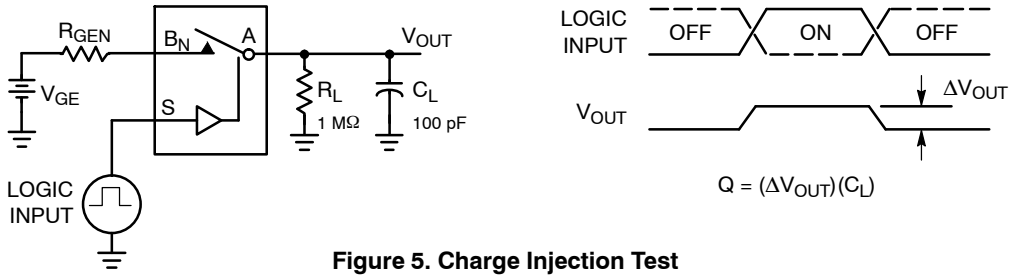


Figure 5. Charge Injection Test

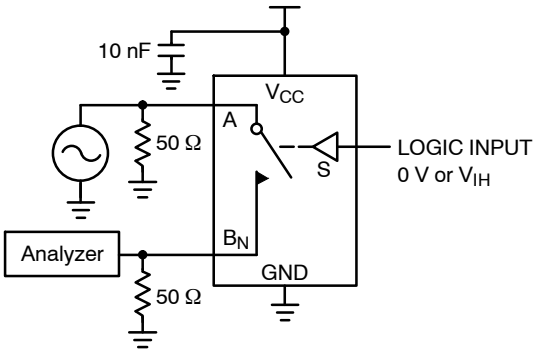


Figure 6. Off Isolation

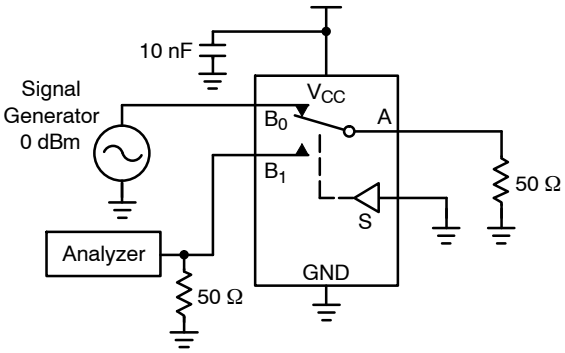


Figure 7. Crosstalk

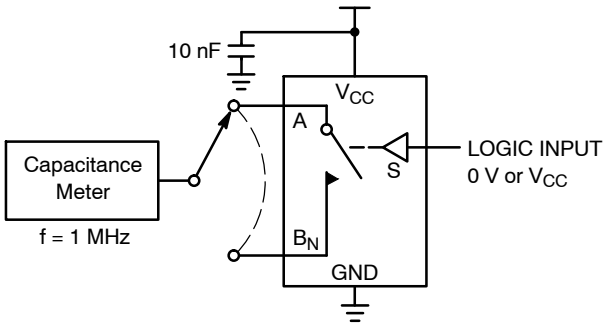


Figure 8. Channel Off Capacitance

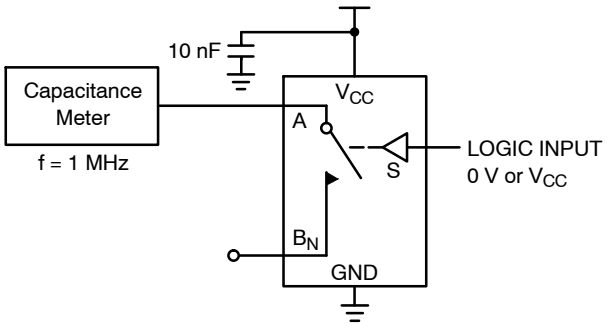


Figure 9. Channel On Capacitance

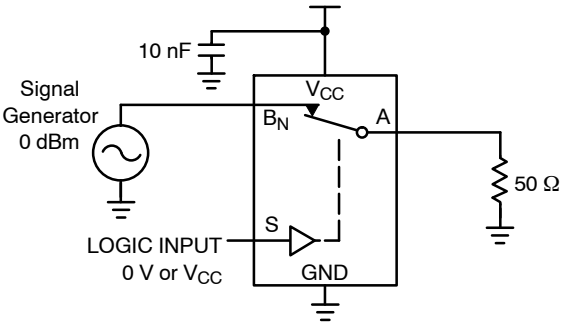
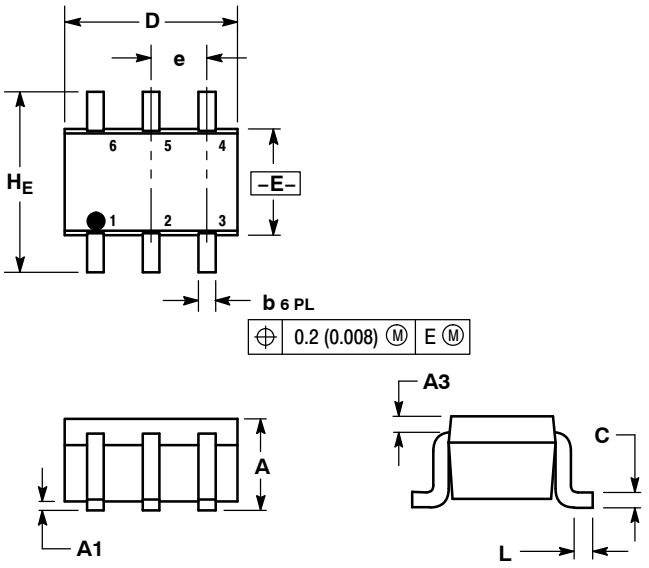


Figure 10. Bandwidth

PACKAGE DIMENSIONS

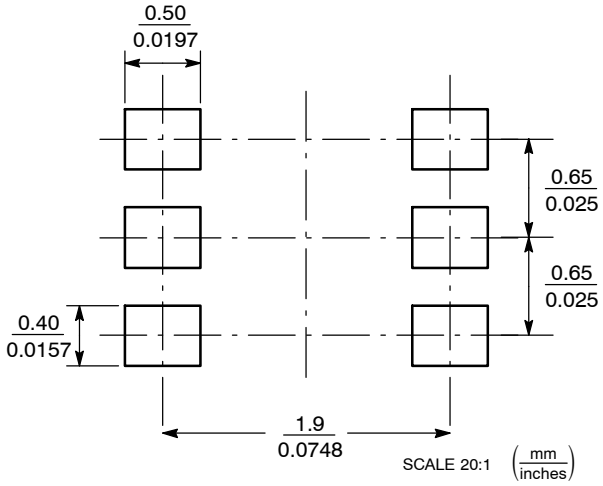
SC−88/SOT−363/SC−70
DF SUFFIX
CASE 419B−02
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3		0.20 REF			0.008 REF	
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65 BSC			0.026 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

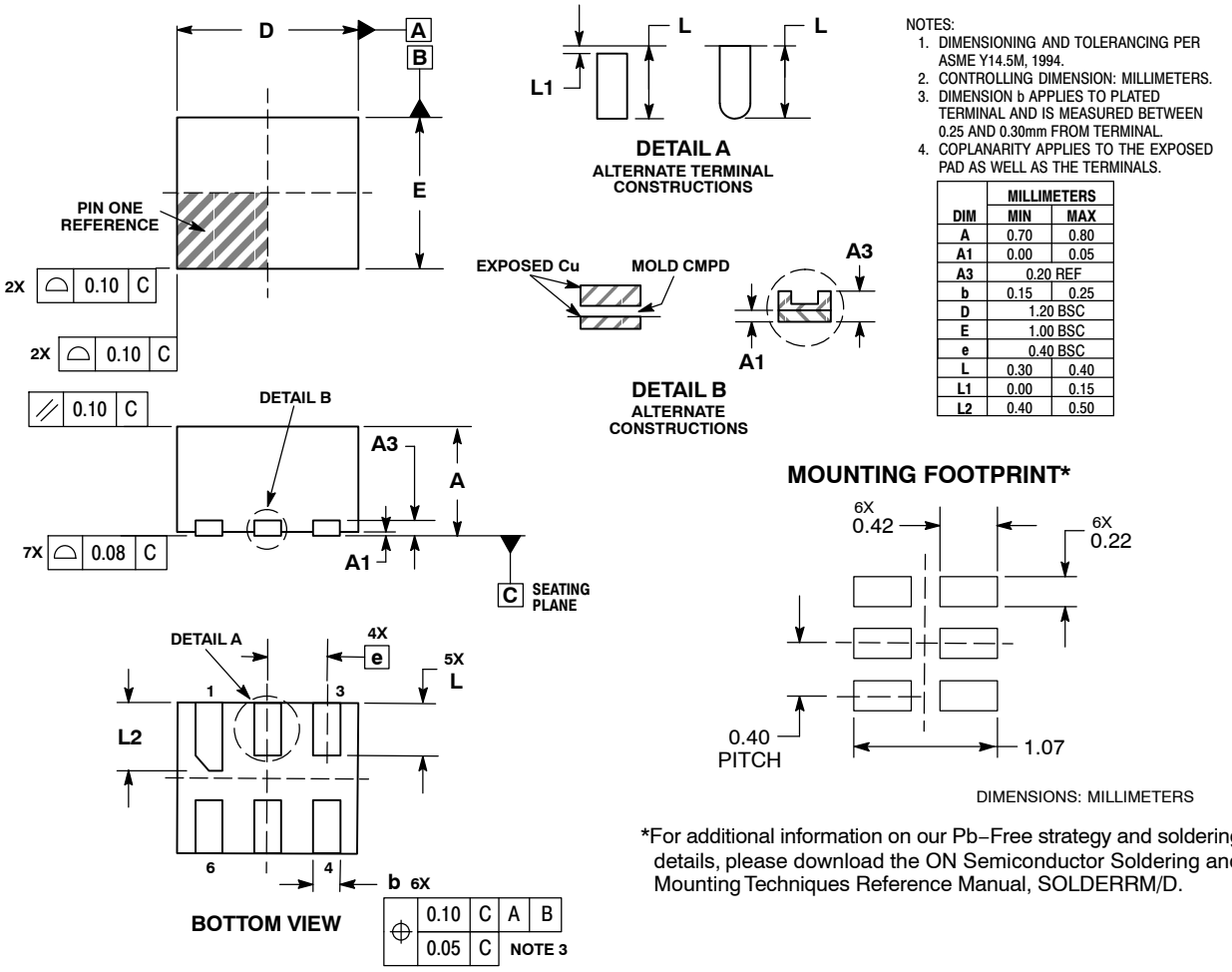
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WDFN6 1.2x1.0, 0.4P
CASE 506AS−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

MOUNTING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your loca
Sales Representative