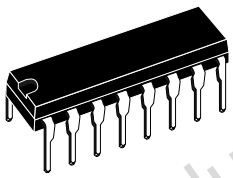
TDA1175P

LOW-NOISE VERTICAL DEFLECTION SYSTEM

FEATURES SUMMARY

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS
- ESD PROTECTED

Figure 1. Package



POWERDIP16
(Plastic Package)

DESCRIPTION

The TDA1175P is a monolithic integrated circuit in POWERDIP16 plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors.

The functions incorporated are: synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

Figure 2. Pin Connections

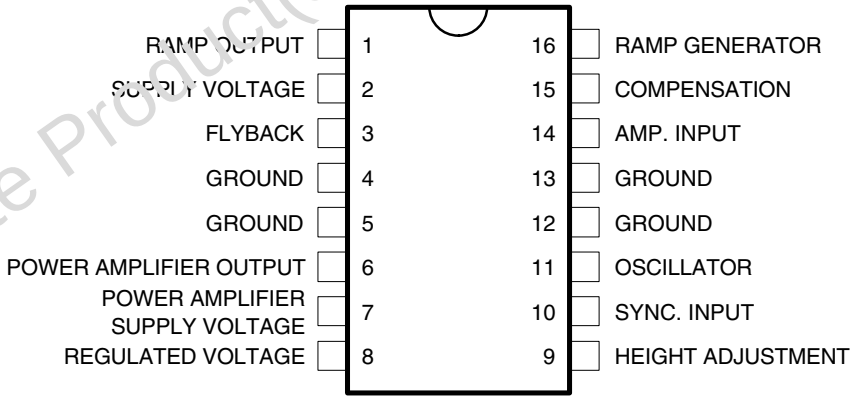


Figure 3. Block Diagram

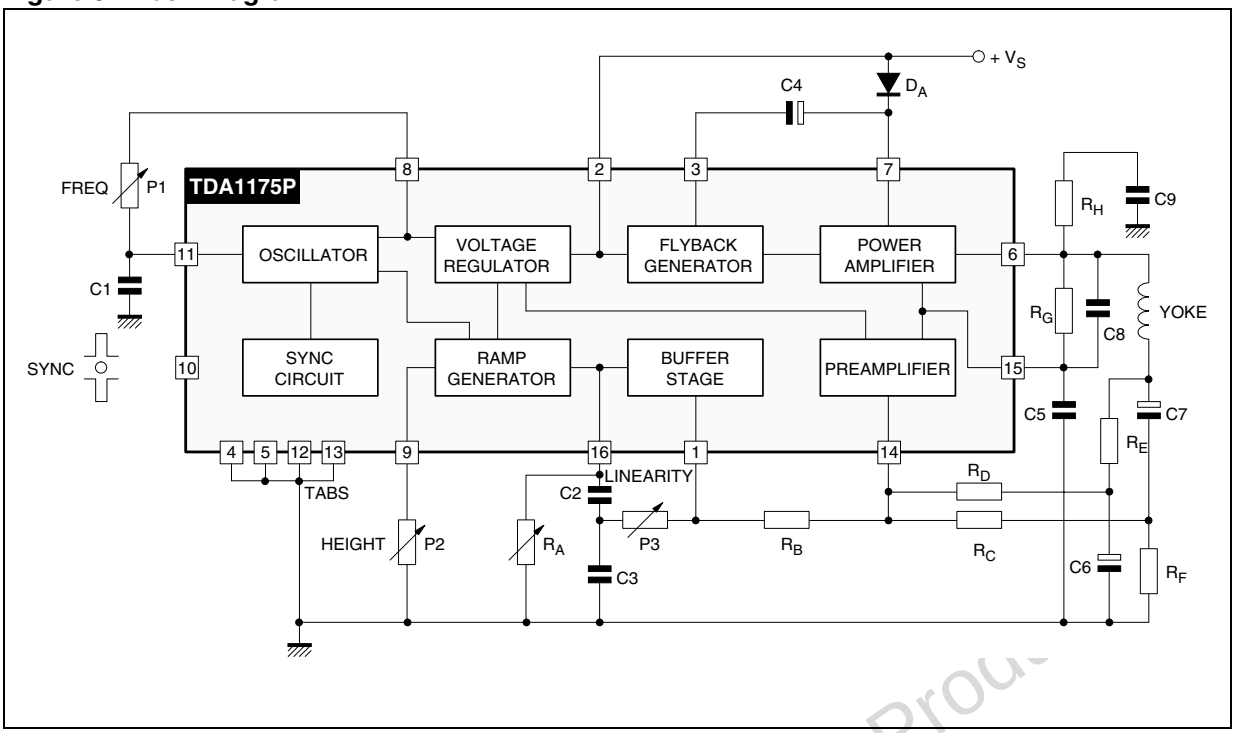


Table 1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_6, V_7	Flyback Peak Voltage	60	V
V_{14}	Power Amplifier Input Voltage	+ 10 – 0.5	V
I_O	Output Peak Current (non repetitive) at t = 2ms	2	A
I_O	Output Peak Current at f = 50Hz, t ≤ 10µs	2.5	A
I_O	Output Peak Current at f = 50Hz, t > 10µs	1.5	A
I_3	Pin 3 DC Current at $V_6 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50Hz, $t_{fly} \leq 1.5$ms	1.8	A
I_{10}	Pin 10 Current	± 20	mA
P_{TOT}	Power Dissipation at at T_{tab} = 90°C	4.3	W
	Power Dissipation at T_{amb} = 70°C (free air) (1)	1	W
T_{STG} , T_j	Storage and Junction Temperature	– 40 to 150	°C

Table 2. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}tab)}$	Thermal Resistance Junction-pin Max.	12	°C/W
$R_{th\ (j\text{-}amb)}$	Thermal Resistance Junction-ambient Max.	80	°C/W(1)

Note: 1. Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, unless otherwise specified)

Table 3. DC CHARACTERISTICS

(Refer to the test circuits, VS = 35V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	I_3 = 0		7	14	mA	5
I7	Pin 7 Quiescent Current	I_6 = 0		8	17	mA	5
$-I_{11}$	Oscillator Bias Current	V_{11} = 1V		0.1	1	µA	4
$-I_{14}$	Amplifier Input Bias Current	V_{14} = 1V		1	10	µA	5
$-I_{16}$	Ramp Generator Bias Current	V_{16} = 0		0.02	0.3	µA	4
$-I_{16}$	Ramp Generator Current	I_9 = 20µA, V_{16} = 0	18.5	20	21.5	µA	5
$\frac{\Delta I_{16}}{I_{16}}$	Ramp Generator Non-linearity	ΔV_{16} = 0 to 12V, I_9 = 20µA		0.2	1	%	5
V_S	Supply Voltage Range		10		35	V	
V_1	Pin 1 Saturation Voltage to Ground	I_1 = 1mA		1	14	V	
V_3	Pin 3 Saturation Voltage to Ground	I_3 = 10mA		1.5	2.5	V	4
V_6	Qiuescent output Voltage	V_s = 10V, R1 = 1kΩ, R2 = 1kΩ	4.1	4.4	4.7	V	4
		V_s = 35V, R1 = 3kΩ, R2 = 1kΩ	8.2	8.8	9.4	V	4
V_{6L}	Output Saturation Voltage to Ground	– I_6 = 0.1A		0.9	1.2	V	6
		– I_6 = 0.8A		1.8	2.2	V	6
V_{6H}	Output Saturation Voltage to Supply	I_6 = 0.1A		1.4	2.1	V	7
		I_6 = 0.8A		2.8	3.1	V	7
V_8	Regulated Voltage at Pin 8		6.5	6.7	6.9	V	5
V_9	Regulated Voltage at Pin 9	I_9 = 20µA	6.6	6.8	7	V	5
$\frac{\lvert\Delta V_8\rvert}{\Delta V_S} \; \frac{\lvert\Delta V_9\rvert}{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	ΔVs = 10 to 35V		1	2	mV/V	5
V_{14}	Amplifier Input Reference Voltage	$V_{10} \leq$ 0.4V	2.20	2.27	2.35	V	

Table 4. AC CHARACTERISTICS
(Refer to the AC test circuit, V_S = 22V, f = 50Hz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_S	Supply Current	$I_Y = 1_{APP}$		140		mA	8
I10	Sync. Input Current (positive or negative)		0.5		2	mA	8
V_6	Flyback Voltage	$I_Y = 1_{APP}$		45		V	8
t_{fly}	Flyback Time	$I_Y = 1_{APP}$		0.7		ms	8
V_{ON}	Peak to Peak Output Noise	Pin 11 Connected to GND		18	30	mV_{pp}	8
f_O	Free Running Frequency	(P1 + R1) = 300kΩ C9 = 0.1 μF	36	43.5		Hz	8
f_{OPER}	Operating Frequency Range		10		120	Hz	8
Δf	Synchronization Range	I_{10} = 0.5mA, C9 = 0.1μF (P1+R1) = 300kΩ	14			Hz	8
$\frac{\Delta f}{\Delta V_S}$	Frequency Drift with Supply Voltage	V_S = 10 to 35V		0.005		Hz/V	8
$\frac{\lvert\Delta f\rvert}{\Delta T_{ab}}$	Frequency Drift with tab Temperature	T_{tab} = 40 to 120°C		0.01		Hz/°C	8

DC TEST CIRCUITS

Figure 4.

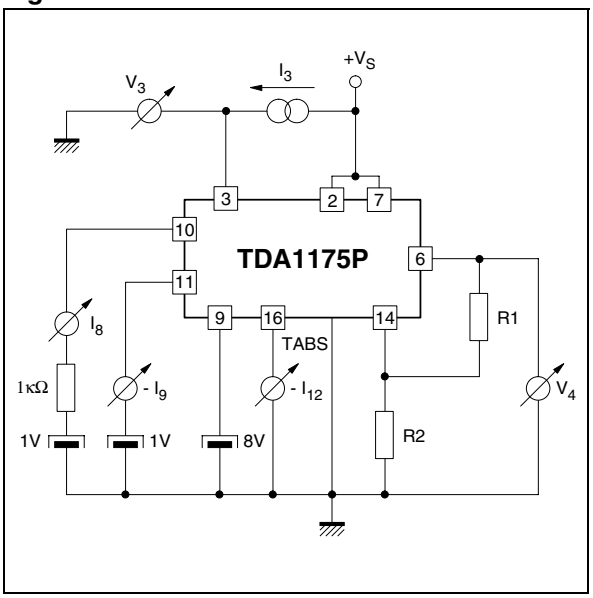


Figure 6.

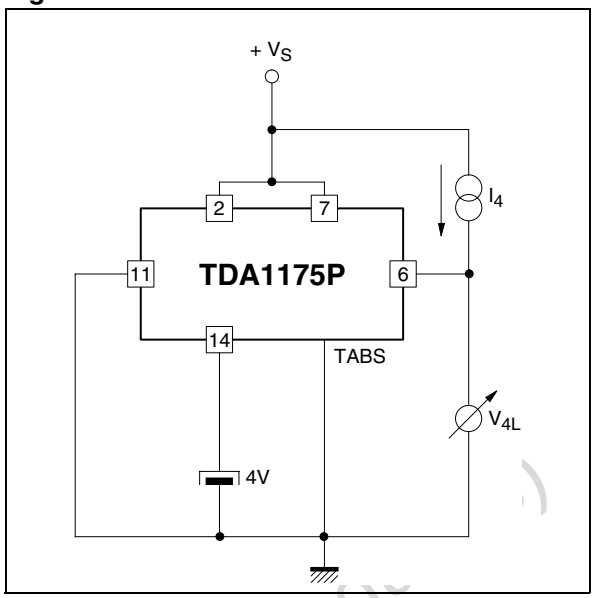


Figure 5.

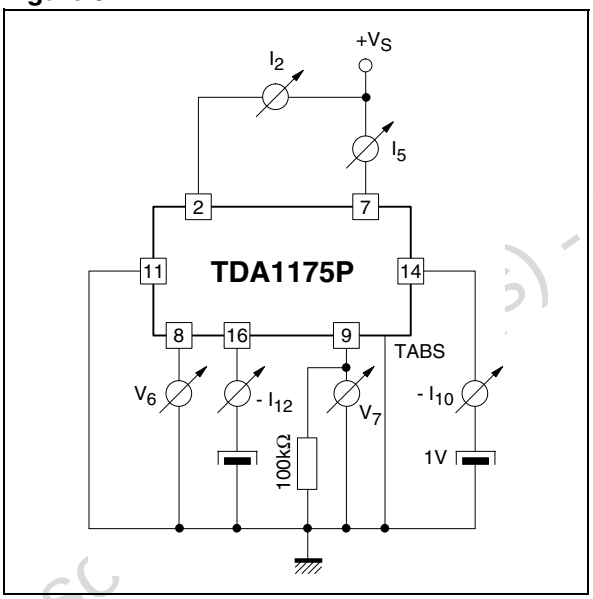


Figure 7.

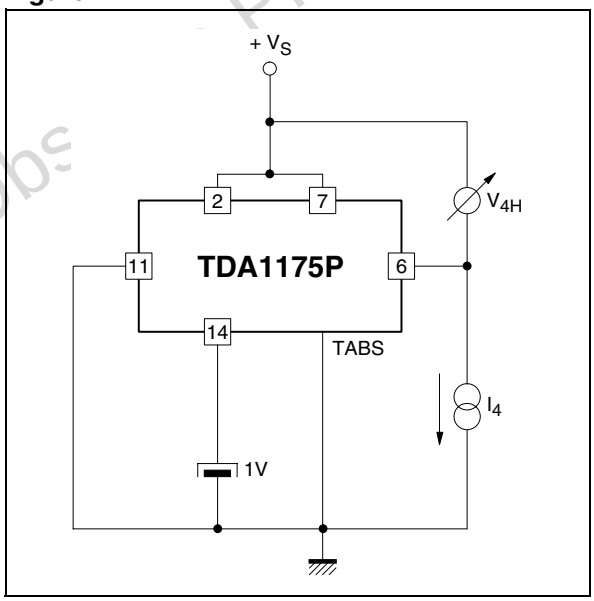


Figure 8. AC Test and Application Circuit for Large Screen B/W TV Set 10Ω/20mH/1A$_{PP}$

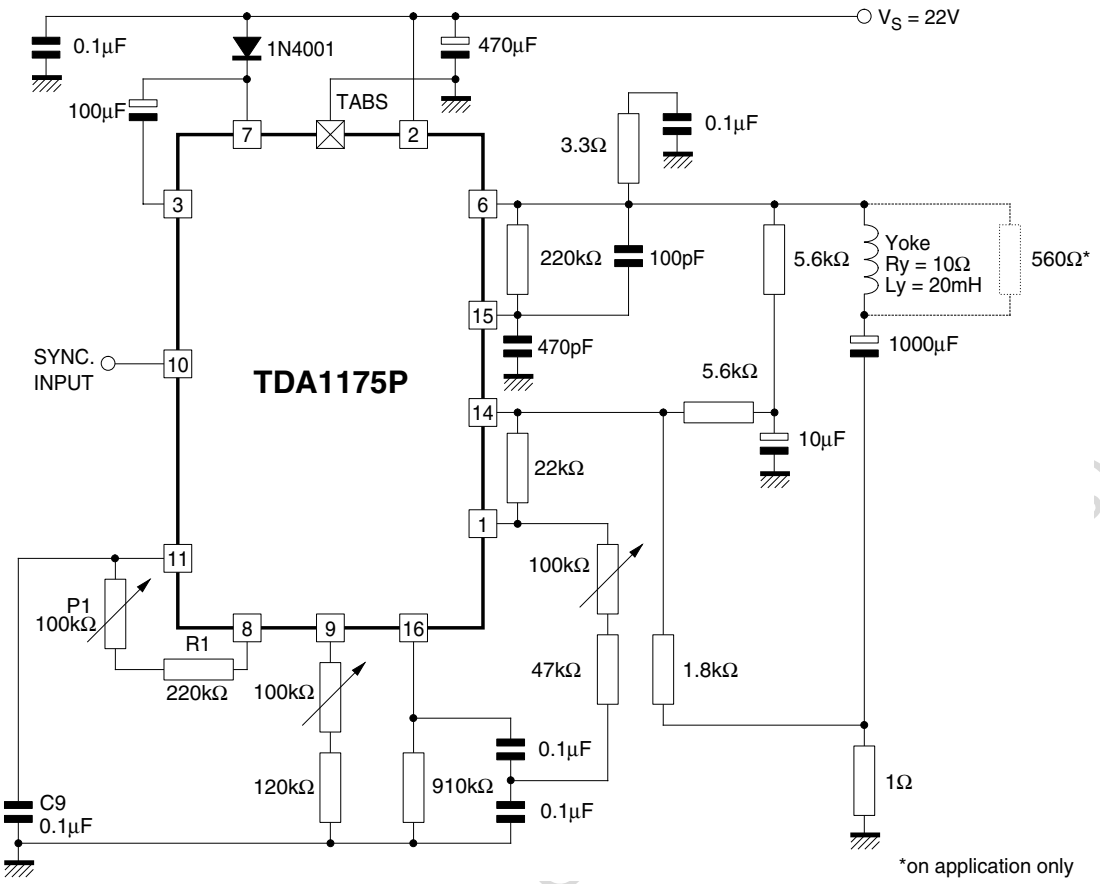


Figure 9. Typical Application Circuit for VGA Monitor (R_Y = 10Ω, L_Y = 20mH, I_Y = 0.8A_{PP})

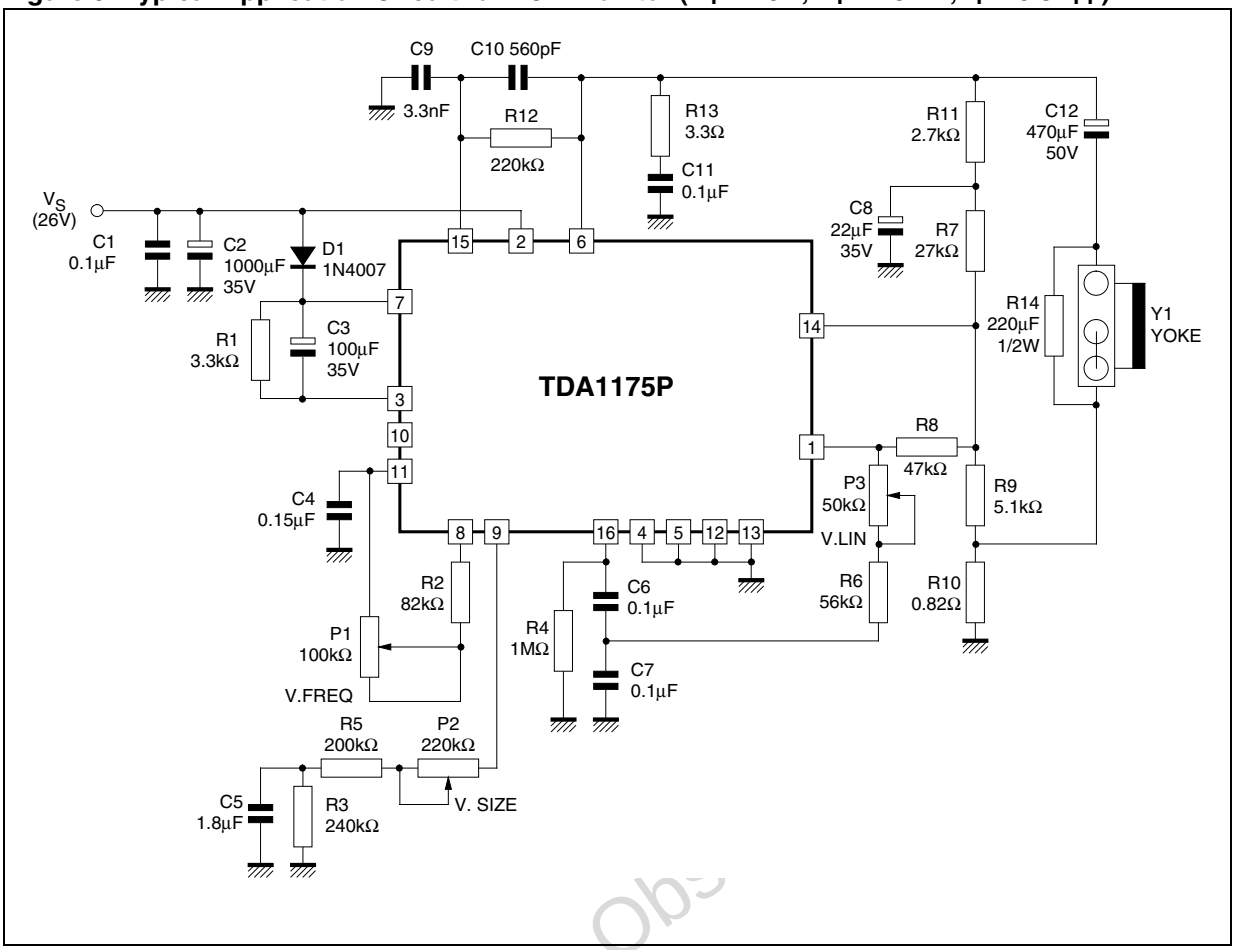


Figure 10. P.C. Board and Components Layout of the Circuit of Figure 9 (1:1 scale)

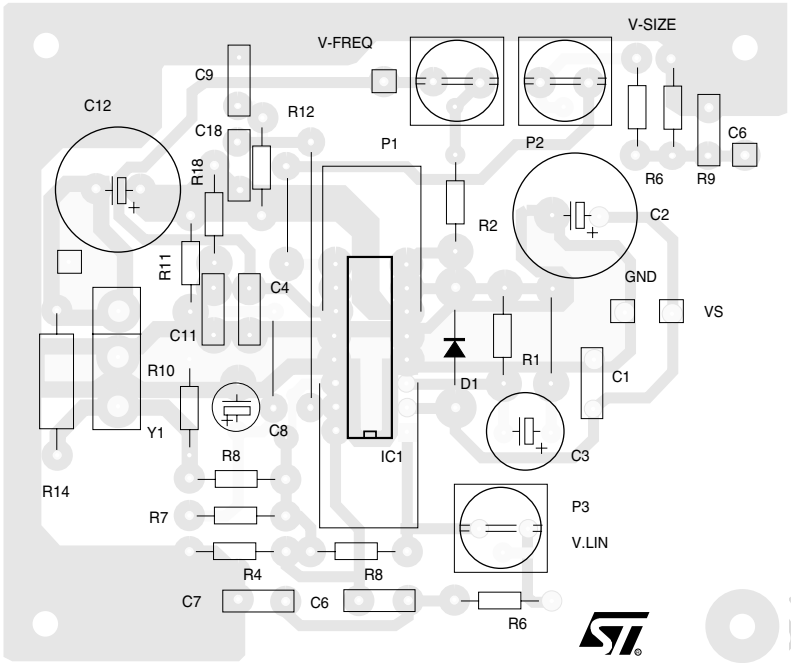


Table 5. Bill of Material

Item	Qty	Reference	Part
1	4	C1, C6, C7, C11	0.1µF
2	1	C2	1000µF 35V
3	1	C3	100µF 35V
4	1	C4	0.15µF
5	1	C5	1.8nF
6	1	C8	22µF 35V
7	1	C9	3.3nF
8	1	C10	560pF
9	1	C12	470µF 50V
10	1	D1	1N4007
11	1	IC1	TDA1175P
12	1	P1	100kΩ POT
13	1	P2	220kΩ POT
14	1	P3	50kΩPOT
15	1	R1	3.3kΩ
16	1	R2	82kΩ
17	1	R3	240kΩ
18	1	R4	1MΩ
19	1	R5	200kΩ
20	1	R6	56kΩ
21	1	R7	27kΩ
22	1	R8	47kΩ
23	1	R9	5.1kΩ
24	1	R10	0.82Ω
25	1	R11	2.7kΩ
26	1	R12	220kΩ
27	1	R13	3.3Ω
28	1	R14	220Ω 1/2W
29	1	Y1	YOKE

MOUNTING INSTRUCTION

The R_{th} (j-a) can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Figure 11) or to an external heatsink (Figure 12).

The diagram of Figure 13 shows the maximum dissipable power P_{tot} and the R_{th} ($_{j-a}$) as a function of the side "l" of two equal square copper areas having a thicknessof 35µ (1.4 mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 11. Example of P.C. Board Copper Area

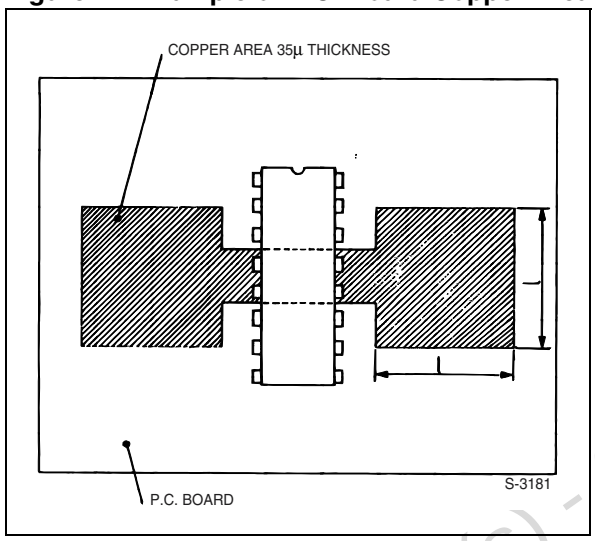


Figure 12. External Heatsink Mounting Example

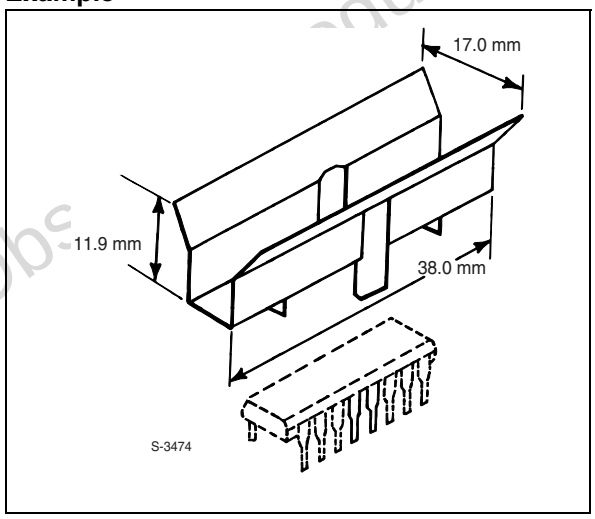


Figure 13. Maximum Power Dissipation and Junction-ambient Thermal Resistance versus "l"

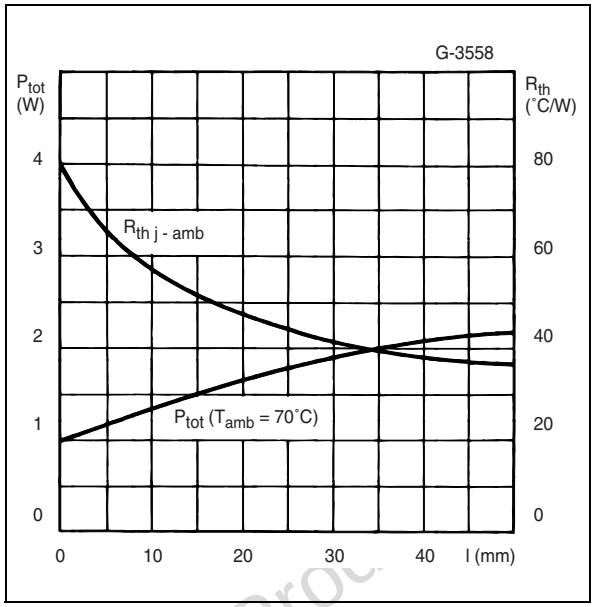
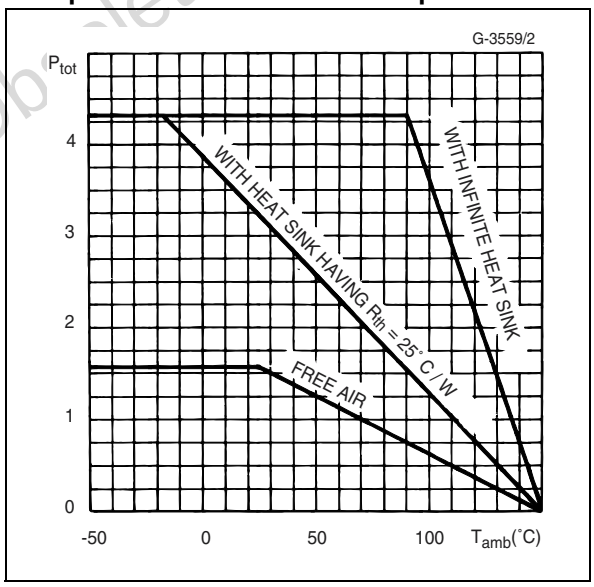


Figure 14. Maximum Allowable Power Dissipation versus Ambient Temperature



PART NUMBERING

Table 6. Order Codes

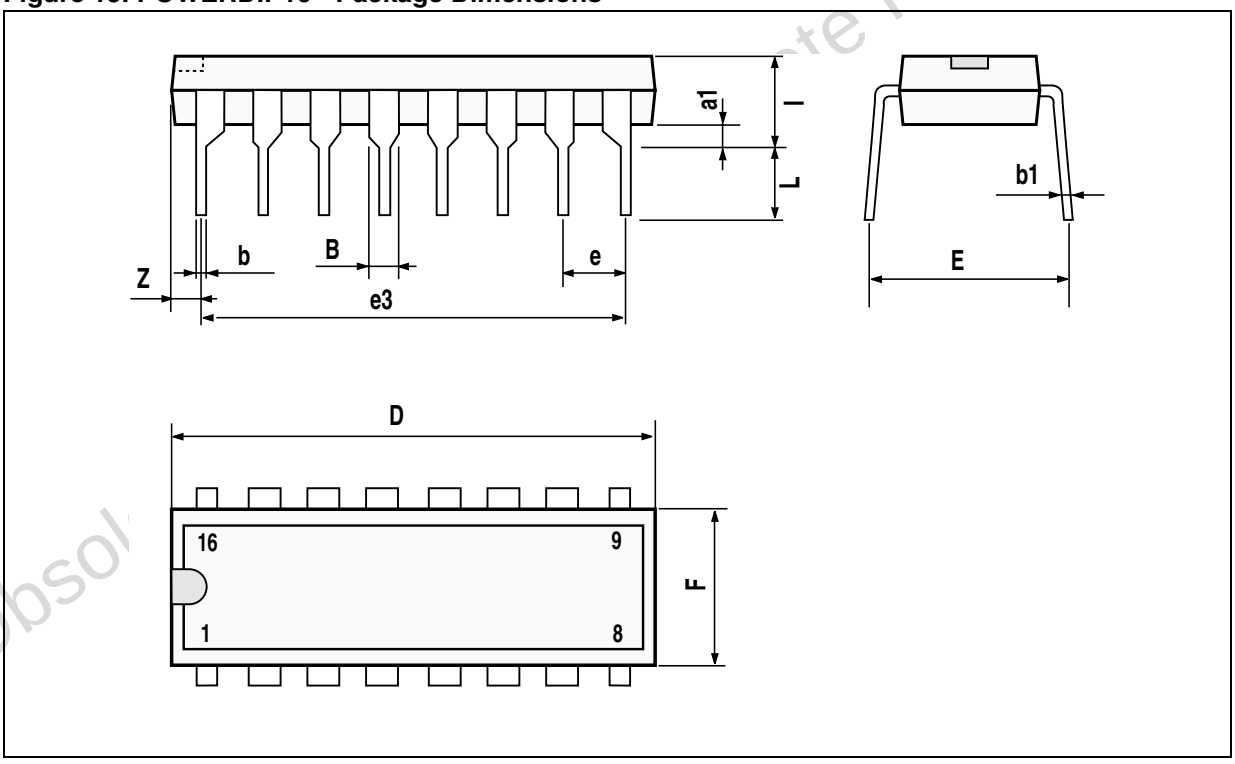
Part Number	Package	Temperature Range
TDA1175P	POWERDIP16	-25 to 85 °C

PACKAGE MECHANICAL

Table 7. POWERDIP16 - Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

Figure 15. POWERDIP16 - Package Dimensions



Note: Drawing is not to scale

REVISION HISTORY

Table 8. Revision History

Date	Revision	Description of Changes
August-1995	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.