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S1D13L04
XGA Simple LCD Controller

Hardware Functional Specification

Document Number: XB3A-A-001-01

Status: Revision 1.0

Issue Date: 2016/3/18

NOTICE

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Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13L04 XGA Simple LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 Overview Description

The S1D13L04 is a simple, multi-purpose Graphics LCD Controller which supports up to XGA resolution TFT panels. With an external SDRAM memory controller, it allows up to 16Mbyte as a display frame buffer. The S1D13L04 supports most popular CPU interfaces in both 16-bit and Direct/Indirect variations.

The S1D13L04's combination of multiple CPU interfaces and display interface types offers a versatile, yet easy to develop display system. Additionally, it offers such features as Multiple Windows (PIP), Alpha Blending, Gamma Correction, and Mirror/Rotation which allow user configurability of various images on the Main/PIP1/PIP2 windows. The S1D13L04 is a flexible, low cost, low power solution that meets the demands of embedded markets such as medical, office automation, factory automation, home automation and measuring instruments, where total system cost concerns can still be met when using TFT panels up to XGA resolution.

Chapter 2 Features

2.1 Memory

- Uses external SDRAM or mobile SDRAM as the display buffer (no embedded memory)
  - Memory is addressable using direct or indirect access modes
  - Linear access to the first 1M bytes of memory and four configurable 256K byte windows into the remaining area
- SDRAM Interface
  - Supports up to 100MHz SDRAM bus clock
  - Supports x16 SDRAM interfaces
  - Supports 8/16M bytes of 4 bank SDRAM
  - Supports 8/16M bytes of 4 bank Mobile SDRAM
  - Low power design
  - Automatic re-entry into self refresh mode

Note
For memory usage guidelines, see Section 14.2, “Memory Bandwidth” on page 176.

2.2 CPU Interfaces

- Direct and indirect interface support of the Intel 80, 68 16-bit CPU interfaces.
- Serial Host Interface
- Registers are memory-mapped - M/R# input selects between memory and register address space

2.3 Panel Interface Support

- RGB interface single-panels
  - Color TFT Panels
  - 16/18-bit interface
  - Generic TFT/TFD interface
- Optional serial command interface supports:
  - TFT w/µ-Wire interface (16-bit)
  - EPSON ND-TFD 4 pin interface (8-bit)
  - EPSON ND-TFD 3 pin interface (9-bit)
  - 8/24-bit command interface

- Panel Resolution Examples
  - For memory usage guidelines, see Section 14.2, “Memory Bandwidth” on page 176.

2.4 Display Features

- Multiple window (layer) support
  - Main window and PIP1 window (if enabled) form the View Port (bottom layer)
  - 8/16/32 bit-per-pixel (bpp) color depths
  - alpha blending is not supported for the View Port
  - mirror and 180° rotation functions
  - optional gamma correction
  - PIP2 window (if enabled) is the top layer
  - 8/16/32 bit-per-pixel (bpp) color depths
  - optional alpha blending function (ARGB 1:5:5:5 / ARGB 4:4:4:4 / ARGB 8:8:8:8 formats including alpha map)
  - optional transparency function
  - mirror and 180° rotation functions
  - optional gamma correction
- Mirror and Rotation
  - Mirror function performs a horizontal flip of the display image
  - independent controls for View Port (Main/PIP window) and PIP2 window
  - Rotation function performs a 180° counter-clockwise rotation of the display image
    - independent controls for View Port (Main/PIP window) and PIP2 window
- Alpha Blending
  - Supports alpha blending between the View Port (Main + PIP1) and the PIP2 window
  - 8-bit constant alpha value
  - Dynamic alpha with alpha map
  - Combined with transparency

- Gamma Correction
  - Selectable gamma correction for Main/PIP1/PIP2 windows
  - 2 Gamma Correction Look-up Tables (Bank A and Bank B) using Single Port SRAM
  - Independent color correction for each of RGB components
  - View Port (Main+PIP1 window) can be dynamically switched between LUT banks
  - Async table access
- Pseudo Color Expansion
  - Async table access
  - 2x2 Dither matrix
  - 2x2 FRM
  - Error Diffusion
  - 2-bit color reduction
- Interrupt support
  - Maskable Non-Display (Vsync) interrupt
  - Vsync interrupt assertion can be delayed a configurable number of lines

2.5 Clock Source

- 2 embedded PLLs
  - PLL1 source: BUSCLK, CLKI3, OSCI1/OSCO1, or OSCI2/OSCO2
  - PLL2 source: BUSCLK, CLKI3, OSCI1/OSCO1, or OSCI2/OSCO2
- Two crystal inputs: OSCI1/OSCO1 and OSCI2/OSCO2
- Two digital inputs: BUSCLK, CLKI3
- Clock Outputs: MEMCLK

2.6 Miscellaneous

- Supports maximum 50MHz Internal System Clock
- IRQ output pin
  - IRQ Source (VSYNC, Delayed VSYNC, Etc.)
- PWM: 4 channel for backlight control
- Software initiated power save mode
- Clocks are dynamically turned off when modules are not needed
- General Purpose Input/Output pins are available
- Operating system independent
- Extended Temperature Range: -40 to 85°
- Power Supplies:
  - IO operates at 3.3 volts ± 0.3V
  - Core operates at 1.8 volts ± 0.15V
- Package Type:
  - QFP22 208-pin package (28 x 28 x 1.4 mm, Pin pitch: 0.5 mm)

Chapter 3 System Diagram

The following diagram is an example of a typical system implementation. For detailed pin descriptions and pin mapping, refer to Section Chapter 5, “Pins” on page 14.

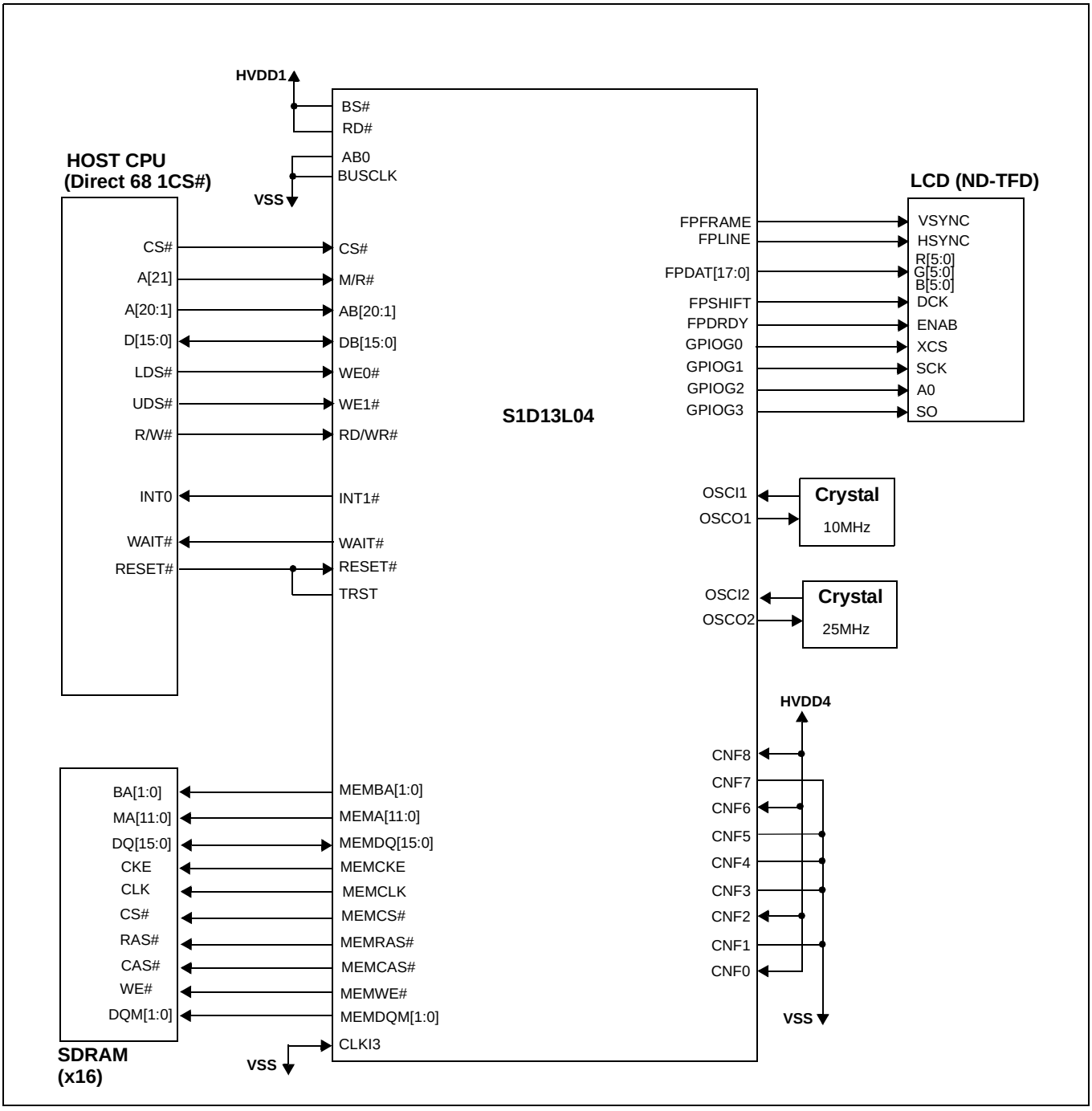

Figure 3-1: Example System Diagram

Chapter 4 Block Diagram

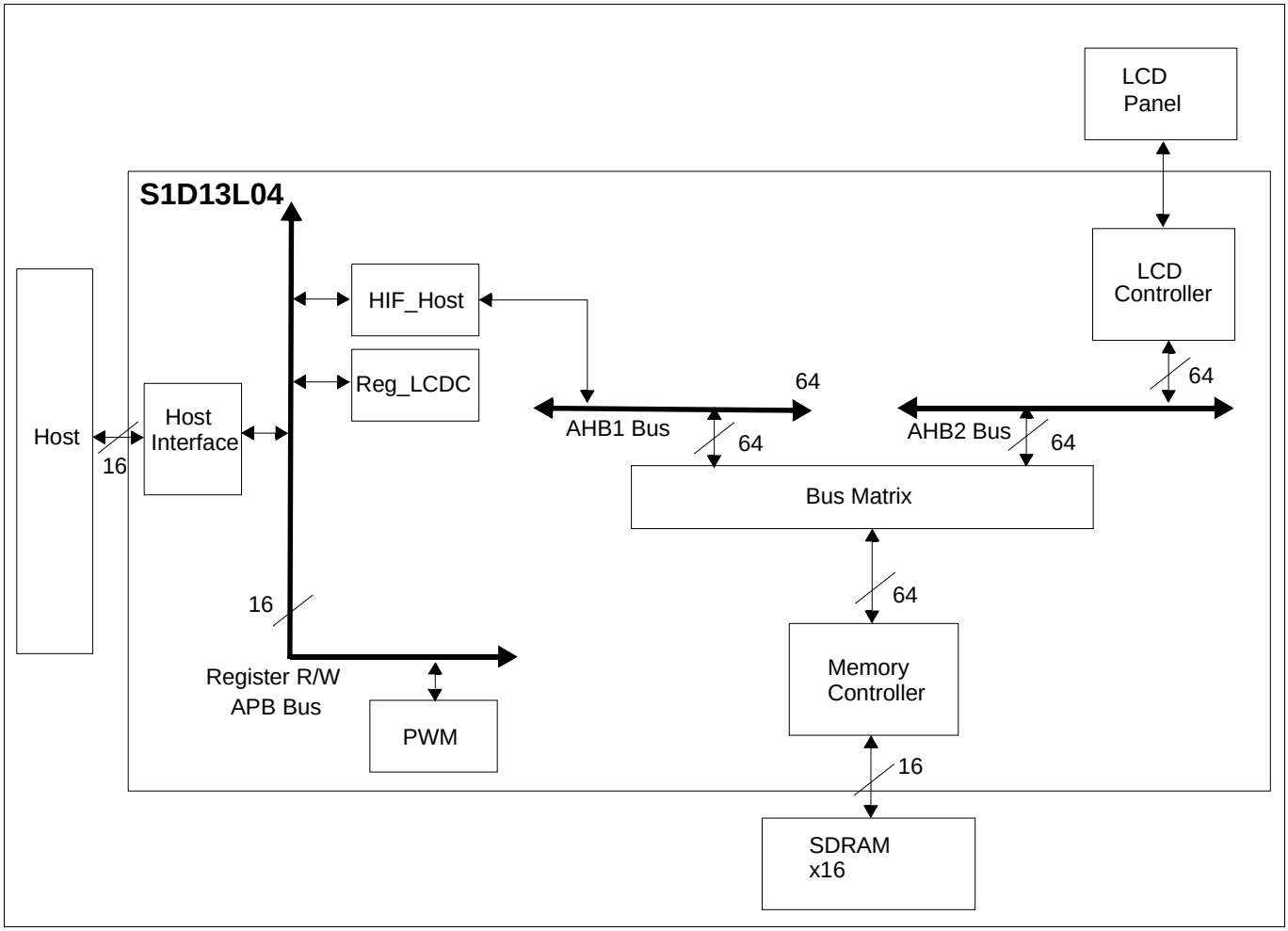

Figure 4-1: Block Diagram

Chapter 5 Pins

The S1D13L04 is available in following package format:

- QFP22 208-pin

5.1 S1D13L04 Pinout Diagrams

5.1.1 QFP22 208-pin Pinout

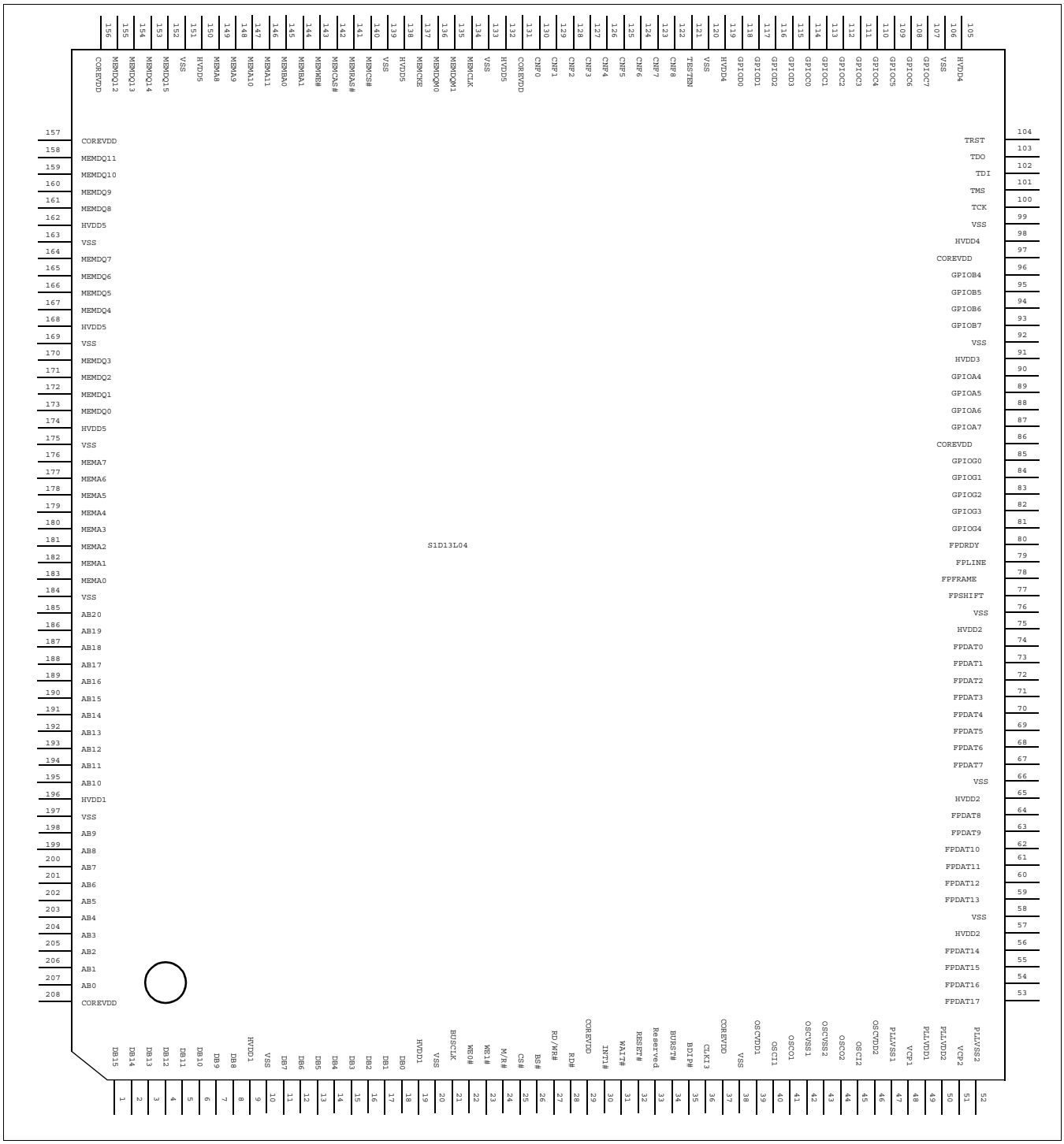

Figure 5-1: QFP22-208 Pinout

5.2 Pin Description

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

H	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 5-1: Cell Descriptions

Cell	Description
ILTR	Low voltage transparent input
OLTR	Low voltage transparent output
IC	LVCMOS input
ICD1	LVCMOS input with pull-down resistor (50kΩ@3.3V)
ICD2	LVCMOS input with pull-down resistor (100kΩ@3.3V)
ICU1	LVCMOS input with pull-up resistor (50kΩ@3.3V)
ICS	LVCMOS schmitt input
ICSD1	LVCMOS schmitt input with pull-down resistor (50kΩ@3.3V)
ICSP1	LVCMOS schmitt input with pull-up resistor (50kΩ@3.3V)
ICSP2	LVCMOS schmitt input with pull-up resistor (100kΩ@3.3V)
OTLN4	Low noise output buffer (4mA@3.3V, deltaV = 0.4V)
OTLN8	Low noise output buffer (8mA@3.3V, deltaV = 0.4V)
BLNC4D1	Low noise LVCMOS IO buffer (4mA@3.3V) with pull-down resistor (50kΩ@3.3V)
BLNC4D2	Low noise LVCMOS IO buffer (4mA@3.3V) with pull-down resistor (100kΩ@3.3V)
BLNC4P1	Low noise LVCMOS IO buffer (4mA@3.3V) with pull-up resistor (50kΩ@3.3V)
BLNCS4D1	Low noise LVCMOS schmitt IO buffer (4mA@3.3V) with pull-down resistor (50kΩ@3.3V)
P	Power

5.2.1 Host Interface

Many of the host interface pins have different functions depending on the host bus interface that is selected using the CNF[6:0] pins (see Section 5.3, “Summary of Configuration Options” on page 29). To determine the pin mapping and pin functions for each host bus interface, refer to Table 5-9:, “Host Bus Interface Pin Mapping (Direct Interfaces),” on page 31, and Table 5-10:, “Host Bus Interface Pin Mapping (Indirect Interfaces),” on page 32.

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
AB[20:0]	I	185-195, 198-207	ICD1	HVDD1	Z	These input pins are System Address pins 20-0. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
DB[15:0]	IO	1-8,11-18	BLNC4D1	HVDD1	Z	These input/output pins are System Data Bus pins 15-0. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
CS#	I	25	ICU1	HVDD1	Z	This input pin is Chip Select and has multiple functions configured according to the Host Bus Interface selected using CNF[4:0]. • For 1 CS# mode, this pin inputs the chip select signal (CS#). • For 2 CS# mode, this pin inputs the memory chip select signal (CSM#). • When the Serial Host Interface is selected, this pin is the Serial Host Chip Select (SCS#). For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
M/R#	I	24	ICU1	HVDD1	Z	This input pin has multiple functions. • For 1 CS# mode, this pin selects between the display buffer and register address spaces. When M/R# is set high, the display buffer is accessed and when M/R# is set low the registers are accessed. • For 2 CS# mode, this pin inputs the register chip select (CSR#). • For Indirect Host Bus Interfaces and Serial Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected. • For Serial Host Bus Interfaces, the internal pull-down resistor is enabled and this pin must be left unconnected. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
RD#	I	28	ICU1	HVDD1	Z	This input pin has multiple functions. • For the Direct/Indirect 68 interface, this pin must be connected to VDD. • For the Direct/Indirect 80 Type 1 and Type 2 interfaces, this pin is the read enable signal (RD#). • For detailed pin functions for all other interfaces, refer to the Specification for each Host. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
RD/WR#	I	27	ICU1	HVDD1	Z	This input pin has multiple functions. • For the Direct/Indirect 68 interface, this pin is the read/write signal (R/W#). • For the Direct/Indirect 80 Type 1 interface, this pin is the write enable signal (WE#). • For the Direct/Indirect 80 Type 2 interface, this pin must be connected to VDD. • For detailed pin functions for all other interfaces, refer to the Specification for each Host. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
WE0#	I	22	ICU1	HVDD1	Z	This input pin has multiple functions. • For the Direct/Indirect 68 interface, this pin is the lower data strobe (LDS#). • For the Direct/Indirect 80 Type 1 interface, this pin is the lower byte enable signal (LBE#). • For the Direct/Indirect 80 Type 2 interface, this pin is the lower byte write enable signal (WEL#). • For detailed pin functions for all other interfaces, refer to the Specification for each Host. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
WE1#	IO	23	BLNC4P1	HVDD1	Z	This input/output pin has multiple functions. • For the Direct/Indirect 68 interface, this pin is the upper data strobe (UDS#). • For the Direct/Indirect 80 Type 1 interface, this pin is the upper byte enable signal (UBE#). • For the Direct/Indirect 80 Type 2 interface, this pin is the upper byte write enable signal (WEU#). • For detailed pin functions for all other interfaces, refer to the Specification for each Host. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
BS#	I	26	ICU1	HVDD1	Z	This input pin has multiple functions. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
BURST#	I	34	ICU1	HVDD1	Z	This pin must be left unconnected.
BDIP#	I	35	ICU1	HVDD1	Z	This pin must be left unconnected.
WAIT#	O	31	OTLN4	HVDD1	Z	During a data transfer, this output pin is driven active to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to the high impedance state after the data transfer is complete. The active polarity is configured according to the Host Bus Interface selected using CNF[4:0]. For detailed pin functions for each host bus interface, see Section 5.4, “Host Bus Interface Pin Mapping” on page 31.
RESET#	I	32	ICS	HVDD1	1	This active low input sets all internal registers to their default state and to force all signals to their inactive states. **Note:** For details on RESET# timing, refer to Section 7.3, “RESET# Timing” on page 43 and Section 7.2, “Power Supply Sequence” on page 41.
BUSCLK	I	21	ICU1	HVDD1	Z	This pin is typically used for clock input for serial host interface. Or it can be used for SDRAM or LCD.Clock input through PLL1 or PLL2. When it is not used, it should be connected to VSS. For details on the S1D13L04 clock structure, refer to Section Chapter 9, “Clocks” on page 69.
INT1#	O	30	OTLN4	HVDD1	Z	This output pin is the primary IRQ output from the S1D13L04. When enabled (REG[002Ah] bit 15 = 1b), it can output all internal IRQ requests to the Host. The output and polarity is configurable using REG[002Ah].

5.2.2 LCD Interface

For a pin mapping summary for each panel type, refer to Table 5-11:, “LCD Interface Pin Mapping for TFT Panels,” on page 33.

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Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
FPDAT[17:0]	O	53-56, 59-64,67-74	OTLN4	HVDD2	L	These output pins are Panel Data bits 17-0. For a summary of pin usage for each panel type, see Section 5.5, “LCD Interface Pin Mapping” on page 33.
FPFRAME	O	78	OTLN4	HVDD2	L	This output pin is Frame Pulse for the LCD panel.
FPLINE	O	79	OTLN4	HVDD2	L	This output pin is Line Pulse for the LCD panel.
FPSHIFT	O	77	OTLN4	HVDD2	L	This output pin is Shift Clock for the LCD panel.
FPDRDY	O	80	OTLN4	HVDD2	L	This output pin has the following function. • Display Enable (DRDY) for TFT panels
GPIOG4	IO	81	BLNCS4D1	HVDD2	0	This input/output pin has multiple functions. • When REG[0C1Ah] bits 9-8 = 00b, this pin is configured as a general purpose input. (default) • REG[0C1Ah] bits 9-8 = 01b is reserved and shouldn’t be set to this value. • When REG[0C1Ah] bits 9-8 = 10b, this pin is configured as a general purpose output. • When REG[0C1Ah] bits 9-8 = 11b, this pin is used for TFT panels with a serial command interface (see Table 5-11:, “LCD Interface Pin Mapping for TFT Panels,” on page 33). Note: This pin has an internal pull-down resistor that is controlled using REG[0468h] bit 4.
GPIOG3	IO	82	BLNCS4D1	HVDD2	0	This input/output pin has multiple functions. • When REG[0C1Ah] bits 7-6 = 00b, this pin is configured as a general purpose input. (default) • REG[0C1Ah] bits 7-6 = 01b is reserved and shouldn’t be set to this value. • When REG[0C1Ah] bits 7-6 = 10b, this pin is configured as a general purpose output. • When REG[0C1Ah] bits 7-6 = 11b, this pin is used for TFT panels with a serial command interface (see Table 5-11:, “LCD Interface Pin Mapping for TFT Panels,” on page 33). Note: This pin has an internal pull-down resistor that is controlled using REG[0468h] bit 3.

Table 5-3: LCD Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIOG2	IO	83	BLNCS4D1	HVDD2	0	This input/output pin has multiple functions. • When REG[0C1Ah] bits 5-4 = 00b, this pin is configured as a general purpose input. (default) • REG[0C1Ah] bits 5-4 = 01b is reserved and shouldn't be set to this value. • When REG[0C1Ah] bits 5-4 = 10b, this pin is configured as a general purpose output. • When REG[0C1Ah] bits 5-4 = 11b, this pin is used for TFT panels with a serial command interface (see Table 5-11:, "LCD Interface Pin Mapping for TFT Panels," on page 33). Note: This pin has an internal pull-down resistor that is controlled using REG[0468h] bit 2.
GPIOG1	IO	84	BLNCS4D1	HVDD2	0	This input/output pin has multiple functions. • When REG[0C1Ah] bits 3-2 = 00b, this pin is configured as a general purpose input. (default) • REG[0C1Ah] bits 3-2 = 01b is reserved and shouldn't be set to this value. • When REG[0C1Ah] bits 3-2 = 10b, this pin is configured as a general purpose output. • When REG[0C1Ah] bits 3-2 = 11b, this pin is used for TFT panels with a serial command interface (see Table 5-11:, "LCD Interface Pin Mapping for TFT Panels," on page 33). Note: This pin has an internal pull-down resistor that is controlled using REG[0468h] bit 1.
GPIOG0	IO	85	BLNCS4D1	HVDD2	0	This input/output pin has multiple functions. • When REG[0C1Ah] bits 1-0 = 00b, this pin is configured as a general purpose input. (default) • REG[0C1Ah] bits 1-0 = 01b is reserved and shouldn't be set to this value,. • When REG[0C1Ah] bits 1-0 = 10b, this pin is configured as a general purpose output. • When REG[0C1Ah] bits 1-0 = 11b, this pin is used for TFT panels with a serial command interface (see Table 5-11:, "LCD Interface Pin Mapping for TFT Panels," on page 33). Note: This pin has an internal pull-down resistor that is controlled using REG[0468h] bit 0.

5.2.3 SDRAM Interface

Table 5-4: SDRAM Interface Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
MEMA[11:0]	O	146-149, 176-183	OTLN4	HVDD5	L	These output pins are used for SDRAM bank row/column address mapping.
MEMBA[1:0]	O	144-145	OTLN4	HVDD5	L	These output pins are used to select the SDRAM Bank Address.
MEMCS#	O	140	OTLN4	HVDD5	H	This output pin is chip select for the SDRAM.
MEMRAS#	O	141	OTLN4	HVDD5	H	This output pin is the RAS# for the SDRAM.
MEMCAS#	O	142	OTLN4	HVDD5	H	This output pin is the CAS# for the SDRAM.
MEMWE#	O	143	OTLN4	HVDD5	H	This output pin is write enable for the SDRAM.
MEMDQ[15:0]	IO	152-155, 158-161, 164-167, 170-173	BLNC4D2	HVDD5	0	These input/output pins are the data bus for the SDRAM. These pins have internal pull-down resistors.
MEMDQM[1:0]	O	135-136	OTLN4	HVDD5	L	These output pins are the byte enables for the SDRAM.
MEMCLK	O	134	OTLN8	HVDD5	H	This output pin is the clock for the SDRAM.
MEMCKE	O	137	OTLN4	HVDD5	H	This output pin is the clock enable for the SDRAM.

5.2.4 GPIO / Multi Function Interface

The S1D13L04 supports many features using the general purpose IO pins. All GPIO pins can be configured, using REG[0C00h] ~ REG[0C1Ah], as an input, output, Non-GPIO function #1, or Non-GPIO function #2, if available. For summary of the functionality for all GPIO pins, see Section 5.6, “GPIO Pin Mapping” on page 34.

Table 5-5: GPIO / Multi Function Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIOA7	IO	87	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C02h] bits 15-14 = 00b, this pin is configured as a general purpose input. (default) • When REG[0C02h] bits 15-14 = 01b, this pin is configured as the PWM Red output (PWMR). • When REG[0C02h] bits 15-14 = 10b, this pin is configured as a general purpose output. • REG[0C02h] bits 15-14 = 11b is reserved and shouldn’t be set to this value. Note: The pull-down resistor on this pin is only active during test mode.
GPIOA6	IO	88	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C02h] bits 13-12 = 00b, this pin is configured as a general purpose input. (default) • When REG[0C02h] bits 13-12 = 01b, this pin is configured as the PWM Green output (PWMG). • When REG[0C02h] bits 13-12 = 10b, this pin is configured as a general purpose output. • REG[0C02h] bits 13-12 = 11b is reserved and shouldn’t be set to this value. Note: The pull-down resistor on this pin is only active during test mode.
GPIOA5	IO	89	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C02h] bits 11-10 = 00b, this pin is configured as a general purpose input. (default) • When REG[0C02h] bits 11-10 = 01b, this pin is configured as the PWM Blue output (PWMB). • When REG[0C02h] bits 11-10 = 10b, this pin is configured as a general purpose output. • REG[0C02h] bits 11-10 = 11b is reserved and shouldn’t be set to this value. Note: The pull-down resistor on this pin is only active during test mode.

Table 5-5: GPIO / Multi Function Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIOA4	IO	90	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C02h] bits 9-8 = 00b, this pin is configured as a general purpose input. (default) • REG[0C02h] bits 9-8 = 01b is reserved and shouldn't be set to this value.. • When REG[0C02h] bits 9-8 = 10b, this pin is configured as a general purpose output. • REG[0C02h] bits 9-8 = 11b is reserved and shouldn't be set to this value. Note: The pull-down resistor on this pin is only active during test mode.
GPIOB7	IO	93	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C06h] bits 15-14 = 00b, this pin is configured as a general purpose input. (default) • When REG[0C06h] bits 15-14 = 01b, this pin is configured as the PWM White output (PWMW). • When REG[0C06h] bits 15-14 = 10b, this pin is configured as a general purpose output. • REG[0C06h] bits 15-14 = 11b is reserved and shouldn't be set to this value. Note: The pull-down resistor on this pin is only active during test mode.
GPIOB6	IO	94	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C06h] bits 13-12 = 00b, this pin is configured as a general purpose input. (default) • REG[0C06h] bits 13-12 = 01b is reserved and shouldn't be set to this value. • When REG[0C06h] bits 13-12 = 10b, this pin is configured as a general purpose output. • When REG[0C06h] bits 13-12 = 11b, this pin is reserved. Note: The pull-down resistor on this pin is only active during test mode.
GPIOB5	IO	95	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C06h] bits 11-10 = 00b, this pin is configured as a general purpose input. (default) • REG[0C06h] bits 11-10 = 01b is reserved and shouldn't be set to this value. • When REG[0C06h] bits 11-10 = 10b, this pin is configured as a general purpose output. • When REG[0C06h] bits 11-10 = 11b, this pin is reserved. Note: The pull-down resistor on this pin is only active during test mode.

Table 5-5: GPIO / Multi Function Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIOB4	IO	96	BLNCS4D1	HVDD3	Z	This pin has multiple functions. • When REG[0C06h] bits 9-8 = 00b, this pin is configured as a general purpose input. (default) • REG[0C06h] bits 9-8 = 01b is reserved and shouldn't be set to this value. • When REG[0C06h] bits 9-8 = 10b, this pin is configured as a general purpose output. • When REG[0C06h] bits 9-8 = 11b, this pin is reserved. Note: The pull-down resistor on this pin is only active during test mode.
GPIOC[7:0]	IO	107-114	BLNCS4D1	HVDD4	0	These pins have multiple functions. • When the appropriate bits from REG[0C0Ah] are set to 00b, the corresponding pins are configured as general purpose inputs. (default) • Appropriate bits from REG[0C0Ah] bits 7-0 shouldn't be set to 01b because this setting is reserved. • When the appropriate bits from REG[0C0Ah] are set to 10b, the corresponding pins are configured as general purpose outputs. • Appropriate bits from REG[0C0Ah] bits 7-0 shouldn't be set to 11b because this setting is reserved. Note: These pins have internal pull-down resistors that are controlled using REG[0464h] bits 7-0.
GPIOD3	IO	115	BLNCS4D1	HVDD4	0	This pin has multiple functions. • When REG[0C0Eh] bits 7-6 = 00b, this pin is configured as a general purpose input. (default) • REG[0C0Eh] bits 7-6 = 01b this pin is configured as the Digital audio input for PWM circuit (AUDIN). • When REG[0C0Eh] bits 7-6 = 10b, this pin is configured as a general purpose output. • REG[0C0Eh] bits 7-6 = 11b is reserved and shouldn't be set to this value. Note: This pin has an internal pull-down resistor that is controlled using REG[0464h] bit 11.

Table 5-5: GPIO / Multi Function Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
GPIOD2	IO	116	BLNCS4D1	HVDD4	0	This pin has multiple functions. • When REG[0C0Eh] bits 5-4 = 00b, this pin is configured as a general purpose input. (default) • REG[0C0Eh] bits 5-4 = 01b is reserved and shouldn't be set to this value. • When REG[0C0Eh] bits 5-4 = 10b, this pin is configured as a general purpose output. • REG[0C0Eh] bits 5-4 = 11b is reserved and shouldn't be set to this value. Note: This pin has an internal pull-down resistor that is controlled using REG[0464h] bit 10.
GPIOD1	IO	117	BLNCS4D1	HVDD4	0	This pin has multiple functions. • When REG[0C0Eh] bits 3-2 = 00b, this pin is configured as a general purpose input. (default) • REG[0C0Eh] bits 3-2 = 01b is reserved and shouldn't be set to this value. • When REG[0C0Eh] bits 3-2 = 10b, this pin is configured as a general purpose output. • REG[0C0Eh] bits 3-2 = 11b is reserved and shouldn't be set to this value. Note: This pin has an internal pull-down resistor that is controlled using REG[0464h] bit 9.
GPIOD0	IO	118	BLNCS4D1	HVDD4	0	This pin has multiple functions. • When REG[0C0Eh] bits 1-0 = 00b, this pin is configured as a general purpose input. (default) • REG[0C0Eh] bits 1-0 = 01b is reserved and shouldn't be set to this value. • When REG[0C0Eh] bits 1-0 = 10b, this pin is configured as a general purpose output. • REG[0C0Eh] bits 1-0 = 11b is reserved and shouldn't be set to this value. Note: This pin has an internal pull-down resistor that is controlled using REG[0464h] bit 8.

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5.2.5 Miscellaneous

Table 5-6: Miscellaneous Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	Power	RESET# State	Description
CNF[8:0]	I	122-130	ICD2	HVDD4	0	These inputs are used to configure the S1D13L04 and must be connected to IOVDD or VSS. The states of these pins are latched at RESET#. These pins have internal pull-down resistors which can be disabled by software after reset (see REG[046Eh]). For more information, see Section 5.3, “Summary of Configuration Options” on page 29.
OSCI1	I	40	ILTR	OSCVDD1	0/1	Crystal input. If an external Oscillator circuit or clock generator is used, connect it to this pin. For details on the clock structure, see Section Chapter 9, “Clocks” on page 69.
OSCO1	O	41	OLTR	OSCVDD1	H	Crystal output. If an external Oscillator is used, this pin should be left unconnected. For details on the clock structure, see Section Chapter 9, “Clocks” on page 69.
OSCI2	I	45	ILTR	OSCVDD2	0/1	Crystal input. If an external Oscillator circuit or clock generator is used, connect it to this pin. For details on the clock structure, see Section Chapter 9, “Clocks” on page 69.
OSCO2	O	44	OLTR	OSCVDD2	H	Crystal output. If an external Oscillator is used, this pin should be left unconnected. For details on the clock structure, see Section Chapter 9, “Clocks” on page 69.
CLKI3	I	36	IC	HVDD1	0/1	Clock input. Typically, this input is used for the SDRAM clock through PLL1. When it is not used, it should be connected to VSS.
TESTEN	I	121	ICSD1	HVDD4	0	This input pin is for production test only and should be left unconnected for normal operation.
VCP1	O	48	OLTR	PLLVDD1	Z	This output is for production test only and should be left unconnected for normal operation.
VCP2	O	51	OLTR	PLLVDD2	Z	This output is for production test only and should be left unconnected for normal operation.
TCK	I	100	ICSP1	HVDD4	1	JTAG Interface pin for Boundary Scan test.
TMS	I	101	ICSP1	HVDD4	1	JTAG Interface pin for Boundary Scan test.
TDI	I	102	ICSP1	HVDD4	1	JTAG Interface pin for Boundary Scan test.
TDO	O	103	OTLN4	HVDD4	L	JTAG Interface pin for Boundary Scan test
TRST	I	104	ICSP2	HVDD4	1	JTAG Interface pin for Boundary Scan test. For normal operations, this pin must be tied to VSS or connected to RESET#.

5.2.6 Power And Ground

Table 5-7: Power And Ground Pin Descriptions

Pin Name	Type	QFP Pin#	Cell	RESET# State	Description
COREVDD	P	29,37,86,97, 131,156, 157,208	P	—	Core VDD
HVDD1	P	9,19,196	P	—	IOVDD for HOST interface
HVDD2	P	57,65,75	P	—	IOVDD for LCD Panel interface
HVDD3	P	91	P	—	IOVDD for GPIO
HVDD4	P	98,105,119	P	—	IOVDD for GPIO, etc.
HVDD5	P	132,138, 150,162, 168,174	P	—	IOVDD for SDRAM interface
VSS	P	10,20,38,58, 66,76,92,99, 106,120, 133,139, 151,163, 169,175, 184,197	P	—	Common Ground
OSCVDD1	P	39	P	—	VDD for OSC1
OSCVSS1	P	42	P	—	GND for OSC1
OSCVDD2	P	46	P	—	VDD for OSC2
OSCVSS2	P	43	P	—	GND for OSC2
PLLVDD1	P	49	P	—	Analog VDD for PLL1
PLLVSS1	P	47	P	—	Analog GND for PLL1
PLLVDD2	P	50	P	—	Analog VDD for PLL2
PLLVSS2	P	52	P	—	Analog GND for PLL2

5.3 Summary of Configuration Options

These pins are used for configuration of the S1D13L04 and must be connected using an external pull-up resistor (1) or left open (0) where an internal pull-down resistor is used. The state of CNF[8:0] has an effect only at the rising edge of RESET#. Changing state at any other time has no effect. In order to stop the constant current when an external pull-up resistor is used, disable the corresponding pull-down resistor (see REG[046Eh]).

Note
The CNF pins select the host bus interface and determine whether the interface is Little or Big Endian.

When a Big Endian host interface is selected, the registers must be accessed using a method which “byte-swaps” the upper and lower data byte in each register. For details on this requirement, see Section 16.6, “Register Accesses for Big Endian Host Interfaces” on page 198.

Table 5-8: Summary of Power-On/Reset Options for CNF6=1

<table>
<tr><th>S1D13L04 Configuration Input</th><th colspan="2">Power-On/Reset State</th></tr>
<tr><th></th><th>1 (connected to IO V_{DD})</th><th>0 (connected to V_{SS})</th></tr>
<tr><td>CNF[8:7]</td><td colspan="2">Selects the PLL1 Clock Source as follows:
CNF8 CNF7 PLL1 Clock Source
0 0 CLKI3 Pin
0 1 BUSCLK Pin
1 0 OSC1 Clock
1 1 OSC2 Clock</td></tr>
<tr><td>CNF6</td><td colspan="2">1 (connected to IO V_{DD})</td></tr>
<tr><td>CNF5</td><td>Big Endian (see Note 1)</td><td>Little Endian</td></tr>
<tr><td>CNF[4:0]</td><td colspan="2">Select host bus interface as follows:
CNF4 CNF3 CNF2 CNF1 CNF0 Host Bus
0 0 0 0 0 Parallel Direct 80 Type 2: 1 CS# (see Note 2)
0 0 0 0 1 Reserved
0 0 0 1 0 Parallel Indirect 80 Type 2
0 0 0 1 1 Reserved
0 0 1 0 0 Parallel Direct 80 Type 1: 1 CS#
0 0 1 0 1 Parallel Direct 68: 1 CS#
0 0 1 1 0 Parallel Indirect 80 Type 1
0 0 1 1 1 Parallel Indirect 68
0 1 0 0 0 Parallel Direct 80 Type 2: 2 CS# (see Note 2)
0 1 0 0 1 Reserved
0 1 0 1 0 Reserved
0 1 0 1 1 Reserved
0 1 1 0 0 Parallel Direct 80 Type 1: 2 CS#
0 1 1 0 1 Parallel Direct 68: 2 CS#
0 1 1 1 0 Reserved
0 1 1 1 1 Reserved
1 0 0 0 0 Serial: Data valid on falling edge
1 0 0 0 1 Reserved
1 0 0 1 0 Reserved
1 0 0 1 1 Reserved
1 0 1 0 0 Reserved
1 0 1 0 1 Reserved
1 0 1 1 0 Reserved
1 0 1 1 1 Reserved
1 1 0 0 0 Serial: Data valid on rising edge
1 1 0 0 1 Reserved
1 1 0 1 0 Reserved
1 1 0 1 1 Reserved
1 1 1 0 0 Reserved
1 1 1 0 1 Reserved
1 1 1 1 0 Reserved
1 1 1 1 1 Reserved</td></tr>
</table>

Note

1.When Big Endian mode is selected (CNF5=1), only memory accesses are byte swapped. Register accesses are unaffected.

2.Big Endian mode (CNF5=1) is not supported for Indirect 80, Indirect 68, and Serial interfaces.

3.CNF6=0 is reserved

5.4 Host Bus Interface Pin Mapping

Table 5-9: Host Bus Interface Pin Mapping (Direct Interfaces)

S1D13L04 Pin Name	Direct 68	Direct 80 Type 1	Direct 80 Type 2
AB[20:1]	A[20:1]	A[20:1]	A[20:1]
AB0	Connected to VSS	Connected to VSS	Connected to VSS
DB[15:0]	D[15:0]	D[15:0]	D[15:0]
WE0#	LDS#	LBE#	WEL#
WE1#	UDS#	UBE#	WEU#
M/R#	Address (1CS#), chip/selection	Address (1CS#), chip/selection	Address (1CS#), chip/selection
CS#	CS#	CS#	CS#
BS#	Connected to VDD	Connected to VDD	Connected to VDD
RD/WR#	R/W#	WE#	HVDD1
RD#	HVDD1	RD#	RD#
BUSCLK	Connected to VSS	Connected to VSS	Connected to VSS
INT1#	INT pin at CPU	INT pin at CPU	INT pin at CPU
INT2#	INT pin at CPU	INT pin at CPU	INT pin at CPU
WAIT#	WAIT#	WAIT#	WAIT#
RESET#	RESET#	RESET#	RESET#
BURST#	Unconnected	Unconnected	Unconnected
BDIP#	Unconnected	Unconnected	Unconnected

Table 5-10: Host Bus Interface Pin Mapping (Indirect Interfaces)

S1D13L04 Pin Name	Indirect 68	Indirect 80 Type 1	Indirect 80 Type 2	Serial
AB[20:3]	Unconnected	Unconnected	Unconnected	Unconnected
AB2	A2	A2	A2	Unconnected
AB1	A1	A1	A1	Unconnected
AB0	Connected to VSS	Connected to VSS	Connected to VSS	SA0
DB[15:2	D[15:2]	D[15:2]	D[15:2]	Unconnected
DB1	D1	D1	D1	SO
DB0	D0	D0	D0	SI
WE0#	LDS#	LBE#	WEL#	Unconnected
WE1#	UDS#	UBE#	WEU#	Unconnected
M/R#	Unconnected	Unconnected	Unconnected	Unconnected
CS#	CS#	CS#	CS#	SCS#
BS#	Connected to VDD	Connected to VDD	Connected to VDD	Unconnected
RD/WR#	R/W#	WE#	HVDD1	Unconnected
RD#	HVDD1	RD#	RD#	Unconnected
BUSCLK	Connected to VSS	Connected to VSS	Connected to VSS	SCLK
INT1#	INT pin at CPU	INT pin at CPU	INT pin at CPU	INT pin at CPU
INT2#	INT pin at CPU	INT pin at CPU	INT pin at CPU	INT pin at CPU
WAIT#	WAIT#	WAIT#	WAIT#	Unconnected
RESET#	RESET#	RESET#	RESET#	RESET#
BURST#	Unconnected	Unconnected	Unconnected	Unconnected
BDIP#	Unconnected	Unconnected	Unconnected	Unconnected

5.5 LCD Interface Pin Mapping

Table 5-11: LCD Interface Pin Mapping for TFT Panels

S1D13L04 Pin Name	Color Active (TFT) Panels							
	Generic TFT		ND-TFD		a-Si TFT		TFT with uWire	
	18-bit	16-bit	18-bit	16-bit	18-bit	16-bit	18-bit	16-bit
FPFRAME	VSYNC		VSYNC		VSYNC		VSYNC	
FPLINE	HSYNC		HSYNC		HSYNC		HSYNC	
FPSHIFT	DCK		DCK		DCK		DCK	
FPDRDY	ENAB		ENAB		ENAB		ENAB	
FPDAT0	R5	R4	R5	R4	R5	R4	R5	R4
FPDAT1	R4	R3	R4	R3	R4	R3	R4	R3
FPDAT2	R3	R2	R3	R2	R3	R2	R3	R2
FPDAT3	G5	G5	G5	G5	G5	G5	G5	G5
FPDAT4	G4	G4	G4	G4	G4	G4	G4	G4
FPDAT5	G3	G3	G3	G3	G3	G3	G3	G3
FPDAT6	B5	B4	B5	B4	B5	B4	B5	B4
FPDAT7	B4	B3	B4	B3	B4	B3	B4	B3
FPDAT8	B3	B2	B3	B2	B3	B2	B3	B2
FPDAT9	R2	R1	R2	R1	R2	R1	R2	R1
FPDAT10	R1	R0	R1	R0	R1	R0	R1	R0
FPDAT11	R0	0	R0	0	R0	0	R0	0
FPDAT12	G2	G2	G2	G2	G2	G2	G2	G2
FPDAT13	G1	G1	G1	G1	G1	G1	G1	G1
FPDAT14	G0	G0	G0	G0	G0	G0	G0	G0
FPDAT15	B2	B1	B2	B1	B2	B1	B2	B1
FPDAT16	B1	B0	B1	B0	B1	B0	B1	B0
FPDAT17	B0	0	B0	0	B0	0	B0	0
GPIOG0	GPIOG0		XCS		SSTB		LCDCS	
GPIOG1	GPIOG1		SCK		SCLK		SCLK	
GPIOG2	GPIOG2		A0		driven 0		driven 0	
GPIOG3	GPIOG3		SO		SDATA		SDO	
GPIOG4	GPIOG4		driven 0		driven 0		driven 0	

5.6 GPIO Pin Mapping

The GPIO pins are used for various interfaces supported by the S1D13L04. The following table summarizes the possible uses for each GPIO pin. Selecting certain combinations of interfaces may not be possible due to the fact that they share the same GPIO pin.

Table 5-12: GPIO Pin Mapping Summary

S1D13L04 Pin Name	Controlled By	GPIO Input	Function #1	GPIO Output	Function #2
GPIOA7	REG[0C02h] bits 15-14	00b: GPIOA7	01b: PWMR	10b: GPIOA7	11b: Reserved
GPIOA6	REG[0C02h] bits 13-12	00b: GPIOA6	01b: PWMG	10b: GPIOA6	11b: Reserved
GPIOA5	REG[0C02h] bits 11-10	00b: GPIOA5	01b: PWMB	10b: GPIOA5	11b: Reserved
GPIOA4	REG[0C02h] bits 9-8	00b: GPIOA4	01b: Reserved	10b: GPIOA4	11b: Reserved
GPIOB7	REG[0C06h] bits 15-14	00b: GPIOB7	01b: PWMW	10b: GPIOB7	11b: Reserved
GPIOB6	REG[0C06h] bits 13-12	00b: GPIOB6	01b: Reserved	10b: GPIOB6	11b: Reserved
GPIOB5	REG[0C06h] bits 11-10	00b: GPIOB5	01b: Reserved	10b: GPIOB5	11b: Reserved
GPIOB4	REG[0C06h] bits 9-8	00b: GPIOB4	01b: Reserved	10b: GPIOB4	11b: Reserved
GPIOC[7:0]	REG[0C0Ah] bits 15-0	00: GPIOC[7:0]	01b: Reserved	10: GPIOC[7:0	11b: Reserved
GPIOD3	REG[0C0Eh] bits 7-6	00: GPIOD3	01b: AUDIN	10: GPIOD3	11b: Reserved
GPIOD2	REG[0C0Eh] bits 5-4	00: GPIOD2	01b: Reserved	10: GPIOD2	11b: Reserved
GPIOD1	REG[0C0Eh] bits 3-2	00: GPIOD1	01b: Reserved	10: GPIOD1	11b: Reserved
GPIOD0	REG[0C0Eh] bits 1-0	00: GPIOD0	01b: Reserved	10: GPIOD0	11b: Reserved
GPIOG[4:0][2]	REG[0C1Ah] bits 9-0	00: GPIOG[4:0]	01b: Reserved	10: GPIOG[4:0]	11b: Serial Panel Interface Support

PWM Interface

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5.7 PWM Interface Pin Mapping

The PWM interface shares some of it's GPIO pins with other interfaces. To determine if specific combinations of interfaces are possible, refer to Figure 5.6 "GPIO Pin Mapping" on page 34.

Table 5-13: PWM Interface Pin Mapping

S1D13L04 Pin Name	PWM Signal Name	Description
GPIOA7	PWMR	PWM Red output
GPIOA6	PWMG	PWM Green output
GPIOA5	PWMB	PWM Blue output
GPIOB7	PWMW	PWM White output
GPIOD3	AUDIN	Digital audio input for PWM circuit

Chapter 6 D.C. Characteristics

Note
1.When applying supply voltages to the S1D13L04, Core V_{DD} must be applied to the chip before, or simultaneously with H V_{DD}, or damage to the chip may result.
2. Core V_{DD}, OSC V_{DD}, and PLL V_{DD} must be equal to or lower than H V_{DD}.

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Supply Voltage	V_{SS} - 0.3 to 2.5	V
H V_{DD}	Supply Voltage	V_{SS} - 0.3 to 4.0	V
OSC V_{DD}	Supply Voltage	V_{SS} - 0.3 to 2.1	V
PLL V_{DD}	Supply Voltage	V_{SS} - 0.3 to 2.1	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to H V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to H V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-65 to 150	° C

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	1.65	1.8	1.95	V
H V_{DD1}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
H V_{DD2}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
H V_{DD3}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
H V_{DD4}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
H V_{DD5}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
OSC V_{DD1}	Supply Voltage	V_{SS} = 0 V	1.65	1.8	1.95	V
OSC V_{DD2}	Supply Voltage	V_{SS} = 0 V	1.65	1.8	1.95	V
PLL V_{DD1}	Supply Voltage	V_{SS} = 0 V	1.65	1.8	1.95	V
PLL V_{DD2}	Supply Voltage	V_{SS} = 0 V	1.65	1.8	1.95	V
V_{IN}	Input Voltage	OSCI1, OSCI2	V_{SS}	—	Core V_{DD}	V
		Other IO Pins	V_{SS}	—	IO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3: Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions		150		µA
I_{IZ}	Input Leakage Current	V_I = 0V or V_{DD}	-5	—	5	µA
I_{OZ}	Output Leakage Current	V_O = 0V or V_{DD}	-5	—	5	µA
I_{OH2}	High Level Output Current	V_{OH} = H V_{DD} - 0.4V	-4	—	—	mA
I_{OH3}	High Level Output Current	H V_{DD} = min	-8	—	—	mA
I_{OL2}	Low Level Output Current	V_{OL} = 0.4V	4	—	—	mA
I_{OL3}	Low Level Output Current	H V_{DD} = min	8	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS level, H V_{DD} = max	2.2	—	H V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS level, H V_{DD} = min	-0.3	—	0.8	V
VT_+	Positive Trigger Voltage	LVCMOS Schmitt	1.4	—	2.7	V
VT_-	Negative Trigger Voltage	LVCMOS Schmitt	0.6	—	1.8	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.3	—	—	V
R_{PU}	Pull-up Resistance	V_I = 0V, Type 1	25	50	120	kΩ
		V_I = 0V, Type 2	50	100	240	kΩ
R_{PD}	Pull-down Resistance	V_I = H V_{DD}, Type 1	25	50	120	kΩ
		V_I = H V_{DD}, Type 2	50	100	240	kΩ
C_I	Input Pin Capacitance	F = 1MHz, H V_{DD} = 0V	—	—	8	pF
C_O	Output Pin Capacitance	F = 1MHz, H V_{DD} = 0V	—	—	8	pF
C_{IO}	Bi-Directional Pin Capacitance	F = 1MHz, H V_{DD} = 0V	—	—	8	pF

Chapter 7 A.C. Characteristics

Conditions: IO V_{DD} = 3.3V ± 10%
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be $\leq$ 5 ns (10% ~ 90%)
C_L = 50pF (CPU Interface), unless noted
C_L = 0pF (LCD Panel Interface)
C_L = 15pF (Display Memory Interface)

7.1 Clock Timing

7.1.1 Input Clocks

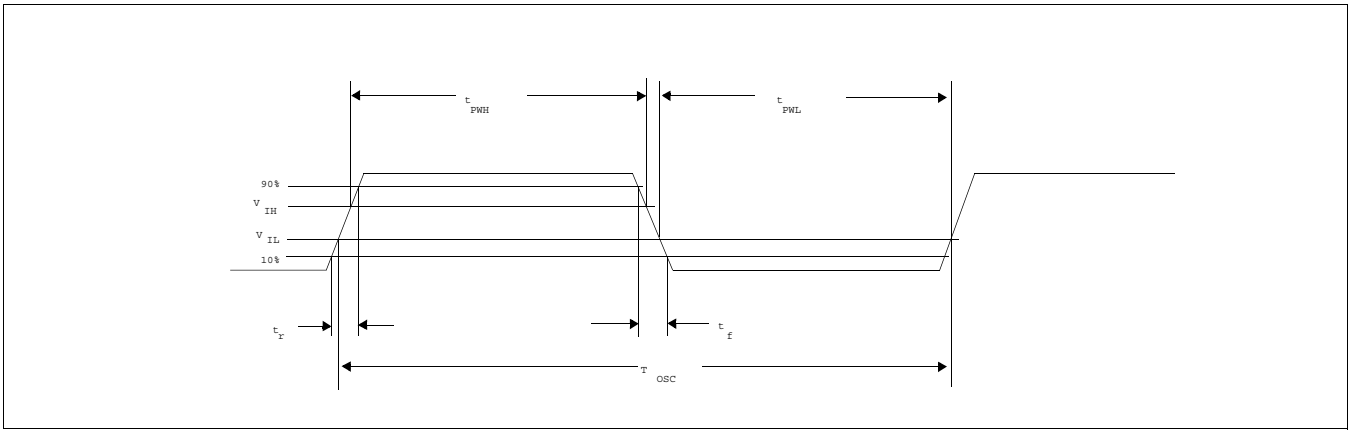

Figure 7-1: Clock Requirements for OSC1/OSC2/CLKI3/BUSCLK

Table 7-1: Clock Requirements for OSC1/OSC2/CLKI3/BUSCLK when used as Clock Input

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC1}	Input Clock Frequency for OSC1	5	—	65	MHz
T_{OSC1}	Input Clock Period for OSC1	—	$1/f_{OSC1}$	—	ns
f_{OSC2}	Input Clock Frequency for OSC2	5	—	27	MHz
T_{OSC2}	Input Clock Period for OSC2	—	$1/f_{OSC2}$	—	ns
f_{CLKI3}	Input Clock Frequency for CLKI3	5	—	100	MHz
T_{CLKI3}	Input Clock Period for CLKI3	—	$1/f_{CLKI3}$	—	ns
t_{PWH}	Input Clock Pulse Width High	0.4	—	0.6	T_{OSC}
t_{PWL}	Input Clock Pulse Width Low	0.4	—	0.6	T_{OSC}
t_f	Input Clock Fall Time (10% - 90%)	—	—	0.2	T_{OSC}
t_r	Input Clock Rise Time (10% - 90%)	—	—	0.2	T_{OSC}

Note
If a host interface that uses BUSCLK is selected (CNF6=0), BUSCLK must remain on continuously while the S1D13L04 is in normal operation mode.

Table 7-2: Clock Requirements for OSC1/OSC2 when used as Crystal Oscillator Input

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC1}	Input Clock Frequency for OSC1	5	—	20	MHz
T_{OSC1}	Input Clock Period for OSC1	—	$1/f_{OSC1}$	—	ns
f_{OSC2}	Input Clock Frequency for OSC2	5	—	27	MHz
T_{OSC2}	Input Clock Period for OSC2	—	$1/f_{OSC2}$	—	ns
t_{PWH}	Input Clock Pulse Width High	0.4	—	0.6	T_{OSC}
t_{PWL}	Input Clock Pulse Width Low	0.4	—	0.6	T_{OSC}
t_f	Input Clock Fall Time (10% - 90%)	—	—	0.2	T_{OSC}
t_r	Input Clock Rise Time (10% - 90%)	—	—	0.2	T_{OSC}

Note
The maximum allowable clock jitter is 300 ps.

7.1.2 Internal Clocks

The following section provides min/max values for some of the S1D13L04 internal clocks. For further information on the internal clocks, refer to Section Chapter 9, “Clocks” on page 69.

Table 7-3: Internal Clock Requirements

Symbol	Parameter	Min	Max	Units
$f_{SDRAMCLK}$	SDRAM Clock Frequency	—	100	MHz
f_{SYSCLK}	System Clock Frequency	20	50	MHz

7.1.3 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

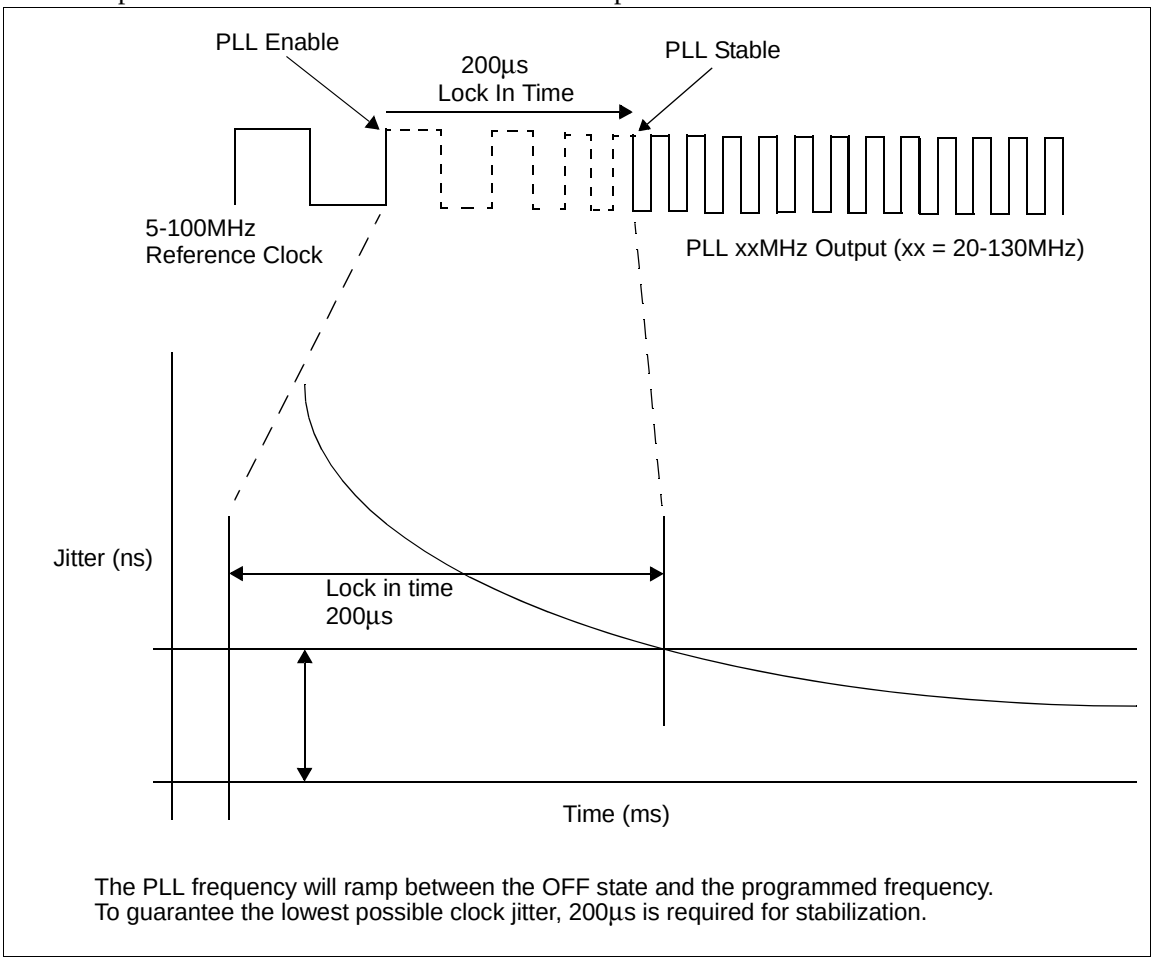

Figure 7-2: PLL Start-Up Time

Table 7-4: PLL Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{PLL}	PLL output clock frequency	20	130	MHz
t_{PStal}	PLL output stable time	—	200	µs

7.2 Power Supply Sequence

7.2.1 Power Supply Structure

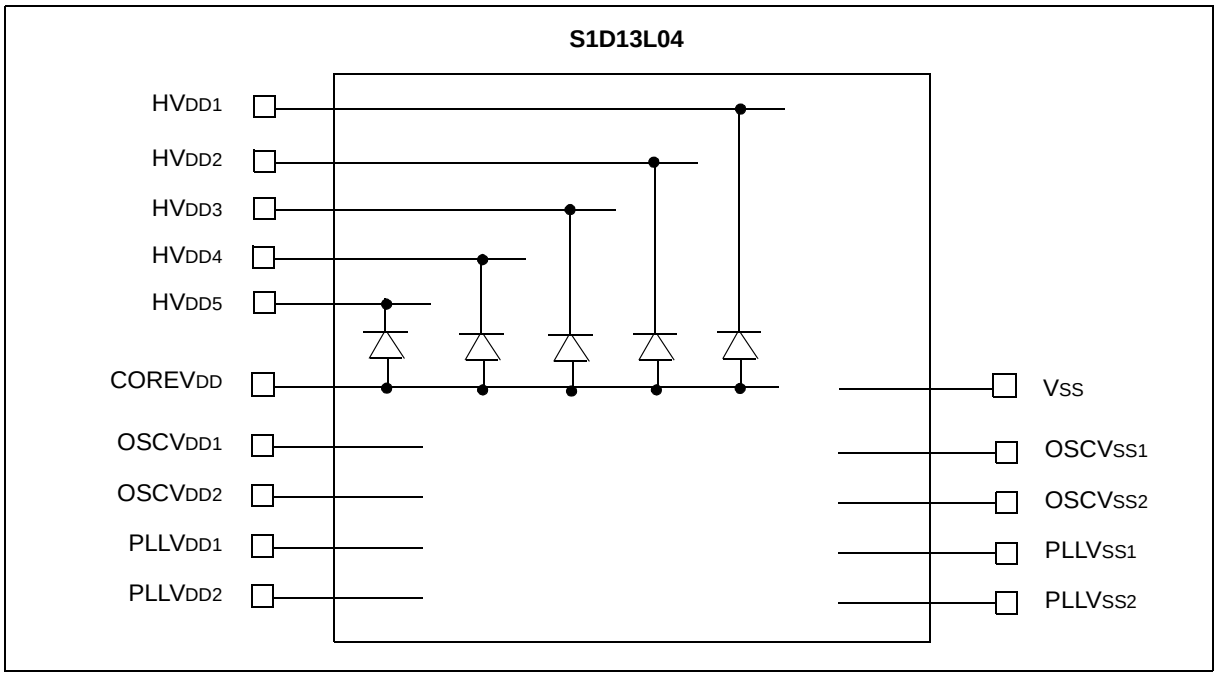

Figure 7-3: Internal Power Structure

7.2.2 Power-On Sequence

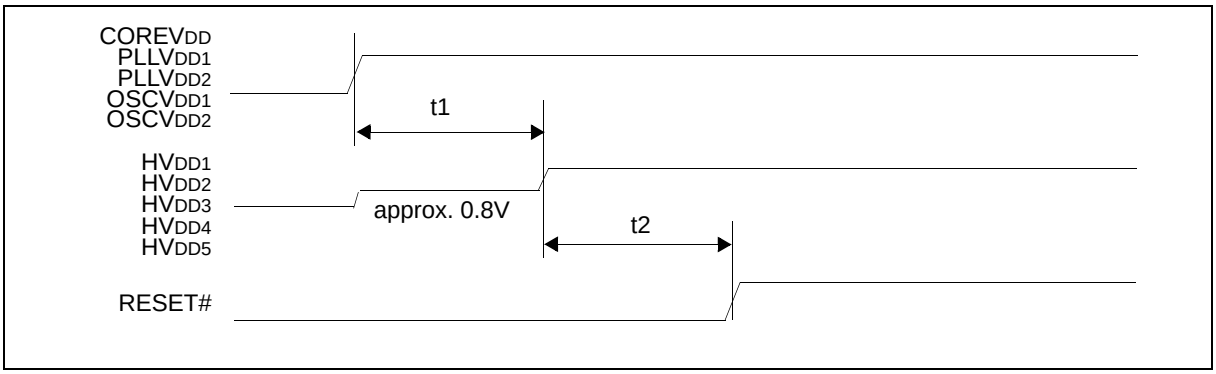

Figure 7-4: Power-On Sequence

Table 7-5: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	HV_{DD1} ~ HV_{DD5} on delay from $COREV_{DD}$, $OSCV_{DD1}$, $OSCV_{DD2}$, $PLLV_{DD1}$, $PLLV_{DD2}$ on	0	500	ms
t2	RESET# deasserted from HV_{DD1} ~ HV_{DD5} on	50	—	ns

7.2.3 Power-Off Sequence

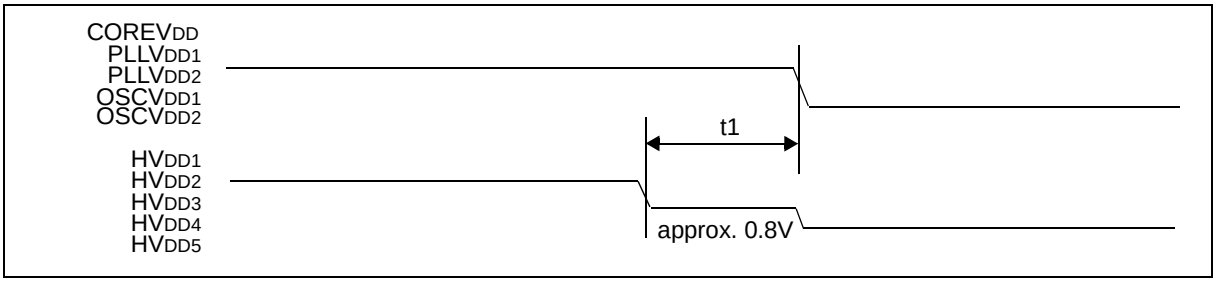

Figure 7-5: Power-Off Sequence

Table 7-6: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	$COREV_{DD}$, $OSCV_{DD1}$, $OSCV_{DD2}$, $PLLV_{DD1}$, $PLLV_{DD2}$ off delay from HV_{DD1} ~ HV_{DD5} off	0	500	ms

7.3 RESET# Timing

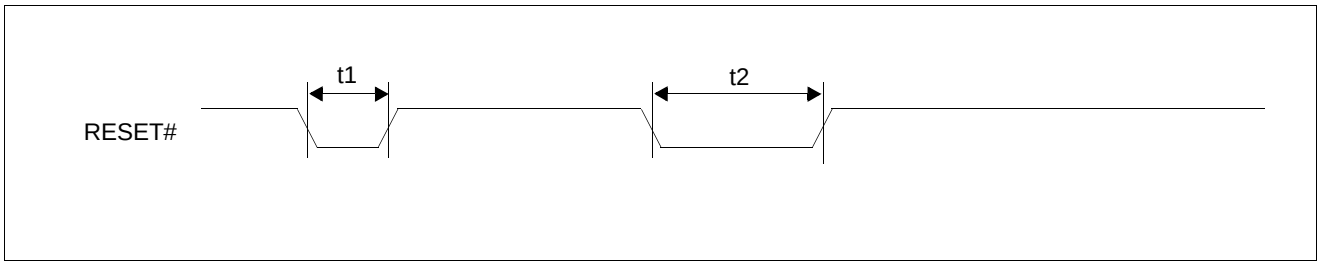

Figure 7-6: S1D13L04 RESET# Timing

Table 7-7: S1D13L04 RESET# Timing

Symbol	Parameter	Min	Max	Units
t1	Reset Pulse Width to be ignored	—	2	ns
t2	Active Reset Pulse Width	50	—	ns

7.4 Host Bus Interface Timing

7.4.1 Direct/Indirect 80 Type 1

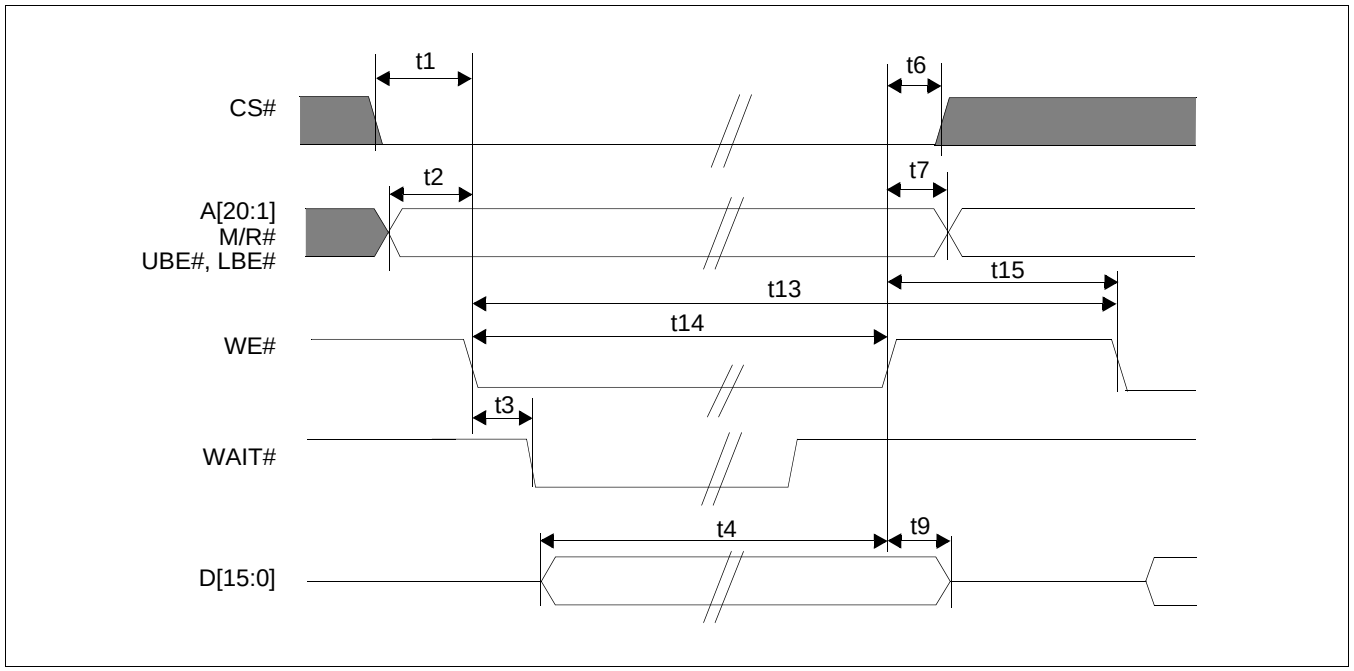

Figure 7-7: Direct/Indirect 80 Type 1 Host Interface Write Timing

Table 7-8: Direct/Indirect 80 Type 1 Host Interface Write Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to WE# falling edge	5	—	ns
t2	A[20:1], M/R#, UBE#, LBE# setup time to WE# falling edge	5	—	ns
t3	WE# falling edge to WAIT# driven low	—	19	ns
t4	D[15:0] setup time to WE# rising edge	15	—	ns
t6	WE# rising edge to CS# hold time	4	—	ns
t7	WE# rising edge to A[20:1], M/R#, UBE#, LBE# hold time	4	—	ns
t9	D[15:0] hold time from WE# rising edge	5	—	ns
t13	WE# cycle time	4.5	—	Ts (Note 1)
t14	WE# pulse active time	3	—	Ts
t15	WE# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

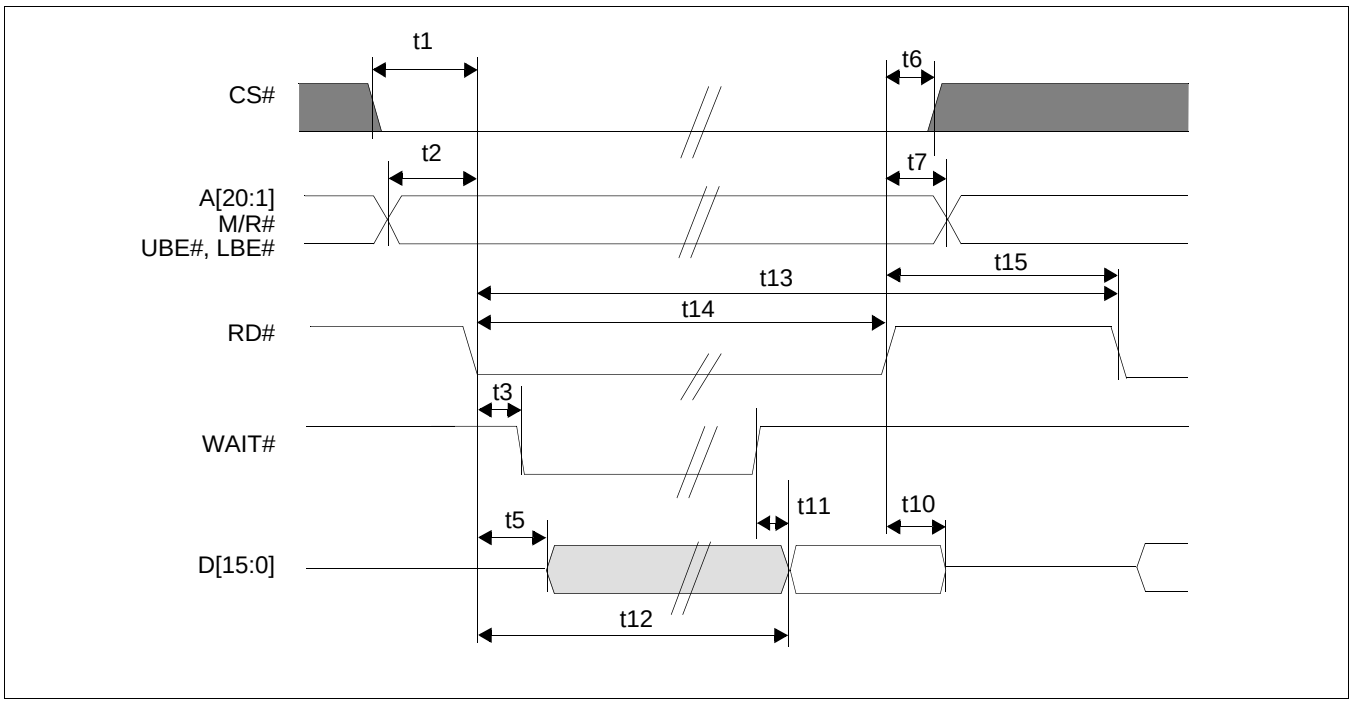

Figure 7-8: Direct/Indirect 80 Type 1 Host Interface Read Timing

Table 7-9: Direct/Indirect 80 Type 1 Host Interface Read Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to RD# falling edge	5	—	ns
t2	A[20:1], M/R#, UBE#, LBE# setup time to RD# falling edge	5	—	ns
t3	RD# falling edge to WAIT# driven low	—	19	ns
t5	RD# falling edge to D[15:0] driven	4	—	ns
t6	RD# rising edge to CS# hold time	4	—	ns
t7	RD# rising edge to A[20:1], M/R#, UBE#, LBE# hold time	4	—	ns
t10	D[15:0] hold time from RD# rising edge	1	10	ns
t11	WAIT# rising edge to valid DATA if WAIT# asserted	—	10	ns
t12	RD# falling edge to valid Data if WAIT# is NOT asserted	—	20	ns
t13	RD# cycle time	4.5	—	Ts (Note 1)
t14	RD# pulse active time	3	—	Ts
t15	RD# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

7.4.2 Direct/Indirect 80 Type 2

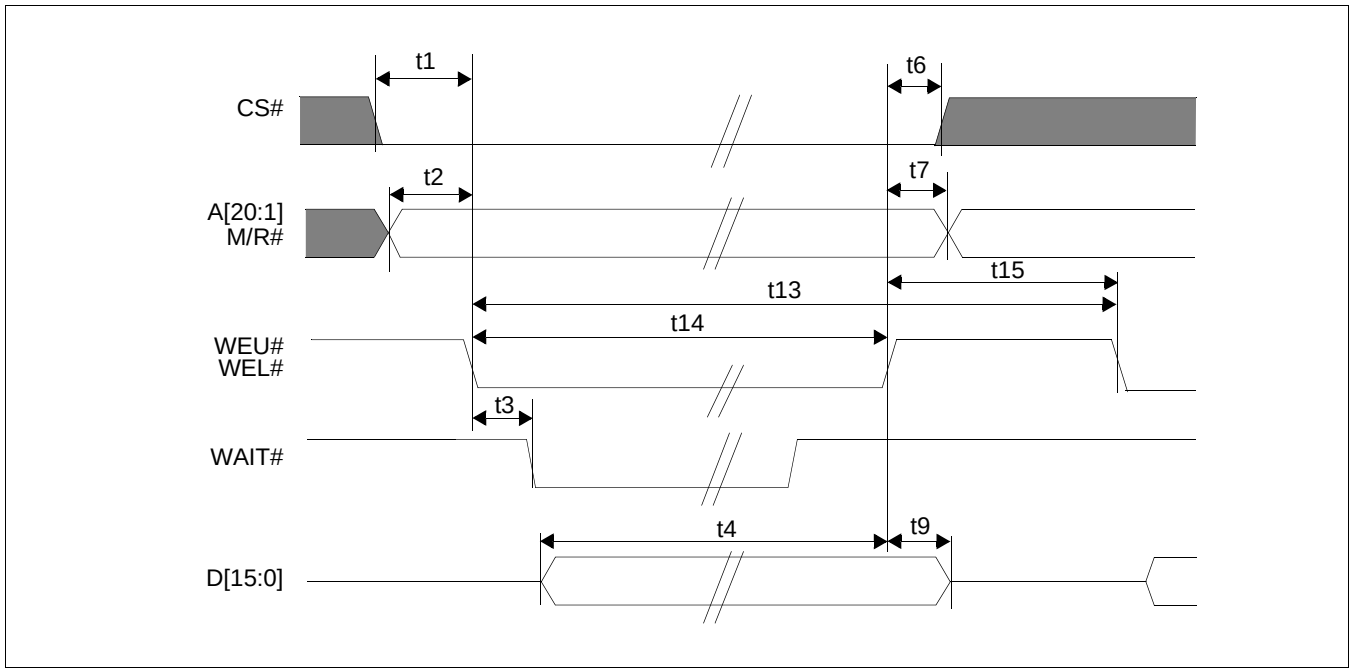

Figure 7-9: Direct/Indirect 80 Type 2 Host Interface Write Timing

Table 7-10: Direct/Indirect 80 Type 2 Host Interface Write Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to WEU#, WEL# falling edge	9	—	ns
t2	A[20:1], M/R# setup time to WEU#, WEL# falling edge	9	—	ns
t3	WEU#, WEL# falling edge to WAIT# driven low	—	19	ns
t4	D[15:0] setup time to WEU#, WEL# rising edge	15	—	ns
t6	WEU#, WEL# rising edge to CS# hold time	4	—	ns
t7	WEU#, WEL# rising edge to A[20:1], M/R# hold time	4	—	ns
t9	D[15:0] hold time from WEU#, WEL# rising edge	5	—	ns
t13	WEU#, WEL# cycle time	4.5	—	Ts (Note 1)
t14	WEU#, WEL# pulse active time	3	—	Ts
t15	WEU#, WEL# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

Note
Big Endian Mode (CNF5=1) is not supported for Direct 80 Type 2 interfaces.

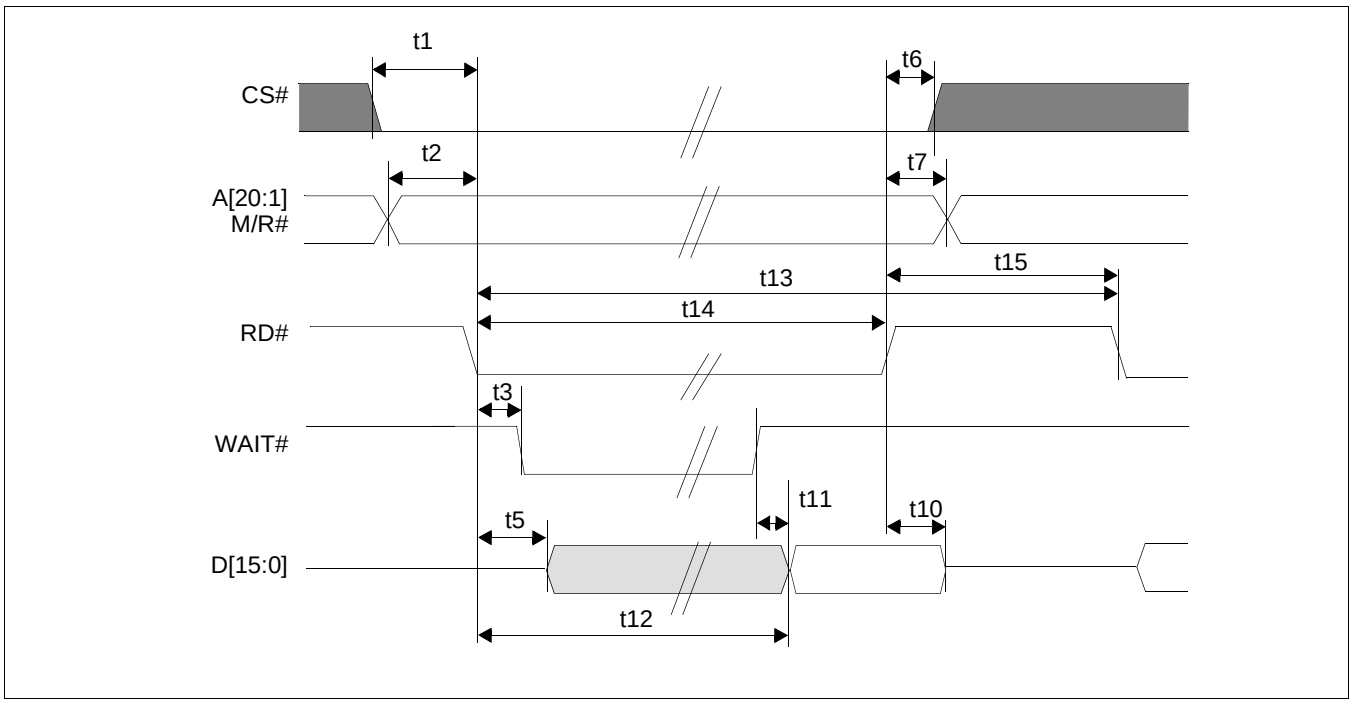

Figure 7-10: Direct/Indirect 80 Type 2 Host Interface Read Timing

Table 7-11: Direct/Indirect 80 Type 2 Host Interface Read Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to RD# falling edge	9	—	ns
t2	A[20:1], M/R# setup time to RD# falling edge	9	—	ns
t3	RD# falling edge to WAIT# driven low	—	19	ns
t5	RD# falling edge to D[15:0] driven	4	—	ns
t6	RD# rising edge to CS# hold time	4	—	ns
t7	RD# rising edge to A[20:1], M/R# hold time	4	—	ns
t10	D[15:0] hold time from RD# rising edge	1	10	ns
t11	WAIT# rising edge to valid DATA if WAIT# asserted	—	10	ns
t12	RD# falling edge to valid Data if WAIT# is NOT asserted	—	20	ns
t13	RD# cycle time	4.5	—	Ts (Note 1)
t14	RD# pulse active time	3	—	Ts
t15	RD# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

Note
Big Endian Mode (CNF5=1) is not supported for Direct 80 Type 2 interfaces.

7.4.3 Direct/Indirect 68

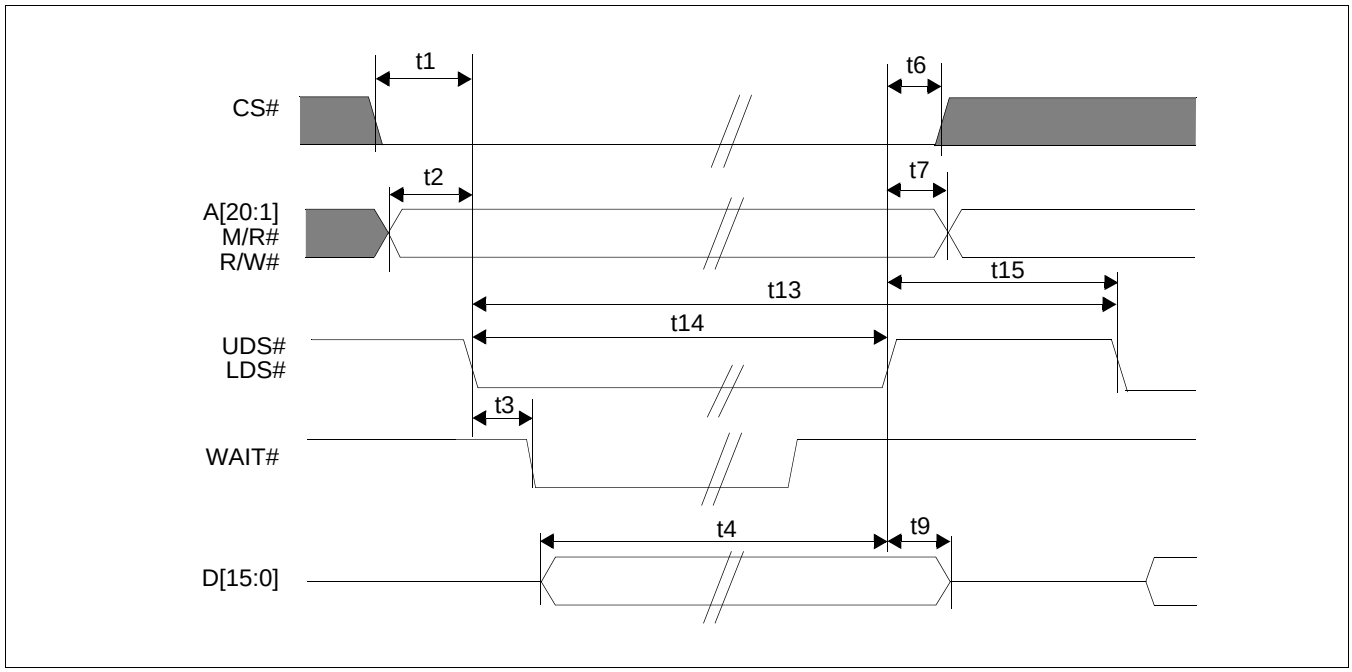

Figure 7-11: Direct/Indirect 68 Host Interface Write Timing

Table 7-12: Direct/Indirect 68 Host Interface Write Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to UDS#, LDS# falling edge	9	—	ns
t2	A[20:1], M/R#, R/W# setup time to UDS#, LDS# falling edge	9	—	ns
t3	UDS#, LDS# falling edge to WAIT# driven low	—	19	ns
t4	D[15:0] setup time to UDS#, LDS# rising edge	15	—	ns
t6	UDS#, LDS# rising edge to CS# hold time	4	—	ns
t7	UDS#, LDS# rising edge to A[20:1], M/R#, R/W# hold time	4	—	ns
t9	D[15:0] hold time from UDS#, LDS# rising edge	5	—	ns
t13	UDS#, LDS# cycle time	4.5	—	Ts (Note 1)
t14	UDS#, LDS# pulse active time	3	—	Ts
t15	UDS#, LDS# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

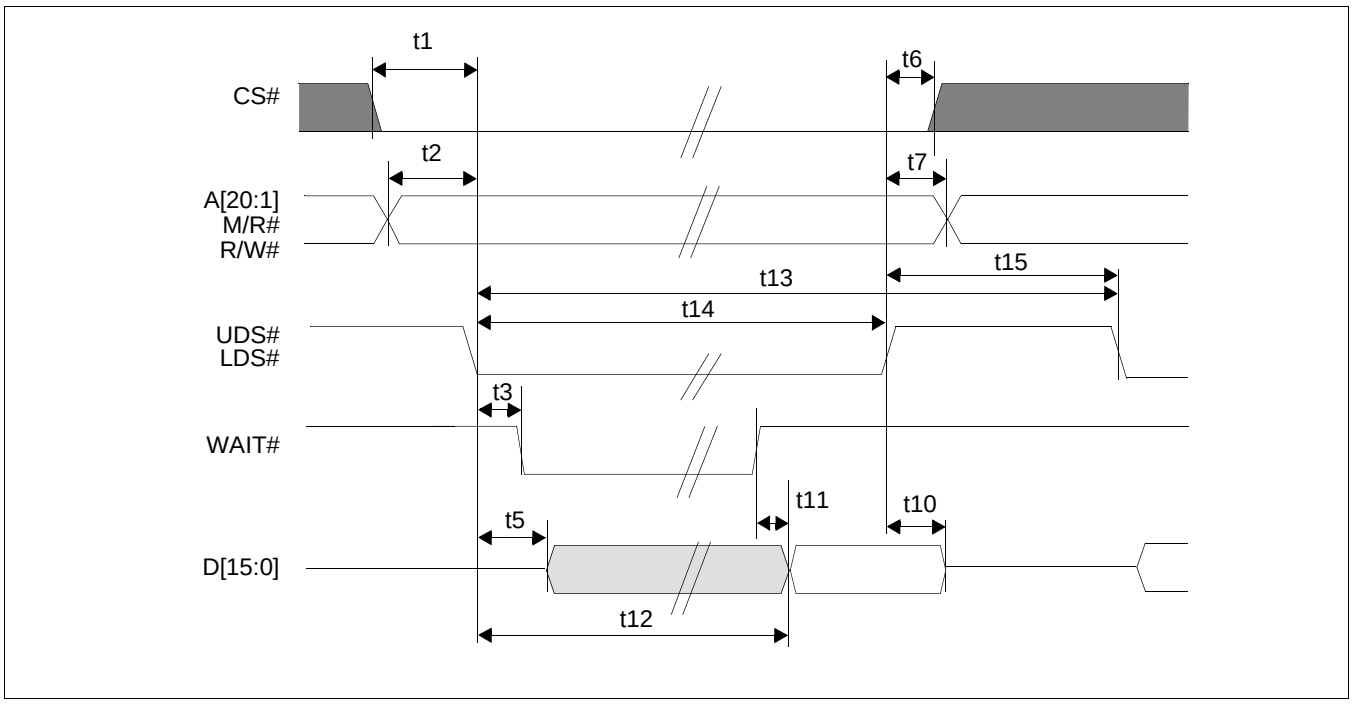

Figure 7-12: Direct/Indirect 68 Host Interface Read Timing

Table 7-13: Direct/Indirect 68 Host Interface Read Timing

Symbol	Parameter	Min	Max	Units
t1	CS# setup time to UDS#, LDS# falling edge	9	—	ns
t2	A[20:1], M/R#, R/W setup time to UDS#, LDS# falling edge	9	—	ns
t3	UDS#, LDS# falling edge to WAIT# driven low	—	19	ns
t5	UDS#, LDS# falling edge to D[15:0] driven	4	—	ns
t6	UDS#, LDS# rising edge to CS# hold time	4	—	ns
t7	UDS#, LDS# rising edge to A[20:1], M/R#, R/W hold time	4	—	ns
t10	D[15:0] hold time from UDS#, LDS# rising edge	1	10	ns
t11	WAIT# rising edge to valid DATA if WAIT# asserted	—	10	ns
t12	UDS#, LDS# falling edge to valid Data if WAIT# is NOT asserted	—	20	ns
t13	UDS#, LDS# cycle time	4.5	—	Ts (Note 1)
t14	UDS#, LDS# pulse active time	3	—	Ts
t15	UDS#, LDS# pulse inactive time	1.5	—	Ts

1. Ts = System clock period

7.4.4 Serial Host

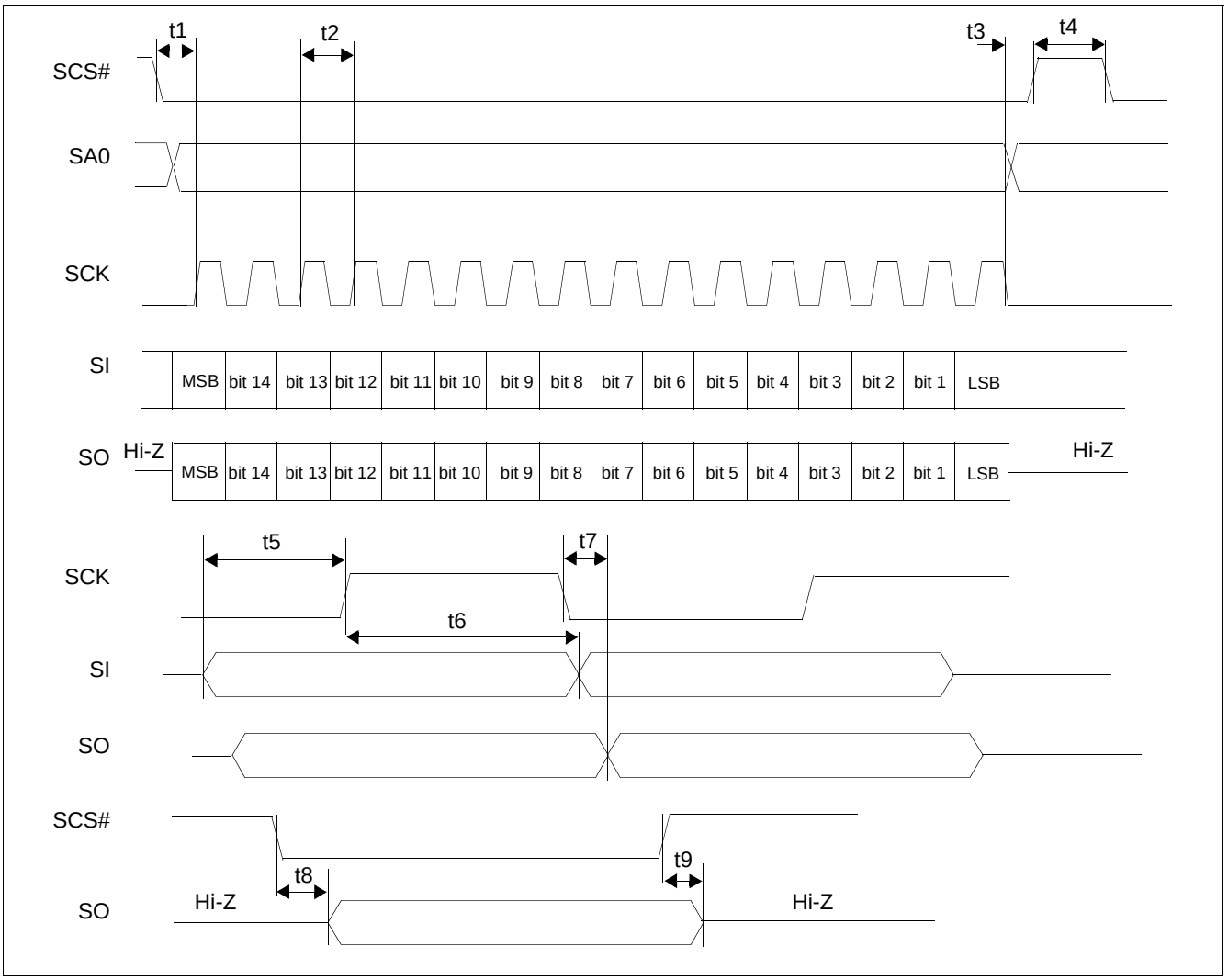

Figure 7-13: Serial Host Interface Timing for Data Valid on Falling Edge of SCK

Table 7-14: Serial Host Interface Timing for Data Valid on Falling Edge of SCK

Symbol	Parameter	Min	Max	Units
t1	SCS# low, SA0 active to rising edge of SCK	2	—	ns
t2	SCK period	63	—	ns
t3	Falling edge of SCK to SCS# high	5	—	ns
t4	SCS# high pulse width	1	—	SCK
t5	SI data setup time to rising edge of SCK	5	—	ns
t6	SI data hold time from rising edge of SCK	5	—	ns
t7	SO data valid from falling edge of SCK	—	14	ns
t8	Falling edge of SCS# to SO active	—	13	ns
t9	Rising edge of SCS# to SO Hi-Z	—	11	ns

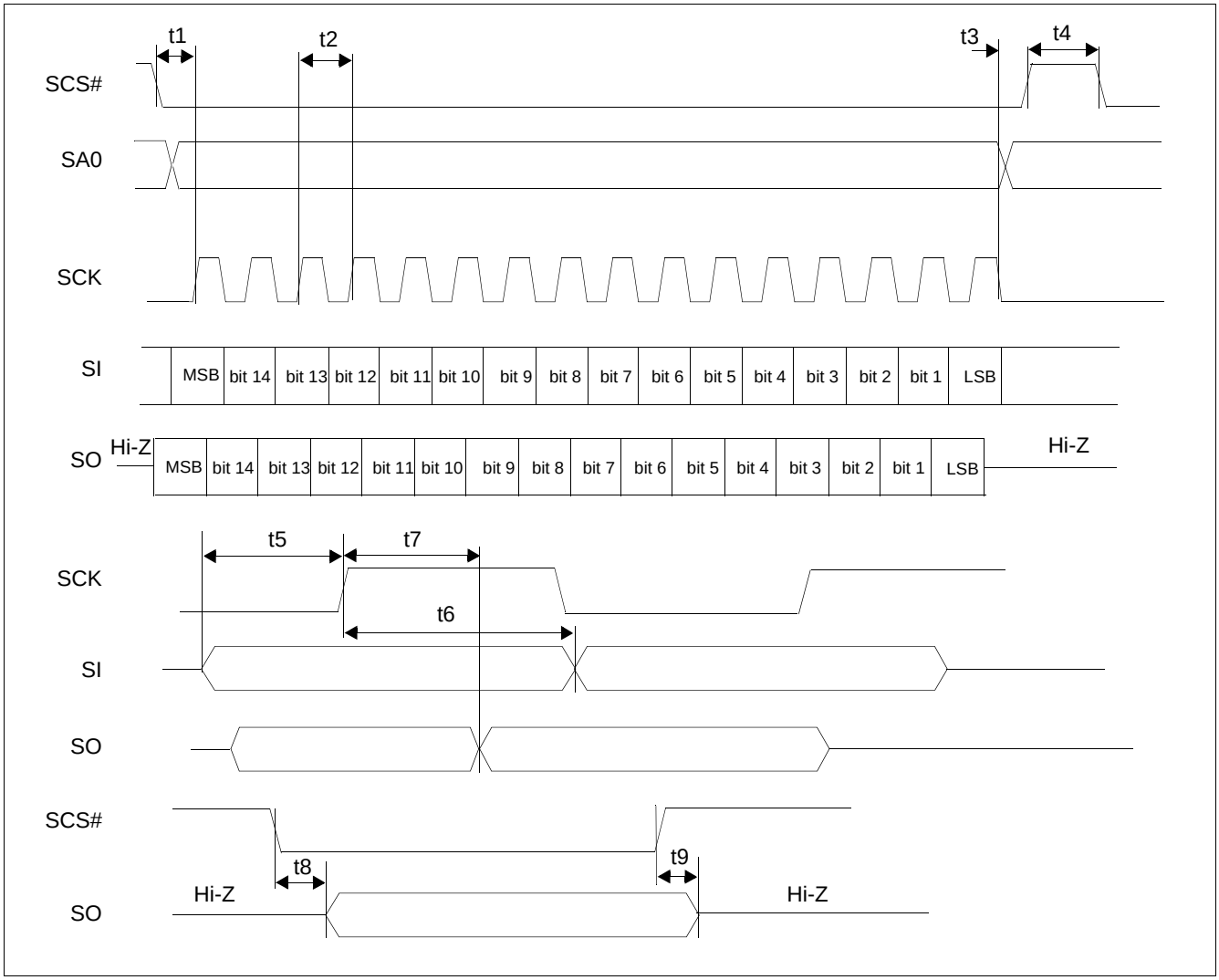

Figure 7-14: Serial Host Interface Timing for Data Valid on Rising Edge of SCK

Table 7-15: Serial Host Interface Timing for Data Valid on Rising Edge of SCK

Symbol	Parameter	Min	Max	Units
t1	SCS# low, SA0 active to rising edge of SCK	2	—	ns
t2	SCK period	63	—	ns
t3	Falling edge of SCK to SCS# high	5	—	ns
t4	SCS# high pulse width	1	—	SCK
t5	SI data setup time to rising edge of SCK	5	—	ns
t6	SI data hold time from rising edge of SCK	5	—	ns
t7	SO data valid from rising edge of SCK	—	14	ns
t8	Falling edge of SCS# to SO active	—	13	ns
t9	Rising edge of SCS# to SO Hi-Z	—	11	ns

7.4.5 Serial Host Interface Burst Mode

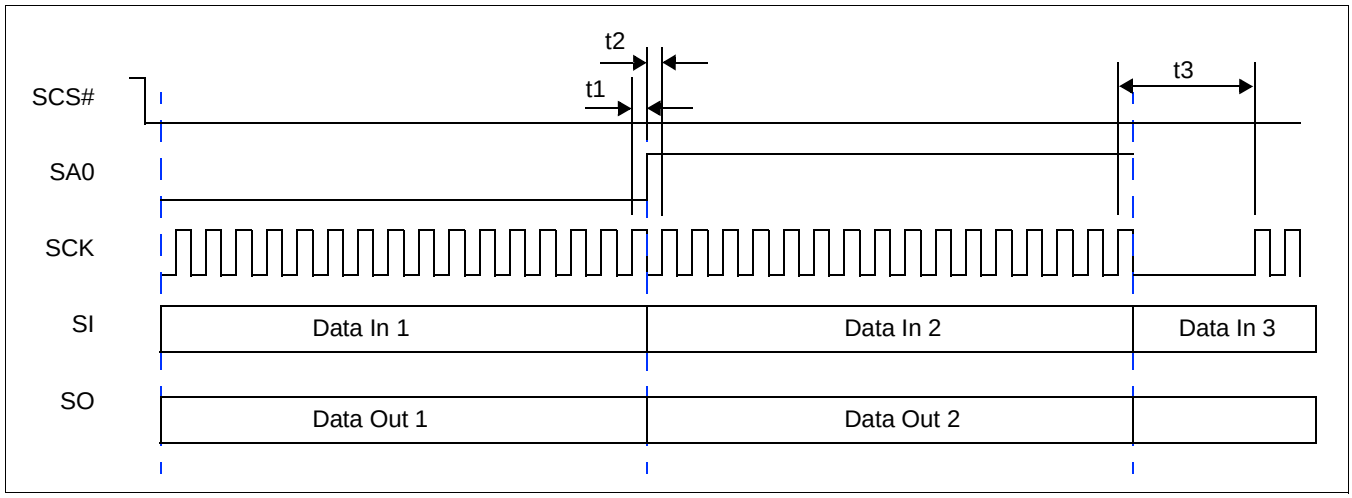

Figure 7-15: Serial Host Interface Burst Mode Timing

Table 7-16: Serial Host Interface Burst Mode Timing

Symbol	Parameter	Min	Max	Units
t1	SA0 hold after the rising edge of SCK	3	SCK-t2	ns
t2	SA0 setup to the rising edge of SCK	1	—	ns
t3	Time between the rising edge of SCK of the last transfer and the rising edge of the next transfer	5	—	ns

7.5 Power Sequencing

Setting REG[0470h] bit 0 = 1b places the S1D13L04 into power save mode. Internally the only clock on is Host Bus interface. All other clocks are off.

7.6 Panel Interface Timing

7.6.1 Generic TFT Panel Timing

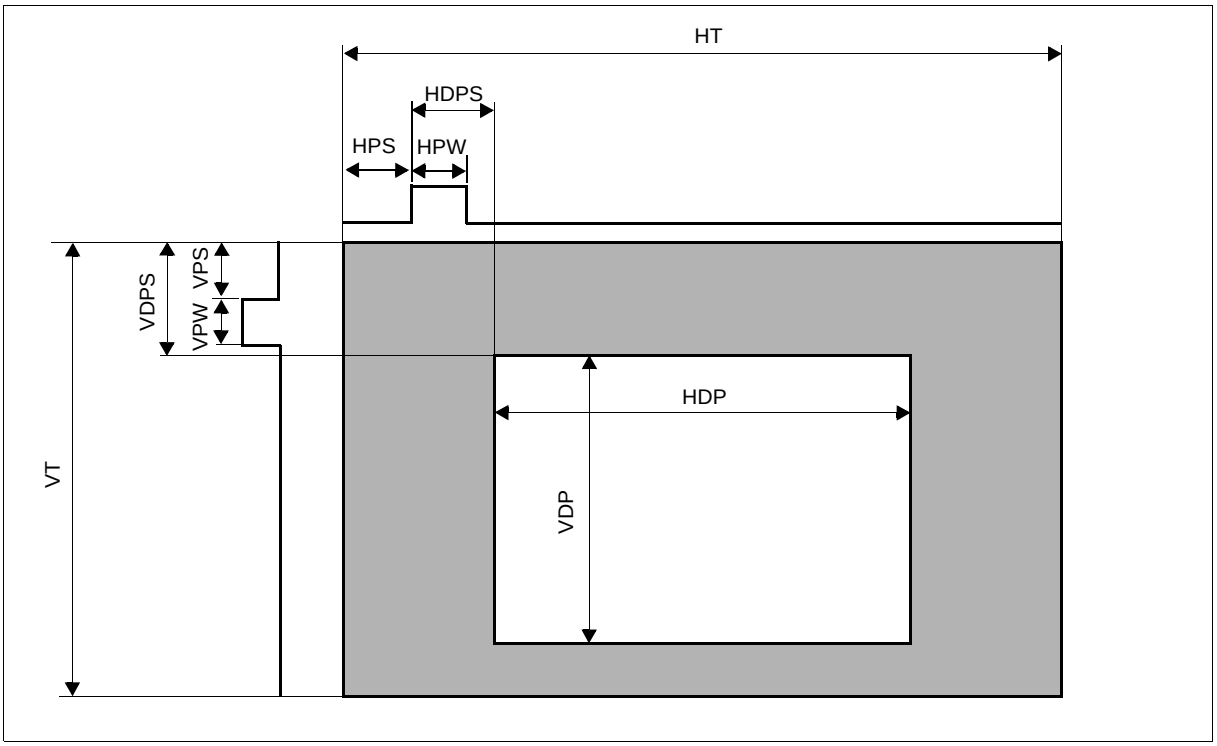

Figure 7-16: Generic TFT Panel Timing

Table 7-17: Generic TFT Panel Timing

Symbol	Description	Derived From	Units
HT	Horizontal Total (FPLINE period)	REG[0802h] bits 11-0 + 1	Ts
HDP	Horizontal Display Period	(REG[0804h] bits 10-0 + 1) x 2	
HDPS	Horizontal Display Period Start Position	REG[0806h] bits 11-0 +1	
HPW	Horizontal Pulse (FPLINE) Width	REG[0808h] bits 8-0 + 1	
HPS	Horizontal Pulse (FPLINE) Start Position	REG[080Ah] bits 11-0	
VT	Vertical Total (FPFRAME period)	REG[080Ch] bits 11-0 + 1	Lines
VDP	Vertical Display Period	REG[080Eh] bits 11-0 + 1	
VDPS	Vertical Display Period Start Position	REG[0810h] bits 11-0	
VPW	Vertical Pulse (FPFRAME) Width	REG[0812h] bits 4-0 + 1	
VPS	Vertical Pulse (FPFRAME) Start Position	REG[0814h] bits 11-0	

1. The following formulas must be valid for all panel timings:
   HDPS + HDP < HT
   VDPS + VDP < VT

Generic RGB Type Interface Panel Horizontal Timing

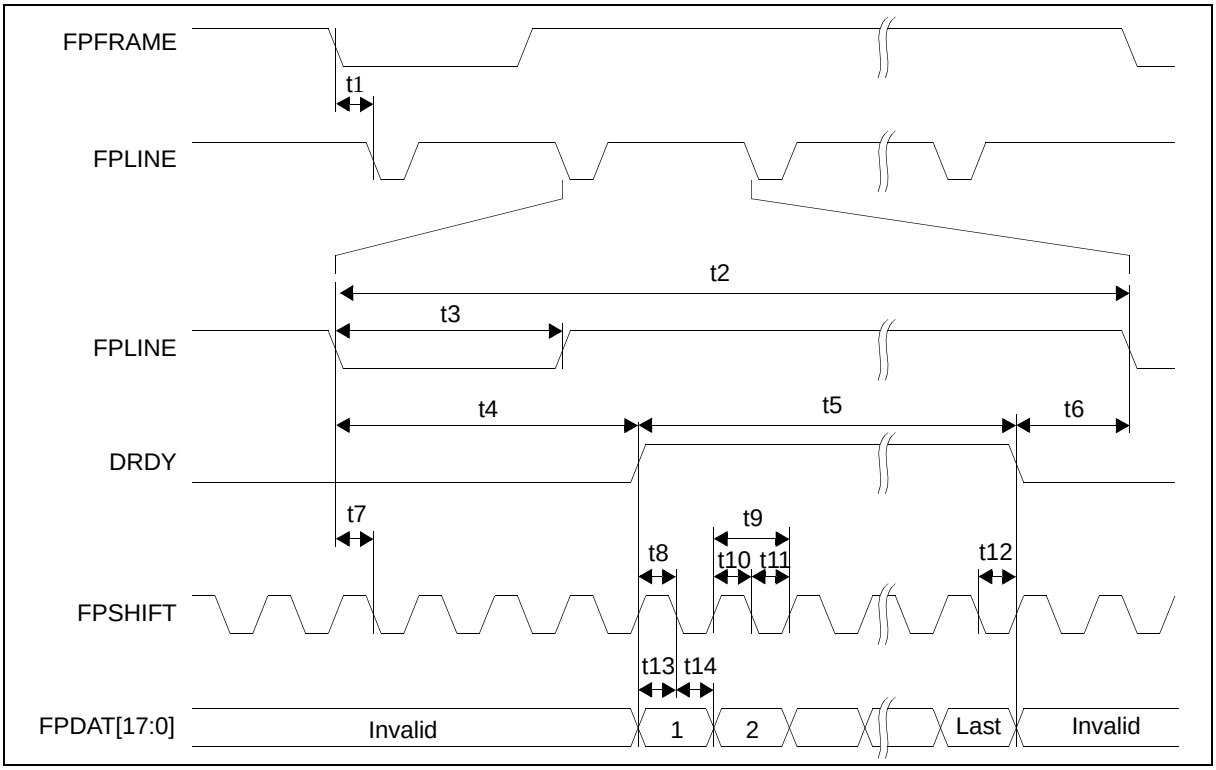

Figure 7-17: Generic RGB Type Interface Panel Horizontal Timing

Table 7-18: Generic RGB Type Interface Panel Horizontal Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	FPFRAME falling edge to FPLINE falling edge	æ	HPS	æ	Ts (Note 1)
t2	Horizontal total period	æ	HT	æ	Ts
t3	FPLINE pulse width	æ	HPW	æ	Ts
t4	FPLINE falling edge to DRDY active	æ	HDPS	æ	Ts
t5	Horizontal display period	æ	HDP	æ	Ts
t6	DRDY falling edge to FPLINE falling edge	æ	Note 2	æ	Ts
t7	FPLINE setup time to FPSHIFT falling edge	0.5Ts - 1	0.5Ts	—	ns
t8	DRDY setup to FPSHIFT falling edge	0.5Ts	—	—	ns
t9	FPSHIFT period	—	1Ts	—	ns
t10	FPSHIFT pulse width high	—	0.5Ts	—	ns
t11	FPSHIFT pulse width low	—	0.5Ts	—	ns
t12	DRDY hold from FPSHIFT falling edge	0.5Ts - 3	0.5Ts	—	ns
t13	Data setup to FPSHIFT falling edge	0.5Ts - 1	0.5Ts	—	ns
t14	Data hold from FPSHIFT falling edge	0.5Ts - 3	0.5Ts	—	ns

1. Ts = pixel clock period
2. t6typ = t2 - t4 - t5

3. The Generic TFT timings are based on the following:
   FPSHIFT Pulse Polarity is 1b (REG[0800h] bit 7 = 1b) so all panel interface signals change at the rising edge of FPSHIFT.
   FPLINE Pulse Polarity bit is active low (REG[0808h] bit 15 = 0b).
   FPFRAME Pulse Polarity bit is active low (REG[0812h] bit 15 = 0b).

Generic RGB Type Interface Panel Vertical Timing

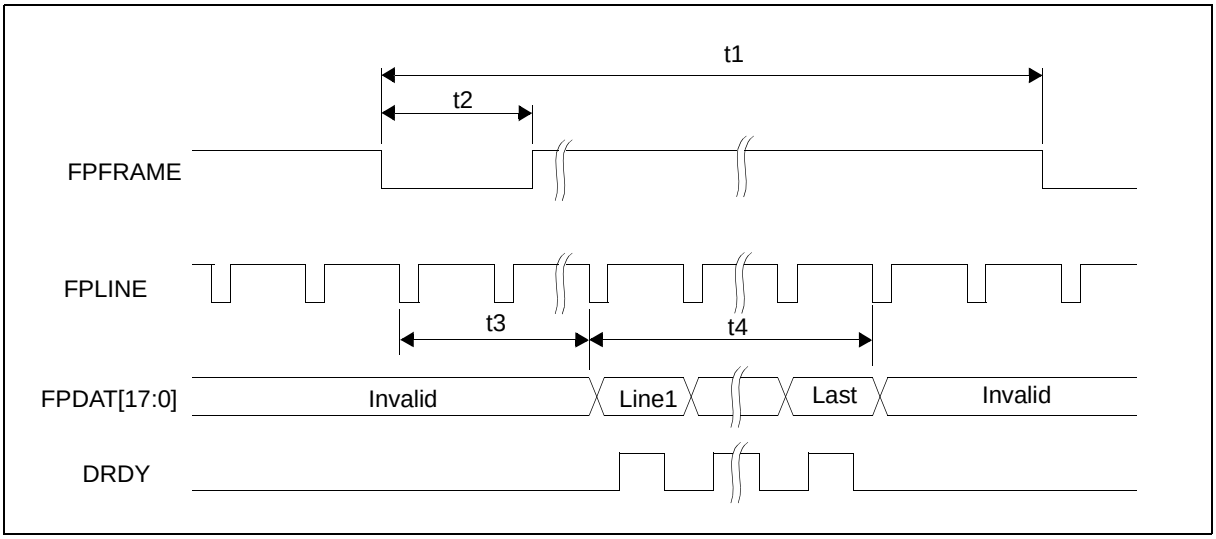

Figure 7-18: Generic RGB Type Interface Panel Vertical timing

Table 7-19: Generic RGB Type Interface Panel Vertical Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Vertical total period	æ	VT	æ	Lines
t2	FPFRAME pulse width	æ	VPW	æ	Lines
t3	Vertical display start position (Note 1)	æ	Note 2	æ	Lines
t4	Vertical display period	æ	VDP	æ	Lines

1. t3 is measured from the first FPLINE pulse at the start of the frame to the last FPLINE pulse before FPDAT is valid.
2. t3typ = VDPS - VPS

7.6.2 ND-TFD 8-Bit Serial Interface Timing

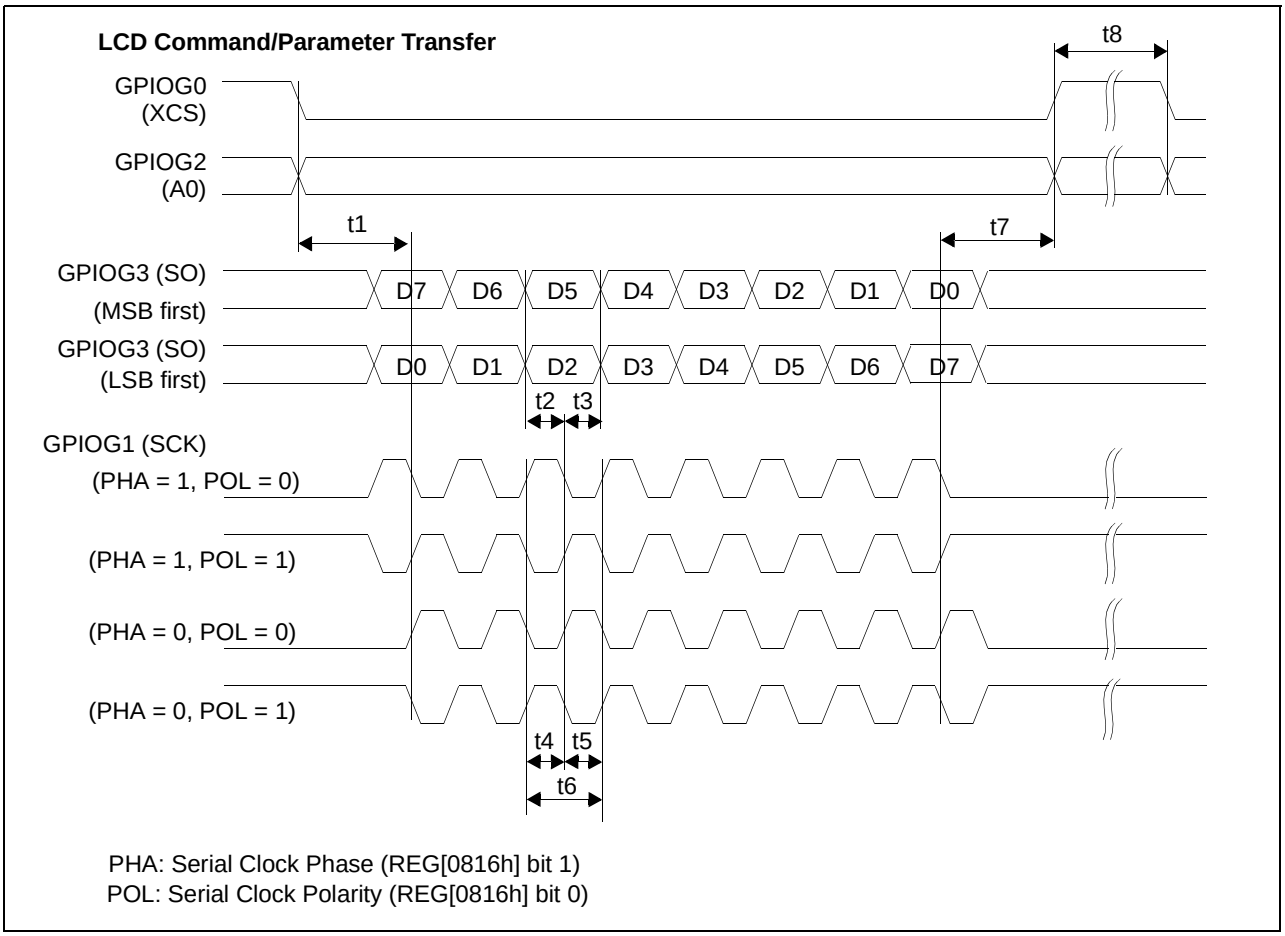

Figure 7-19: ND-TFD 8-Bit Serial Interface Timing

Table 7-20: ND-TFD 8-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	1.5Ts - 1	1.5	1.5Ts + 1	Ts (Note 1)
t2	Data setup time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t3	Data hold time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t4	Serial clock pulse width low (high)	æ	0.5	æ	Ts
t5	Serial clock pulse width high (low)	æ	0.5	æ	Ts
t6	Serial clock period	æ	1	æ	Ts
t7	Chip select hold time for command/parameter transfer	1.5Ts - 1	1.5	1.5Ts + 1	Ts
t8	Chip select de-assert to reassert	æ	1	æ	Ts

1. Ts = Serial clock period

7.6.3 ND-TFD 9-Bit Serial Interface Timing

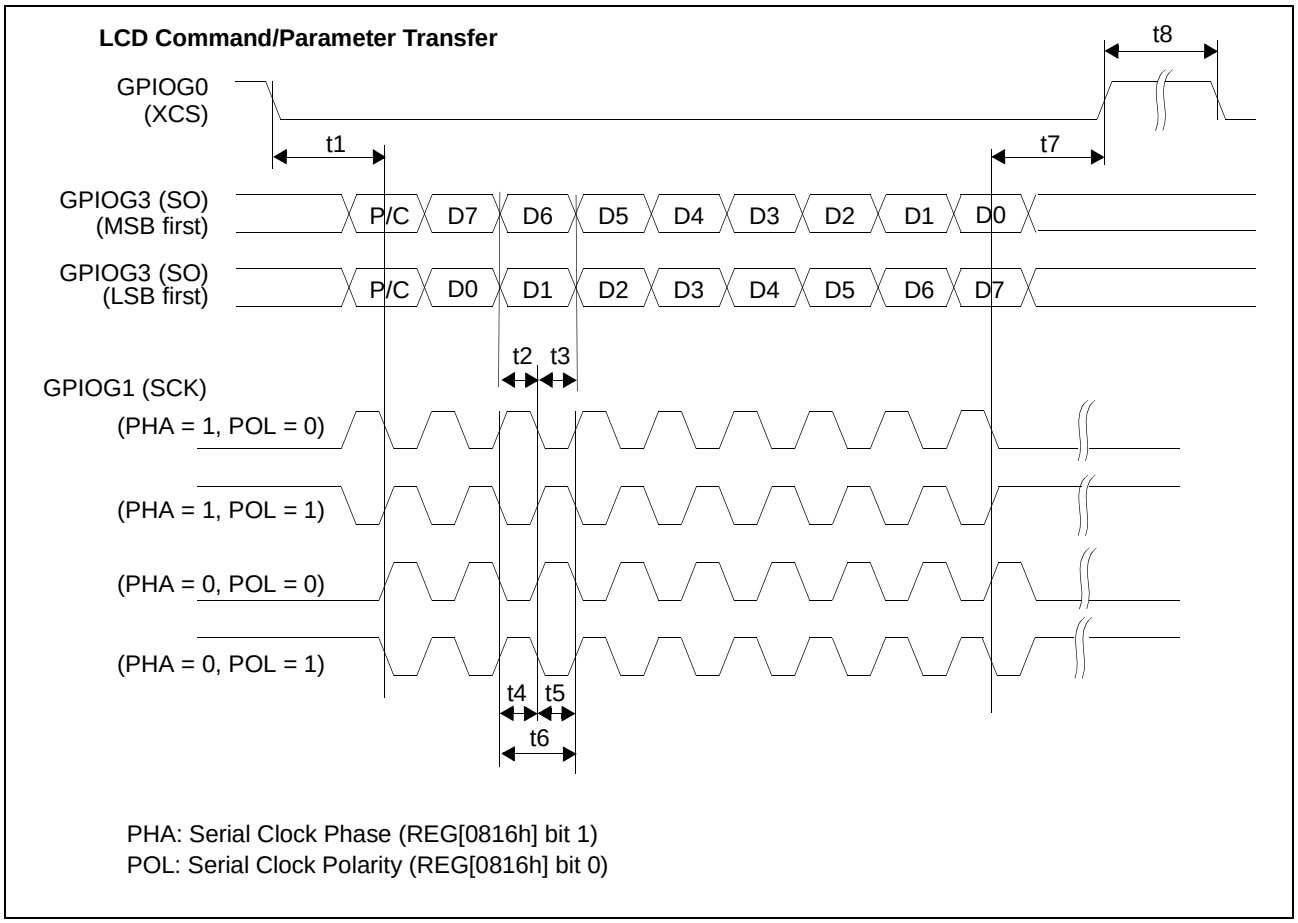

Figure 7-20: ND-TFD 9-Bit Serial Interface Timing

Table 7-21: ND-TFD 9-Bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	1.5Ts - 1	1.5	1.5Ts + 1	Ts (Note 1)
t2	Data setup time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t3	Data hold time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t4	Serial clock pulse width low (high)	æ	0.5	æ	Ts
t5	Serial clock pulse width high (low)	æ	0.5	æ	Ts
t6	Serial clock period	æ	1	æ	Ts
t7	Chip select hold time for command/parameter transfer	1.5Ts - 1	1.5	1.5Ts + 1	Ts
t8	Chip select de-assert to reassert	æ	1	æ	Ts

1. Ts = Serial clock period

7.6.4 a-Si TFT Serial Interface Timing

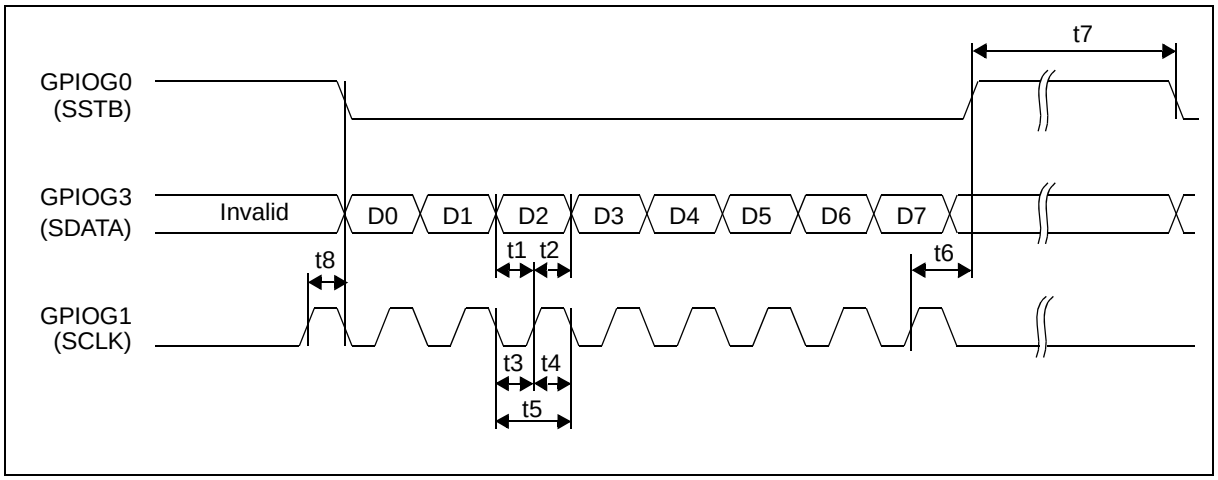

Figure 7-21: a-Si TFT Serial Interface Timing

Table 7-22: a-Si TFT Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Data Setup Time	0.5Ts - 1	0.5	0.5Ts + 1	Ts (Note 1)
t2	Data Hold Time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t3	Serial clock plus low period	æ	0.5	æ	Ts
t4	Serial clock pulse high period	æ	0.5	æ	Ts
t5	Serial clock period	æ	1	æ	Ts
t6	Chip select hold time	1.5Ts - 1	1.5	1.5Ts + 1	Ts
t7	Chip select de-assert to reassert	æ	Note 2	æ	Ts
t8	SCLK rising edge to SSTB falling edge	0.5Ts - 1	æ	0.5Ts + 1	Ts

1. Ts = Serial clock period
2. This setting depends on software.

7.6.5 uWIRE Serial Interface Timing

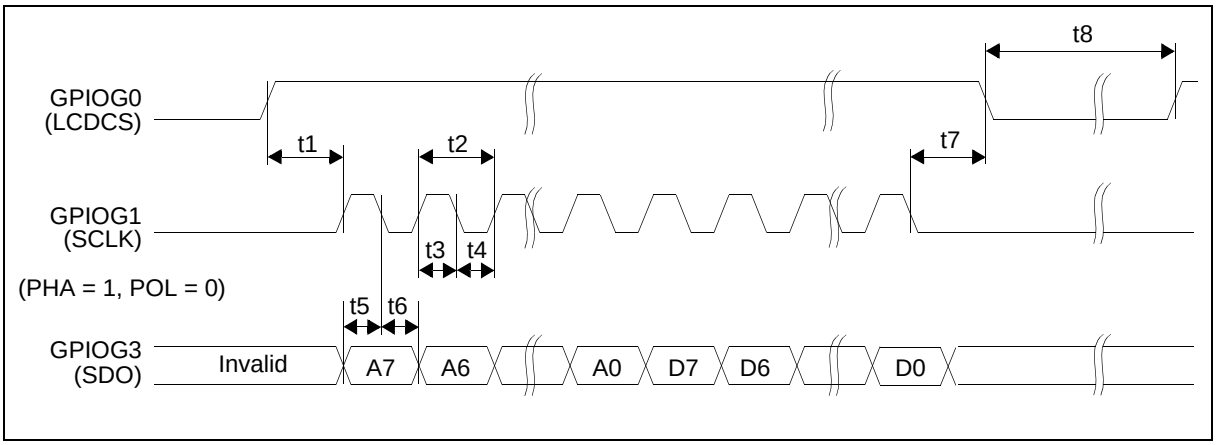

Figure 7-22: uWIRE Serial Interface Timing

Table 7-23: uWIRE Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	1.0Ts - 1	1	1.0Ts + 1	Ts (Note 1)
t2	Serial clock Period	æ	1	æ	Ts
t3	Serial clock pulse width low	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t4	Serial clock pulse width high	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t5	Data setup time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t6	Data hold time	0.5Ts - 1	0.5	0.5Ts + 1	Ts
t7	Chip select hold time	1.5Ts - 1	1.5	1.5Ts + 1	Ts
t8	Chip select de-assert to reassert	æ	Note 2	æ	Ts

1. Ts = Serial clock period
2. This setting depends on software

7.6.6 24-bit Serial Interface Timing

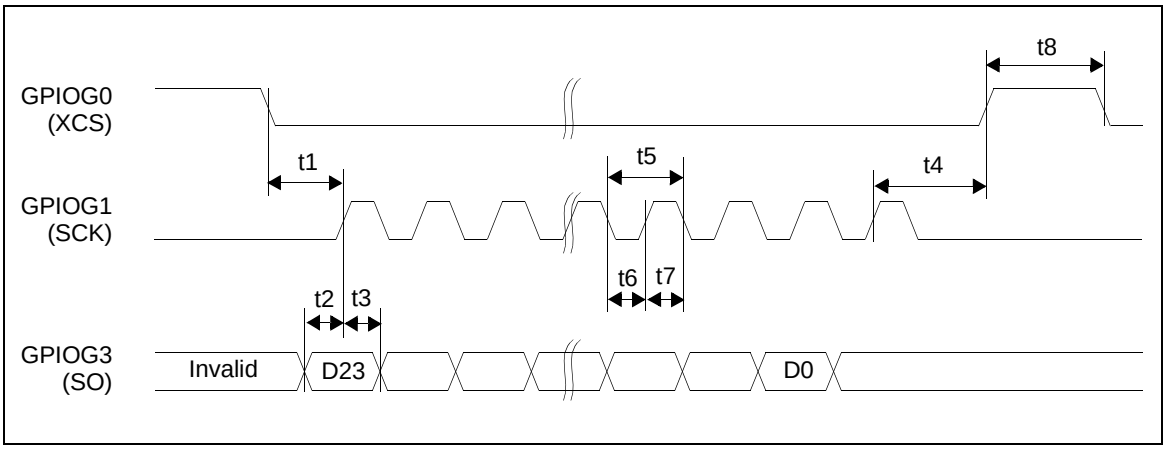

Figure 7-23: 24-bit Serial Interface Timing

Table 7-24: 24-bit Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	Chip select setup time	1.5Ts - 1	—	1.5Ts + 1	ns (Note 1)
t2	Data setup time	0.5Ts - 1	—	0.5Ts + 1	ns
t3	Data hold time	0.5Ts - 1	—	0.5Ts + 1	ns
t4	Chip select hold time	1.5Ts - 1	—	1.5Ts + 1	ns
t5	Serial clock period	—	1	—	ns
t6	Serial clock pulse low	—	0.5	—	ns
t7	Serial clock pulse high	—	0.5	—	ns
t8	Chip select de-assert to re-assert	—	Note 2	—	ns

1. Ts = Serial clock period
2. This setting depends on software.

7.7 SDRAM Interface Timing

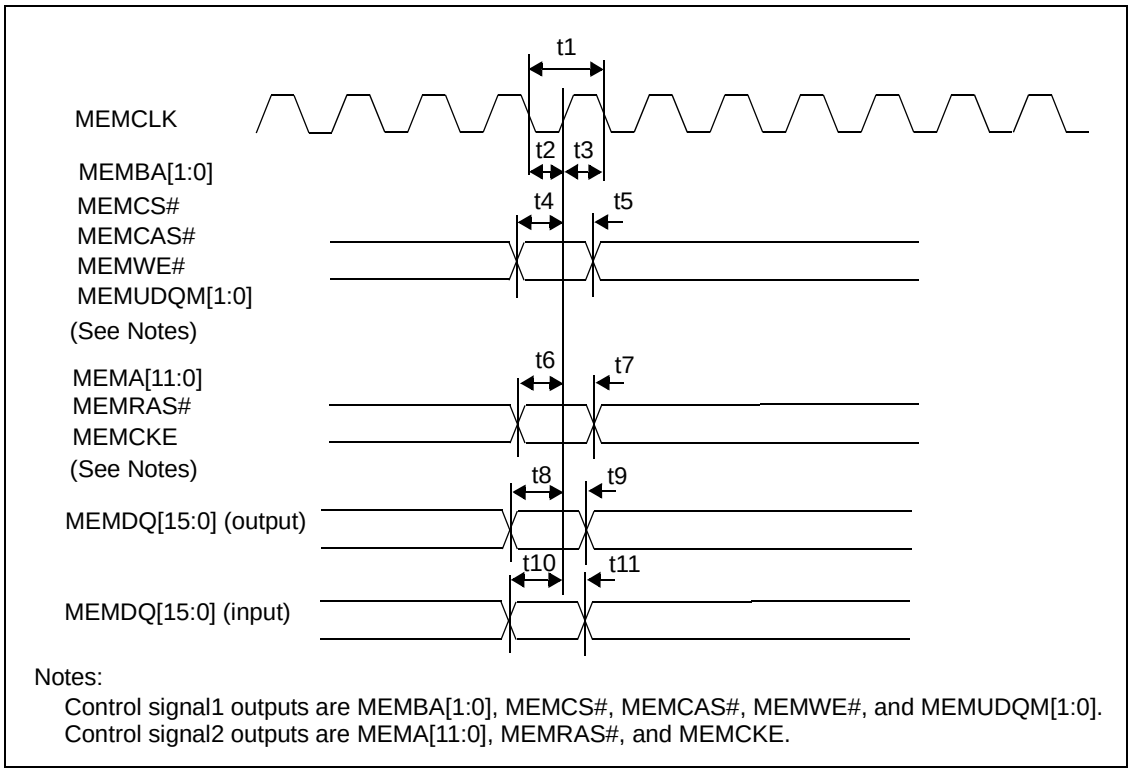

Figure 7-24: SDRAM Setup/Hold to MEMCLK Timing

Table 7-25: SDRAM Setup/Hold to MEMCLK Timing

Symbol	Parameter	Min	Max	Units
t1	MEMCLK cycle time	8	—	ns
t2	MEMCLK low pulse width	3	—	ns
t3	MEMCLK high pulse width	3	—	ns
t4	Control signal1 outputs setup time to MEMCLK (see Note)	0.5Tc-1ns	—	Tc
t5	Control signal1 outputs hold time to MEMCLK (see Note)	0.5	—	Tc
t6	Control signal2 outputs setup time to MEMCLK (see Note)	0.5Tc-2ns	—	Tc
t7	Control signal2 outputs hold time to MEMCLK (see Note)	0.5	—	Tc
t8	MEMDQ[15:0] output setup time to MEMCLK	0.5Tc-2ns	—	Tc
t9	MEMDQ[15:0] output hold time to MEMCLK	0.5Tc-2ns	—	Tc
t10	MEMDQ[15:0] input setup time to MEMCLK (See Note)	3.6	—	ns
t11	MEMDQ[15:0] input hold time to MEMCLK	0	—	ns

1. Tc is a unit of MEMCLK cycle.
2. The MEMDQ[15:0] setup time (t10) is the value specified by REG[1C00h] = 11h.

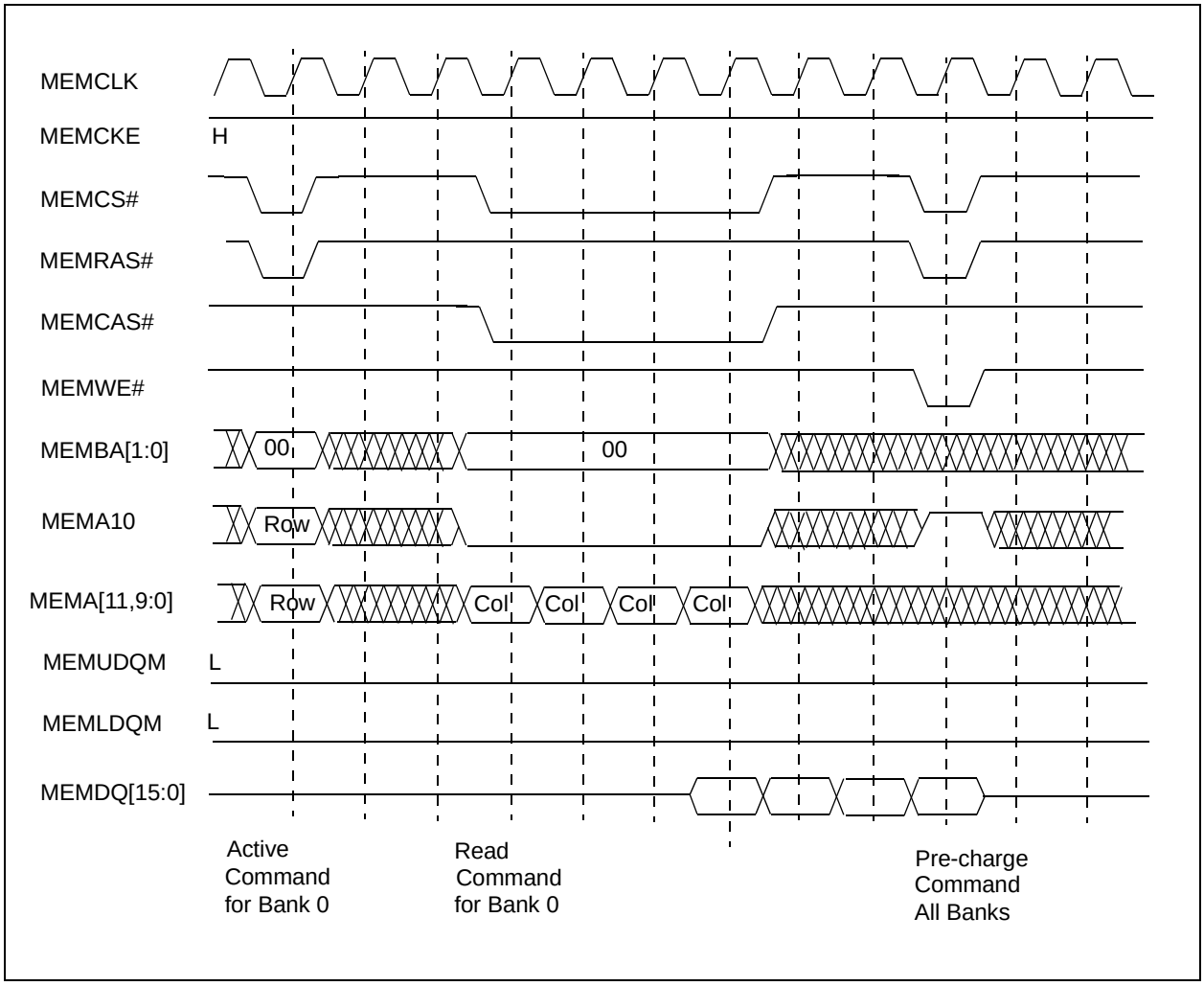

Figure 7-25: SDRAM Read Timing (Ex. Read Length = 4, CAS Latency = 3)

Note

Burst length is automatically set (undefined length).

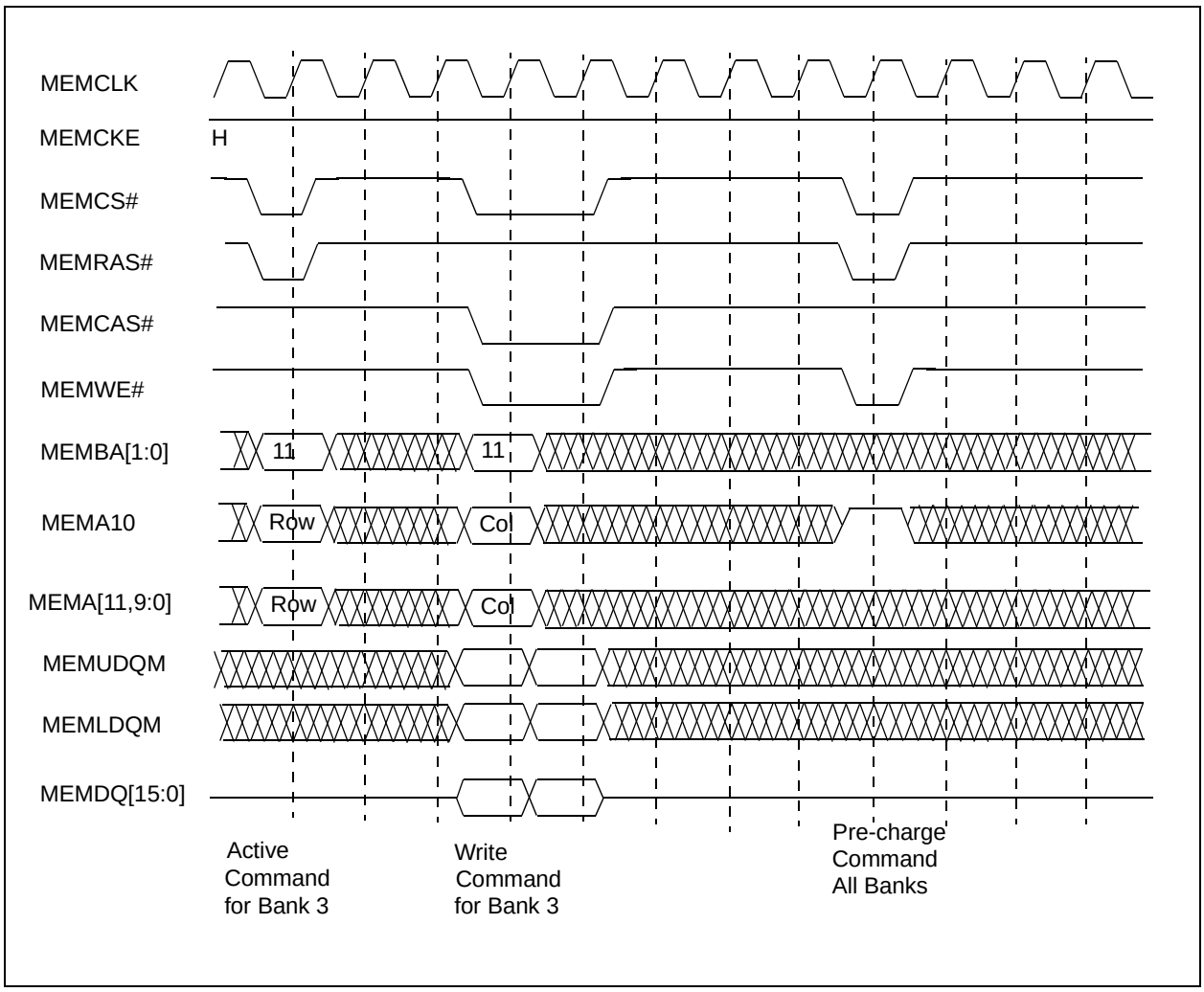

Figure 7-26: SDRAM Write Timing (Ex. Write Length = 2)

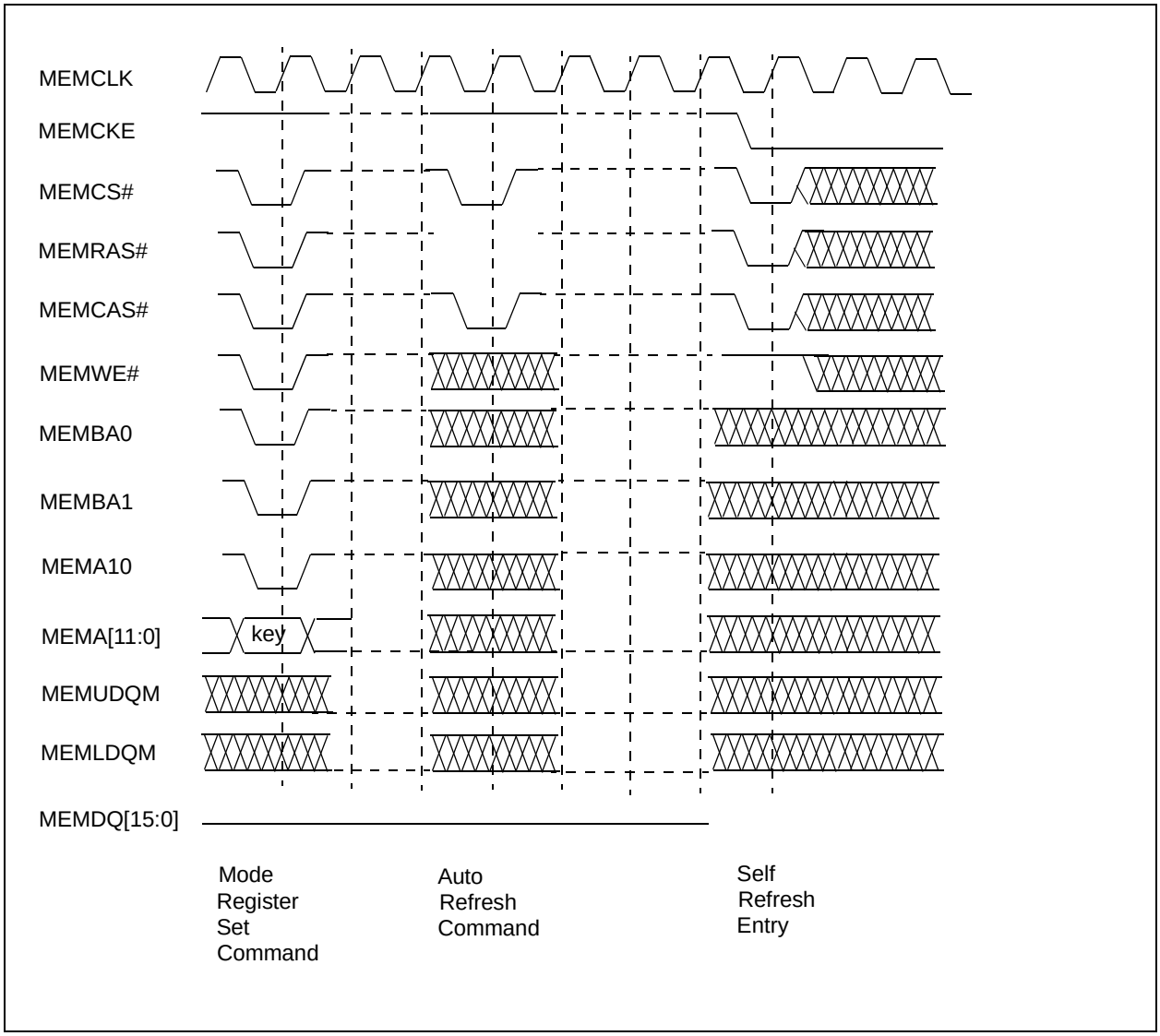

Figure 7-27: Mode Register Set / Auto Refresh / Auto Pre-charge Timing

Chapter 8 Memory Map

The S1D13L04 includes an SDRAM interface which supports either 64Mbit (8M bytes), or 128Mbit (16M bytes) of external SDRAM or external mobile SDRAM.

This memory must be accessed differently depending on the addressing method used.

Note
The S1D13L04 host interface includes a memory buffer which accelerates memory accesses by "reading ahead". For further details on this Read Ahead feature, see Section 16.4, "Read Ahead Feature" on page 190.

8.1 Accessing Memory using Direct Addressing

When direct addressing is selected (see Section 5.3, "Summary of Configuration Options" on page 29), the first Megabyte of external SDRAM can be addressed linearly. The remaining memory (up to 15M bytes) must be accessed using four 256K byte pages which are re-directed into the SDRAM address space (see Figure 8-1: "Memory Access Example using Direct Addressing (16M Byte Example)" on page 67.

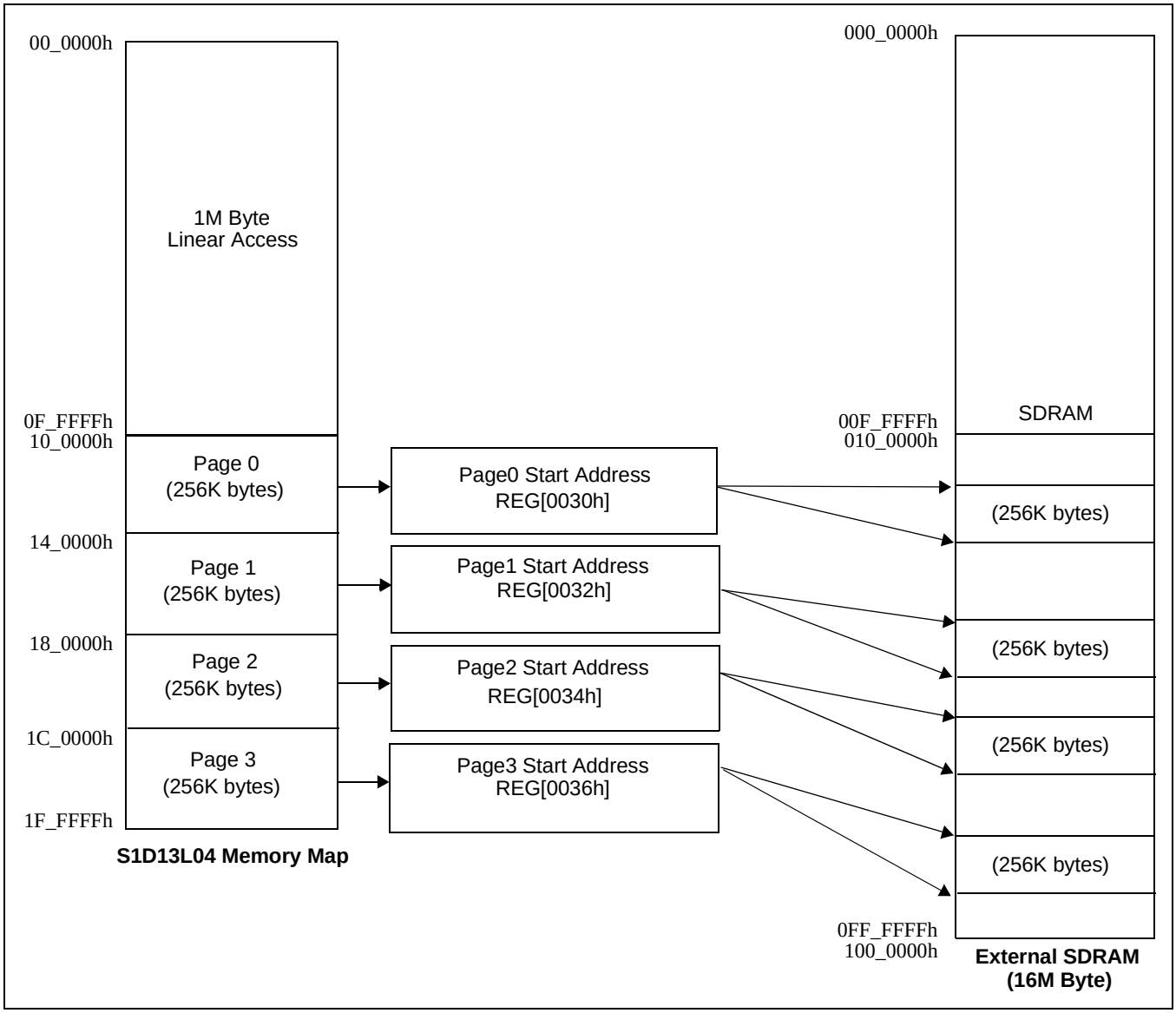

Figure 8-1: Memory Access Example using Direct Addressing (16M Byte Example)

8.2 Accessing Memory using Indirect Addressing

When indirect addressing is selected (see Section 5.3, “Summary of Configuration Options” on page 29), the SDRAM memory is addressed according to the address set in REG[0012h] ~ REG[0014h]. The address size allows access to the full range of possible SDRAM memory sizes. Once the address is set, the memory can be read/written through the Indirect Interface Memory Access Data Port, REG[0018h]. When a memory access completes, the address is incremented automatically.

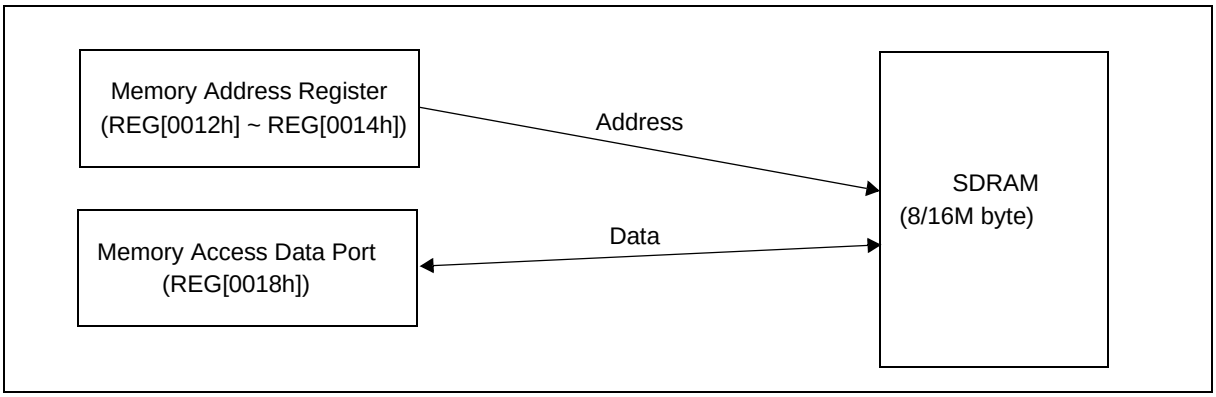

Figure 8-2: External Memory (Indirect Access)

8.3 IO Map

To access the functional registers for each IO device, refer to Table 10-2:, “S1D13L04 Register Mapping,” on page 71.

Chapter 9 Clocks

9.1 Clock Overview

The following diagram provides a logical representation of the S1D13L04 internal clocks.

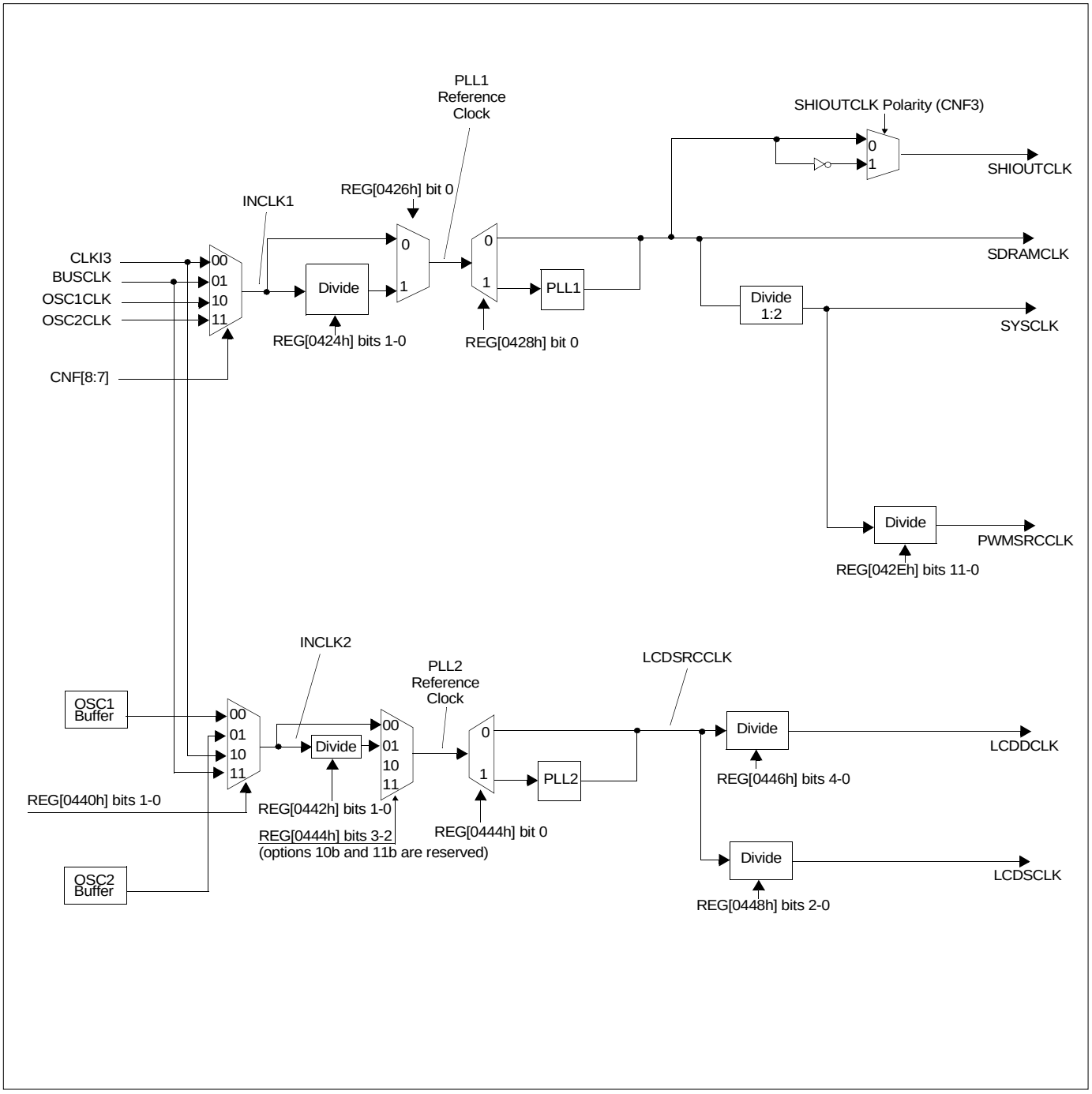

Figure 9-1: Clock Diagram

9.2 PLL Programming Examples

Before changing the frequency of either PLL1 or PLL2, the PLL must be disabled using the PLL1 Enable bit (REG[0410h] bit 0) or PLL2 Enable bit (REG[0418h], as appropriate. Note that when the PLL is enabled after the changes, it is unstable for a maximum of 200µs.

Example 1: Set PLL2 for a fPLLOUT = 20MHz using fPLLREFCLK = 5MHz.

1. Find the value of NN.
   NN = fPLL2OUT ÷ fPLL2REFCLK
   NN = 20MHz ÷ 5MHz
   NN = 4
   Set the PLL2 N Multiplier bits 3-0 = 0011b (see REG[0414h] bits 3-0).

2. Find the VCO frequency.
   fVCO = fPLL2OUT x VV
   fVCO = 20 x 2
   fVCO = 40 MHz
   In this case, the default VV of 2 does not meet the following condition:
   100MHz <= fVCO <= 400MHz

   A VV of 8 does meet the condition (20MHz x 8 = 160MHz).
   Therefore, set the V Divider bits 1-0 to 11b (see REG[0414h] bits 5-4).

3. Set the PLL2 VC bits 3-0 for fVCO = 160MHz (REG[0414h] bits 11-8 = 0010b).

4. Set the Low Pass Filter resistance for a fPLL2REFCLK of 5MHz.
   Set the PLL2 RS bits 3-0 to 1010b (see REG[0414h] bits 15-12).

Chapter 10 Registers

This section discusses how and where to access the S1D13L04 registers. It also provides detailed information about the layout and usage of each register.

Note
If a Big Endian Host interface is selected, the registers must be accessed using the procedure shown in Section 16.6, “Register Accesses for Big Endian Host Interfaces” on page 198.

10.1 Register Mapping

The S1D13L04 registers are memory-mapped. When the system decodes the input pins as CS# = 0 and M/R# = 0, the registers may be accessed.

Table 10-1: S1D13L04 Memory/Register Selection

M/R#	Address	Size	Function
1	000000h to 1FFFFFh	2M bytes	SDRAM memory Space
0	000000h to 1FFFFFh	2M bytes	All registers spaces

Note
When Power Save Mode is enabled, synchronous registers and SDRAM memory must not be accessed.

The register space is decoded by AB[20:0] and is mapped as follows.

Table 10-2: S1D13L04 Register Mapping

Address	Type	Function
0000h to 0004h	Asynchronous	Host Interface Registers
0006h to 0044h	Synchronous	
0400h to 0472h	Asynchronous	System Control Registers
0800h to 081Ch	Synchronous	LCD Panel Configuration Registers
0830h to 0870h	Synchronous	LCD Display Mode Registers
0C00h to 0C2Ah	Asynchronous	GPIO Registers
1C00h to 1C14h	Synchronous	Memory Controller Registers
3400h to 3412h	Synchronous	PWM Registers

10.2 Register Set

The S1D13L04 registers are listed in the following table

Table 10-3: S1D13L04 Register Set

Table 10-3: S1D13L04 Register Set (Continued)

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10.3 Register Restrictions

All reserved bits must be set to 0b unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. All register accesses must be 16-bit accesses.

10.4 Register Descriptions

10.4.1 Host Interface Registers

REG[0000h] through REG[0002h] are Reserved

REG[0004h] Embedded Memory Size Register
Default = 0000h — Read Only

Embedded Memory Size bits 15-8							
15	14	13	12	11	10	9	8
Embedded Memory Size bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Embedded Memory Size bits [15:0]
These bits indicate the size of the embedded memory. Since the S1D13L04 has no embedded memory, these bits return 0000h.

REG[0006h] through REG[0010h] are Reserved

These registers are Reserved and should not be written.

REG[0012h] Indirect Interface Memory Address Register 0
Default = 0000h — Read/Write

Indirect Interface Memory Address bits 15-8							
15	14	13	12	11	10	9	8
Indirect Interface Memory Address bits 7-1							Indirect Interface Memory Access Read/Write Select
7	6	5	4	3	2	1	0

REG[0014h] Indirect Interface Memory Address Register 1
Default = 0000h — Read/Write

Reserved	Indirect Interface Memory Address bits 30-24						
15	14	13	12	11	10	9	8
Indirect Interface Memory Address bits 23-16							
7	6	5	4	3	2	1	0

REG[0012h] bit 0 Indirect Interface Memory Access Read/Write Select
This bit is used for Indirect Interface modes only.
This bit selects whether a memory access done through the Indirect Interface Memory Access Data Port (REG[0018h]) is a read or write access.
When this bit = 0b, a write access takes place. (default)
When this bit = 1b, a read access takes place.

REG[0014h] bit 15 Reserved
The default value for this bit is 0b.

REG[0014h] bits 14-0

REG[0012h] bits 15-1 Indirect Interface Memory Address bits [30:1]

These bits are used for Indirect Interface modes only.

These bits specify the address used for each memory access when an indirect interface is selected.

REG[0014h] bits 9-0, REG[0012h] bits 15-1
= Indirect Interface Memory Address bits 25-1

For further information on accessing memory using the indirect interface, see Section 8.2, “Accessing Memory using Indirect Addressing” on page 68.

REG[0016h] is Reserved

This register is Reserved and should not be written.

REG[0018h] Indirect Interface Memory Access Data Port Register

Default = 0000h — Read/Write

Indirect Interface Memory Access Data Port bits 15-8							
15	14	13	12	11	10	9	8
Indirect Interface Memory Access Data Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Indirect Interface Memory Access Data Port bits [15:0]

These bits are used for Indirect Interface modes only.

These bits are the memory read/write port for the Indirect Interface. For more information on using the Indirect Interface, see Section 16.3, “Indirect Interface” on page 186.

REG[001Ah] Memory Access Status Register

Default = 0000h — Read Only

Memory Busy	n/a						
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

bit 15 Memory Busy

When this bit = 0b, the memory controller is idle and the Host CPU can access memory. Data read / write is possible via the Indirect Interface Memory Access Data Port (REG[0018h]).

When this bit = 1b, the memory controller is busy and the Host CPU cannot access memory.

REG[001Ch] through REG[001Eh] are Reserved

These registers are Reserved and should not be written.

REG[0020h] Interrupt Status Register
Default = 0000h Read/Write

n/a				Reserved			
15	14	13	12	11	10	9	8
Reserved				GPIO Interrupt Flag	VSYNC Interrupt Flag	Reserved	Host Interrupt Flag
7	6	5	4	3	2	1	0

bits 11-4 Reserved
These bits must set to 00000000b.

bit 3 GPIO Interrupt Flag
This bit indicates the status of the GPIO interrupt which occurs when one of the GPIOA or GPIOB Interrupt Status bits returns a 1b (see REG[0C2Ah]).
When this bit = 0b, a GPIO interrupt has not occurred.
When this bit = 1b, a GPIO interrupt has occurred.

To clear this flag, clear the GPIO Interrupt Status bits in REG[0C2Ah].

bit 2 VSYNC Interrupt Flag
This bit indicates the status of the VSYNC interrupt which occurs when the VSYNC Interrupt Status bit returns a 1b (see REG[0818h] bit 11).
When this bit = 0b, a VSYNC interrupt has not occurred.
When this bit = 1b, a VSYNC interrupt has occurred.

To clear this flag, clear the VSYNC Interrupt Status bit in REG[0818h] bit 11.

bit 1 Reserved
The default value for this bit is 0b.

bit 0 Host Interrupt Flag
This bit indicates the status of the Host interrupt which is generated when a Host Read/Write Cycle Time-out (see REG[0026h] bits 1-0) or Host WAIT# Length Time-out (see REG[0472h] bits 2-0) occurs. For further information on the time-out functions, refer to Section 16.2, “Host Bus Time-out Function” on page 184.
When this bit = 0b, a Host interrupt has not occurred.
When this bit = 1b, a Host interrupt has occurred.

To clear this flag, clear the interrupt flags in REG[0026h] bits 1-0.

REG[0022h] is Reserved

This register is Reserved and should not be written.

REG[0024h] Host Time-out Control Register
Default = 007Fh — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
Host Time-out Enable	Host Time-out Value bits 6-0						

bit 7 Host Time-out Enable
This bit controls the bus time-out function for the host bus interface. A host bus time-out occurs when the host accesses SDRAM and the host cycle exceeds the time-out value specified by the Host Time-out Value bits, REG[0024h] bits 6-0. For further information, see Section 16.2, “Host Bus Time-out Function” on page 184.
When this bit = 0b, the time-out function is disabled.
When this bit = 1b, the time-out function is enabled.

bits 6-0 Host Time-out Value bits [6:0]
These bits specify the time-out value for the Host Time-out function, in system clocks. When these bits are set to 00h, a Host Time-out will not occur.

REG[0026h] Bus Error Interrupt Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	Reserved

7	6	5	4	3	2	1	0
n/a						Memory Read Error Interrupt Flag	Memory Write Error Interrupt Flag

bit 9 Reserved
The default value for this bit is 0b.

bit 8 Reserved
The default value for this bit is 0b.

bit 1 Memory Read Error Interrupt Flag
This bit indicates the status of the Memory Read Error interrupt which occurs when a read access does not return the value within the specified time (see REG[0024h] bits 6-0). This bit is masked by the Memory Read Error Interrupt Enable bit and is only available when REG[0028h] bit 1 = 1b.
When this bit = 0b, a Memory Read Error interrupt has not occurred.
When this bit = 1b, a Memory Read Error interrupt has occurred.

bit 0 Memory Write Error Interrupt Flag
This bit indicates the status of the Memory Write Error interrupt which occurs when a write access does not complete within the specified time (see REG[0024h] bits 6-0). This bit is masked by the Memory Write Error Interrupt Enable bit and is only available when REG[0028h] bit 0 = 1b.
When this bit = 0b, an Memory Write Error interrupt has not occurred.
When this bit = 1b, an Memory Write Error interrupt has occurred.

REG[0028h] Bus Error Interrupt Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	Reserved
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						Memory Read Error Interrupt Enable	Memory Write Error Interrupt Enable

bit 9 Reserved
The default value for this bit is 0b.

bit 8 Reserved
The default value for this bit is 0b.

bit 1 Memory Read Error Interrupt Enable
This bit controls the Memory Read Error interrupt. The status is indicated by the Memory Read Error Interrupt Flag, REG[0026h] bit 1.
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 0 Memory Write Error Interrupt Enable
This bit controls the Memory Write Error interrupt. The status is indicated by the Memory Write Error Interrupt Flag, REG[0026h] bit 0.
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

REG[002Ah] Interrupt Pin Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
INT1# Pin Interrupt Enable	Reserved	INT1# Output Control	Reserved	INT1# Pin Polarity Select	n/a		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a							

bit 15 INT1# Pin Interrupt Enable
This bit controls whether the INT1# pin sends interrupt requests to the Host. T
When this bit = 0b, the INT1# pin does not send interrupt requests to the Host (output is disabled).
When this bit = 1b, the INT1# pin sends interrupt requests to the Host (output is enabled).

bit 14 Reserved
The default value for this bit is 0b.

bit 13 INT1# Output Control
This bit controls the output of the INT1# pin. For a summary, refer to Table 10-4:, “INT1# Output Control/Pin Polarity Select Summary,” on page 80.
When this bit = 0b and the INT1# Pin Polarity Select bit is set for active low, INT1# is driven Hi-Z when inactive and LOW when active.
When this bit = 0b and the INT1# Pin Polarity Select bit is set for active high, INT1# is driven LOW when inactive and HIGH when active.
When this bit = 1b, the output is always driven HIGH or LOW depending on the INT1# polarity.

bit 12 Reserved
The default value for this bit is 0b.

bit 11 INT1# Pin Polarity Select
This bit selects the polarity of the INT1# pin. For a summary, refer to Table 10-4:, “INT1# Output Control/Pin Polarity Select Summary,” on page 80.
When this bit = 0b, the INT1# pin is active low.
When this bit = 1b, the INT1# pin is active high.

Table 10-4: INT1# Output Control/Pin Polarity Select Summary

REG[002Ah] bit11	INT1# Interrupt Status	REG[002Ah] bits 15,13	
		00b	11b
00b	Interrupt has not occurred	INT1# = HIGHZ	INT1# = Driven HIGH
	Interrupt has occurred	INT1# = Driven LOW	INT1# = Driven LOW
11b	Interrupt has not occurred	INT1# = Driven LOW	INT1# = Driven LOW
	Interrupt has occurred	INT1# = Driven HIGH	INT1# = Driven HIGH

REG[002Ch] through REG[002Eh] are Reserved

These registers are Reserved and should not be written.

REG[0030h] SDRAM Host Page 0 Start Address Register
Default = 0000h Read/Write

n/a						Reserved	
15	14	13	12	11	10	9	8
SDRAM Host Page 0 Start Address bits 23-18						n/a	
7	6	5	4	3	2	1	0

bits 9-8 Reserved
The default value for this bit is 0b.

bits 7-2 SDRAM Host Page 0 Start Address bits [23:18]

These bits specify bits 23-18 of the memory start address for Page 0, which re-directs Host CPU memory accesses to a 256K byte window in SDRAM. Page 0 is accessed by the HOST CPU through memory address 100000h - 13FFFFh. For further information on accessing the external SDRAM memory, see Section 8.1, “Accessing Memory using Direct Addressing” on page 66.

REG[0030h] bits 7-2 = SDRAM Host Page 0 Start Address bits [23:18]

REG[0032h] SDRAM Host Page 1 Start Address Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	
SDRAM Host Page 1 Start Address bits 23-18						n/a	
7	6	5	4	3	2	1	0

bits 7-2 SDRAM Host Page 1 Start Address bits [23:18]

These bits specify bits 23-18 of the memory start address for Page 1, which re-directs Host CPU memory accesses to a 256K byte window in SDRAM. Page 1 is accessed by the HOST CPU through memory address 140000h - 17FFFFh. For further information on accessing the external SDRAM memory, see Section 8.1, “Accessing Memory using Direct Addressing” on page 66.

REG[0032h] bits 7-2 = Host SDRAM Page 1 Start Address bits [23:18]

REG[0034h] SDRAM Host Page 2 Start Address Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	
SDRAM Host Page 2 Start Address bits 23-18						n/a	
7	6	5	4	3	2	1	0

bits 7-2 SDRAM Host Page 2 Start Address bits [23:18]

These bits specify bits 23-18 of the memory start address for Page 2, which re-directs Host CPU memory accesses to a 256K byte window in SDRAM. Page 2 is accessed by the HOST CPU through memory address 180000h - 1BFFFFh. For further information on accessing the external SDRAM memory, see Section 8.1, “Accessing Memory using Direct Addressing” on page 66.

REG[0034h] bits 7-2 = Host SDRAM Page 2 Start Address bits [23:18]

REG[0036h] SDRAM Host Page 3 Start Address Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Reserved						Reserved	
7	6	5	4	3	2	1	0
SDRAM Host Page 3 Start Address bits 23-18						n/a	

bits 7-2 Host SDRAM Page 3 Start Address bits [23:18]
These bits specify bits 23-18 of the memory start address for Page 3, which re-directs Host CPU memory accesses to a 256K byte window in SDRAM. Page 3 is accessed by the HOST CPU through memory address 1C0000h - 1FFFFFh. For further information on accessing the external SDRAM memory, see Section 8.1, “Accessing Memory using Direct Addressing” on page 66.
REG[0036h] bits 7-0 = Host SDRAM Page 3 Start Address bits [23:18]

REG[0038h] through REG[0042h] are Reserved

These registers are Reserved and should not be written.

REG[0044h] Host Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Prefetch Buffer Disable	n/a				Reserved	n/a	
7	6	5	4	3	2	1	0
n/a				Reserved			Reserved

bit 15 Prefetch Buffer Disable
This bit enables/disables the prefetch buffer used for memory access acceleration. When the prefetch buffer is enabled, memory coherency issues may be possible (see Section 16.4, “Read Ahead Feature” on page 190).
When this bit = 0b, the prefetch buffer is enabled. (default)
When this bit = 1b, the prefetch buffer is disabled.

Note
1.The prefetch buffer must be enabled for indirect memory accesses.
2.This bit only applies for S1D13L04 revision 02h. For revisions 00h and 01h, the prefetch buffer is always enabled regardless of the setting of this bit.

bit 10 Reserved
This bit must set to 0b.

bits 3-1 Reserved
These bits must be set to 000b.

bit 0 Reserved
This bit must set to 0b.

10.4.2 System Control Registers

REG[0400h] through REG[0404h] are Reserved

These registers are Reserved and should not be written.

REG[0406h] Configuration Pins Status Register
Default = xxxxh — Read Only

15	14	13	12	11	10	9	8
n/a							CNF8 Status
7	6	5	4	3	2	1	0
CNF[7:0] Status							

bits 8-0 CNF[8:0] Status bits (Read Only)
These bits indicate the current status of the corresponding S1D13L04 configuration pins CNF[8:0]. The state of the CNF[8:0] pins only have an effect at the rising edge of RESET#. If the state of the CNF[8:0] pins changes after the rising edge of RESET#, it has no effect but the change will be indicated in this register. For a functional description of each configuration pin, see Section 5.3, “Summary of Configuration Options” on page 29.

REG[0408h] OSC1 Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							OSC1 Enable

bit 0 OSC1 Enable
This bit controls OSC1. A typical use for OSC1 is to provide the clock source for the panel interface when the PLL1 Source is not convenient. For a detailed diagram of the clock structure, refer to Figure 9-1: “Clock Diagram” on page 69.
When this bit = 0b, OSC1 is disabled. (default)
When this bit = 1b, OSC1 is enabled.

Note
1.If OSC1 is selected as the PLL2 source (REG[0440h] bits 1-0 = 00b), the LCD output must be disabled (REG[0830h] bit 0 = 0b) before disabling OSC1.
2.This bit is not affected by a software reset.
3.After enabling OSC1, wait until the oscillator becomes stable before performing the next register write. Note that the time required for the oscillator to become stable depends on the on-board crystal circuitry.

REG[040Ah] OSC2 Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							OSC2 Enable

bit 0 OSC2 Enable
This bit controls OSC2. For a detailed diagram of the clock structure, refer to Figure 9-1: "Clock Diagram" on page 69.
When this bit = 0b, OSC2 is disabled. (default)
When this bit = 1b, OSC2 is enabled.

Note
1.If OSC2 is selected as the PLL2 source (REG[0440h] bits 1-0 = 01b), the LCD output must be disabled (REG[0830h] bit 0 = 0b) before disabling OSC2.
2.This bit is not affected by software reset.
3.After enabling OSC2, wait until the oscillator becomes stable before performing the next register write. Note that the time required for the oscillator to become stable depends on the on-board crystal circuitry.

REG[040Ch] PLL1 Configuration Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
PLL1 RS bits 3-0				PLL1 VC bits 3-0			
7	6	5	4	3	2	1	0
Reserved		PLL1 V Divider bits 1-0		PLL1 N Multiplier bits 3-0			

Note
For example, the value of 8311h results in a PLL1 output of 100MHz when a 50MHz reference clock is input to PLL1.

bits 15-12 PLL1 RS bits [3:0]
These bits are used to configure the Low Pass Filter (LPF) resistance and should be set based on the frequency of the PLL1 reference clock.

Table 10-5: PLL1 RS Configuration

REG[040Ch] bits 15-12	PLL1 Reference Clock Frequency
0000b ~ 0111b	Reserved
1000b	20MHz ≤ fPLL1REFCLK ≤ 150MHz
1001b	Reserved
1010b	5MHz ≤ fPLL1REFCLK ≤ 20MHz
1011b ~ 1111b	Reserved

bits 11-8 PLL1 VC bits [3:0]

These bits set the analog adjustment pins for PLL1 and should be set according to the VCO frequency.

Table 10-6: PLL1 VC Configuration

REG[040Ch] bits 11-8	PLL1 VCO Frequency
0000b	Reserved
0001b	100MHz ≤ fVCO ≤ 120MHz
0010b	120MHz < fVCO ≤ 160MHz
0011b	160MHz < fVCO ≤ 200MHz
0100b	200MHz < fVCO ≤ 240MHz
0101b	240MHz < fVCO ≤ 280MHz
0110b	280MHz < fVCO ≤ 320MHz
0111b	320MHz < fVCO ≤ 360MHz
1000b	360MHz < fVCO ≤ 400MHz
1001b ~ 1111b	Reserved

bits 7-6 Reserved

The default value for these bits is 00b.

bits 5-4 PLL1 V Divider bits [1:0]

These bits are used to configure the VCO frequency which must be set between 100MHz and 400MHz. These bits should be set using the following formula.

fVCO = fPLL1OUT x VV

Where:
fVCO is the frequency of VCO, in MHz
fPLL1OUT is the desired PLL1 output frequency, in MHz (see N Multiplier bits)
VV is the value based on the V Divider bits as follows.

Table 10-7: VV Value

REG[040Ch] bits 5-4	VV Value
00b	Reserved
01b	2
10b	4
11b	8

Note

Normally VV is set to 2. When fPLL1OUT is lower than 50MHz, stabilize VCCO by setting VV to 4 or 8. Also, the PLL1 VC bits (REG[040Ch] bits 11-8) must be set according to the resulting fVCO. The frequency of VCO (fVCO) must always be within 100MHz ~ 400MHz.

bits 3-0 PLL1 N Multiplier bits [3:0]
These bits are used to determine the output frequency of PLL1 according to the following formula.

fPLL1OUT = fPLL1REFCLK x NN

Where:
fPLL1OUT is the desired PLL1 output frequency, in MHz
fPLL1REFCLK is the PLL1 reference clock input frequency, in MHz
NN is the N Multiplier value + 1

REG[040Eh] PLL1 Configuration Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
PLL1 Configuration 1 bits 15-8							
7	6	5	4	3	2	1	0
PLL1 Configuration 1 bits 7-0							

bits 15-0 PLL1 Configuration 1 bits [15:0]
These bits are used to configure PLL1 and should be set to the recommended value of 0040h.

REG[0410h] PLL1 Control Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							PLL1 Enable

bit 0 PLL1 Enable
This bit controls PLL1. PLL1 must be disabled before changing the PLL1 Configuration registers, REG[040Ch] ~ REG[040Eh].
When this bit = 0b, PLL1 is disabled and in a power down state. (default)
When this bit = 1b, PLL1 is enabled.

REG[0412h] is Reserved

This register is Reserved and should not be written.

REG[0414h] PLL2 Configuration Register 0
Default = 0000h Read/Write

PLL2 RS bits 3-0				PLL2 VC bits 3-0			
15	14	13	12	11	10	9	8
Reserved		PLL2 V Divider bits 1-0		PLL2 N Multiplier bits 3-0			
7	6	5	4	3	2	1	0

Note
For example, the value of A333h results in a PLL2 output of 23.8MHz when a 5.95MHz reference clock is input to PLL2.

bits 15-12 PLL2 RS bits [3:0]
These bits are used to configure the Low Pass Filter (LPF) resistance and should be set based on the frequency of the PLL2 reference clock.

Table 10-8: PLL2 RS Configuration

REG[0414h] bits 15-12	PLL2 Reference Clock Frequency
0000b ~ 0111b	Reserved
1000b	20MHz ≤ fPLL2REFCLK ≤ 150MHz
1001b	Reserved
1010b	5MHz ≤ fPLL2REFCLK ≤ 20MHz
1011b ~ 1111b	Reserved

bits 11-8 PLL2 VC bits [3:0]
These bits set the analog adjustment pins for PLL2 and should be set according to the VCO frequency.

Table 10-9: PLL2 VC Configuration

REG[0414h] bits 11-8	PLL2 VCO Frequency
0000b	Reserved
0001b	100MHz ≤ fVCO ≤ 120MHz
0010b	120MHz < fVCO ≤ 160MHz
0011b	160MHz < fVCO ≤ 200MHz
0100b	200MHz < fVCO ≤ 240MHz
0101b	240MHz < fVCO ≤ 280MHz
0110b	280MHz < fVCO ≤ 320MHz
0111b	320MHz < fVCO ≤ 360MHz
1000b	360MHz < fVCO ≤ 400MHz
1001b ~ 1111b	Reserved

bits 7-6 Reserved
The default value for these bits is 00b.

bits 5-4 PLL2 V Divider bits [1:0]

These bits are used to configure the VCO frequency which must be set between 100MHz and 400MHz. These bits should be set using the following formula.

fVCO = fPLL2OUT x VV

Where:
fVCO is the frequency of VCO, in MHz
fPLL2OUT is the desired PLL2 output frequency, in MHz (see N Multiplier bits)
VV is the value based on the V Divider bits as follows.

Table 10-10: VV Value

REG[0414h] bits 5-4	VV Value
00b	Reserved
01b	2
10b	4
11b	8

Note
Normally VV is set to 2. When fPLL2OUT is lower than 50MHz, stabilize VCCO by setting VV to 4 or 8. Also, the PLL2 VC bits (REG[0414h] bits 11-8) must be set according to the resulting fVCO. The frequency of VCO (fVCO) must always be within 100MHz ~ 400MHz.

bits 3-0 N Multiplier bits [3:0]

These bits are used to determine the output frequency of PLL2 according to the following formula.

fPLL2OUT = fPLL2REFCLK x NN

Where:
fPLL2OUT is the desired PLL2 output frequency, in MHz
fPLL2REFCLK is the PLL2 reference clock input frequency, in MHz
NN is the N Multiplier value + 1

REG[0416h] PLL2 Configuration Register 1
Default = 0000h Read/Write

PLL2 Configuration 1 bits 15-8							
15	14	13	12	11	10	9	8
PLL2 Configuration 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 PLL2 Configuration 1 bits [15:0]

These bits are used to configure PLL2 and should be set to the recommended value of 0040h.

REG[0418h] PLL2 Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							PLL2 Enable

bit 0 PLL2 Enable

This bit controls PLL2. PLL2 must be disabled before changing the PLL2 Configuration registers, REG[0414h] ~ REG[0416h].

When this bit = 0b, PLL2 is disabled and in a power down state. (default)

When this bit = 1b, PLL2 is enabled.

REG[041Ah] through REG[0422h] are Reserved

These registers are Reserved and should not be written.

REG[0424h] PLL1 Reference Clock Divide Select Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						PLL1 Reference Clock Divide Select bits 1-0	

bits 1-0 PLL1 Reference Clock Divide Select bits [1:0]

These bits determine the divide ratio applied to the clock used for the PLL1 reference clock. The PLL1 reference clock is derived from the clock input as selected by the CNF[8:7] pins at the rising edge of RESET#. The resulting clock can be used as the PLL1 reference clock (input to PLL1), or used as the PLL2 reference clock (input to PLL2). For detailed information on these options, refer to Section Chapter 9, “Clocks” on page 69.

Table 10-11: PLL1 Reference Clock Divide Ratio Selection

REG[0424h] bits 1-0	PLL1 Source Divide Ratio
00b	1:1 (Default after Reset)
01b	1:2
10b	1:4
11b	1:8

REG[0426h] PLL1 Control Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							PLL1 Reference Clock Select

bit 0 PLL1 Reference Clock Select
This bit selects whether the PLL1 reference clock goes through the divide controlled by REG[0424h] bits 1-0.
When this bit = 0b, the PLL1 reference clock is the clock selected by the CNF[8:7] pins. (default)
When this bit = 1b, the PLL1 reference clock is the divided clock output specified by REG[0424h] bits 1-0.

REG[0428h] PLL1 Control Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							PLL1 Output Enable

bit 0 PLL1 Output Enable
This bit controls the output of PLL1 which is used as the source for SDRAMCLK and SYSCLK (SYSCLK is automatically 1/2 of SDRAMCLK). For further information, refer to Section Chapter 9, “Clocks” on page 69.

Before enabling the PLL1 output, the PLL1 Configuration registers (REG[040Ch] ~ REG[040Eh]) must be configured with appropriate values. For further information, refer to the bit descriptions for REG[040Ch] ~ REG[040Eh].
When this bit = 0b, PLL1 output is disabled. (default)
When this bit = 1b, PLL1 output is enabled.

Note
When the PLL1 output is disabled, the PLL1 Reference Clock can be used as the SDRAMCLK and SYSCLK source.

To enable PLL1, the following sequence should be used.

1. Set the PLL1 for a target frequency, program REG[040Ch] ~ REG[040Eh]
2. Enable PLL1, set REG[0410h] bit 0 = 1b
3. Wait for PLL1 output to stabilize
4. Enable PLL1 output, REG[0428h] bit 0 = 1b

REG[042Ch] is Reserved

This register is Reserved and should not be written.

REG[042Eh] PWM Source Clock Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a			PWM Source Clock Enable	PWM Source Clock Divide Select bits 11-8			
PWM Source Clock Divide Select bits 7-0							
7	6	5	4	3	2	1	0

bit 12 PWM Source Clock Enable
This bit controls the clock used for the PWM Interface (PWMSRCCLK). The clock is derived from SYSCLK using the PWM Clock Divide Select bits, REG[042Eh] bits 11-0. For further information on PWMSRCCLK, refer to Section Chapter 9, “Clocks” on page 69.
When this bit = 0b, the PWM interface clock (PWMSRCCLK) is disabled.
When this bit = 1b, the PWM interface clock (PWMSRCCLK) is enabled.

bits 11-0 PWM Source Clock Divide Select bits [11:0]
These bits select the divide ratio used to determine the PWM Interface clock (PWMSRC-CLK). The source clock for the PWMSRCCLK is SYSCLK. For further information on PWMSRCCLK, refer to Section Chapter 9, “Clocks” on page 69.

Table 10-12: PWM Source Clock Divide Ratio Selection

REG[042Eh] bits 11-0	Divide Ratio
000h	1:1
001h	1:2
002h	1:3
2 2 2	2 2 2
FFDh	1:4094
FFEh	1:4095
FFFh	1:4096

REG[0430h] is Reserved

This register is Reserved and should not be written.

REG[0440h] PLL2 Control Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						PLL2 Source Select bits 1-0	

bits 1-0 PLL2 Source Select bits [1:0]
These bits select which clock is used for the PLL2 Source. The PLL2 Source is used to derive the clock used for the panel interface. For further information, see Section Chapter 9, “Clocks” on page 69.

Table 10-13: PLL2 Source Selection

REG[0440h] bits 1-0	PLL2 Source
00b (default)	OSC1 Clock
01b	OSC2 Clock
10b	CLKI3 Pin
11b	BUSCLK Pin

REG[0442h] PLL2 Control Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						PLL2 Reference Clock Divide Select bits 1-0	

bits 1-0 PLL2 Reference Clock Divide Select bits [1:0]
These bits determine the divide ratio applied to the PLL2 Reference clock. The PLL2 Reference Clock is derived from the clock input as selected by the PLL2 Source Select bits, REG[0440h] bits 1-0. The resulting clock is used as the PLL2 reference clock (input to PLL2). For detailed information on these options, refer to Section Chapter 9, “Clocks” on page 69.

Table 10-14: PLL2 Reference Clock Divide Ratio Selection

REG[0442h] bits 1-0	PLL2 Reference Clock Divide Ratio
00b (default)	1:1
01b	1:2
10b	1:4
11b	1:8

REG[0444h] PLL2 Control Register 2
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PLL2 Reference Clock Source Select bits 1-0		n/a	PLL2 Output Enable
7	6	5	4	3	2	1	0

bits 3-2 PLL2 Reference Clock Source Select bits [1:0]
These bits select which clock is the source for the PLL2 Reference clock. For further information, refer to Section Chapter 9, “Clocks” on page 69.

Table 10-15: PLL2 Reference Clock Source Selection

REG[0444h] bits 3-2	PLL2 Reference Clock Source
00b (default)	PLL2 Source
01b	PLL2 Divided Source (see REG[0442h] bits 1-0)
10b	Reserved
11b	Reserved

bit 0 PLL2 Output Enable
This bit controls the output of PLL2 which is used to derive LCDDCLK or LCDSCLK. For further information, refer to Section Chapter 9, “Clocks” on page 69.

Before enabling the PLL2 output, the PLL2 Configuration registers (REG[0414h] ~ REG[0416h]) must be configured with appropriate values. For further information, refer to the bit descriptions for REG[0414h] ~ REG[0416h].
When this bit = 0b, PLL2 output is disabled. (default)
When this bit = 1b, PLL2 output is enabled.

Note
When the PLL2 output is disabled, the PLL2 Reference Clock can be used as the LCDDCLK or LCDSCLK source.

To enable PLL2, the following sequence should be used.

1. Select which clock will be used for the PLL2 reference clock, REG[0444h] bits 3-2
2. Configure REG[0408h], REG[040Ah], REG[0440h], REG[0442h], if necessary
3. Set the PLL2 for a target frequency, program REG[0414h] ~ REG[0416h]
4. Enable PLL2, set REG[0418h] bit 0 = 1b
5. Wait for PLL2 output to stabilize
6. Enable PLL2 output, REG[0444h] bit 0 = 1b

REG[0446h] LCD Clock Control Register 0
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a			LCDDCLK Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 LCDDCLK Divide Select bits [4:0]
These bits select the divide ratio used to generate the LCD panel clock (LCDDCLK) from either the output of PLL2 or the PLL2 reference clock as selected by REG[0444h] bit 0. These bits must only be changed when the LCD interface is inactive, REG[0830h] bit 2 = 0b.

Table 10-16: LCDDCLK Divide Selection

REG[0446h] bits 4-0	LCDDCLK Divide Ratio	REG[0446h] bits 4-0	LCDDCLK Divide Ratio
00000b (00h)	Reserved	10000b (10h)	Reserved
00001b (01h)	1:2	10001b (11h)	1:18
00010b (02h)	Reserved	10010b (12h)	Reserved
00011b (03h)	1:4	10011b (13h)	1:20
00100b (04h)	Reserved	10100b (14h)	Reserved
00101b (05h)	1:6	10101b (15h)	1:22
00110b (06h)	Reserved	10110b (16h)	Reserved
00111b (07h)	1:8	10111b (17h)	1:24
01000b (08h)	Reserved	11000b (18h)	Reserved
01001b (09h)	1:10	11001b (19h)	1:26
01010b (0Ah)	Reserved	11010b (1Ah)	Reserved
01011b (0Bh)	1:12	11011b (1Bh)	1:28
01100b (0Ch)	Reserved	11100b (1Ch)	Reserved
01101b (0Dh)	1:14	11101b (1Dh)	1:30
01110b (0Eh)	Reserved	11110b (1Eh)	Reserved
01111b (0Fh)	1:16	11111b (1Fh)	1:32

REG[0448h] LCD Clock Control Register 1
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a			LCDSCLK Divide Select bits 4-0				
7	6	5	4	3	2	1	0

bits 4-0 LCDSCLK Divide Select bits [4:0]

These bits select the divide ratio used to generate the serial clock (LCDSCLK) for the LCD serial command interface, from either the output of PLL2 or the PLL2 reference clock as selected by REG[0444h] bit 0.

Table 10-17: LCDSCLK Divide Selection

REG[0448h] bits 4-0	LCDSCLK Divide Ratio	REG[0448h] bits 4-0	LCDSCLK Divide Ratio
00000b (00h)	Reserved	10000b (10h)	Reserved
00001b (01h)	1:2	10001b (11h)	1:18
00010b (02h)	Reserved	10010b (12h)	Reserved
00011b (03h)	1:4	10011b (13h)	1:20
00100b (04h)	Reserved	10100b (14h)	Reserved
00101b (05h)	1:6	10101b (15h)	1:22
00110b (06h)	Reserved	10110b (16h)	Reserved
00111b (07h)	1:8	10111b (17h)	1:24
01000b (08h)	Reserved	11000b (18h)	Reserved
01001b (09h)	1:10	11001b (19h)	1:26
01010b (0Ah)	Reserved	11010b (1Ah)	Reserved
01011b (0Bh)	1:12	11011b (1Bh)	1:28
01100b (0Ch)	Reserved	11100b (1Ch)	Reserved
01101b (0Dh)	1:14	11101b (1Dh)	1:30
01110b (0Eh)	Reserved	11110b (1Eh)	Reserved
01111b (0Fh)	1:16	11111b (1Fh)	1:32

REG[0460h] Software Reset Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Software Reset bits 15-8							
7	6	5	4	3	2	1	0
Software Reset bits 7-0							

bits 15-0 Software Reset bits [15:0]
These bits are used to perform a software reset of the S1D13L04. Writing a value of "A55Ah" to these bits causes all synchronous registers to be reset to their default values. A software reset via this register does not modify the contents of any external SDRAM memory.

Note
All data written to this register can be read back, except for A55Ah.

REG[0462h] Clock Enable Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a		Reserved		PCLK Enable	HCLK2 Enable	HCLK1 Enable	Reserved

bits 5-4 Reserved
The default value for these bits is 00b.

bit 3 PCLK Enable
This bit controls the internal clock used for read/write access to the synchronous registers. This bit must be enabled once the PLL becomes stable and before accessing any of the synchronous registers (see Section 10.1, "Register Mapping" on page 71). If no synchronous registers will be used, this bit can be disabled to achieve additional power savings.
When this bit = 0b, PCLK is disabled.
When this bit = 1b, PCLK is enabled.

bit 2 HCLK2 Enable
This bit controls the internal clock used for the LCDC and SDRAM. This bit must be enabled once the PLL becomes stable and before using either the LCDC or SDRAM. If **neither** of these will be used, this bit can be disabled to achieve additional power savings.
When this bit = 0b, HCLK2 is disabled.
When this bit = 1b, HCLK2 is enabled.

bit 1 HCLK1 Enable
This bit controls the internal clock used for Host and SDRAM access. This bit must be enabled once the PLL becomes stable and before accessing or configuring any of these interfaces. If **none** of these interfaces will be used, this bit can be disabled to achieve additional power savings.
When this bit = 0b, HCLK1 is disabled.
When this bit = 1b, HCLK1 is enabled.

bit 0 Reserved
The default value for this bit is 0b.

REG[0464h] GPIOC&D Pull-down Resistor Control Register
Default = 0000h Read/Write

n/a				GPIOD[3:0] Pull-down Control bits 3-0			
15	14	13	12	11	10	9	8
GPIOC[7:0] Pull-down Control bits 7-0							
7	6	5	4	3	2	1	0

bits 11-8 GPIOD[3:0] Pull-down Control bits [3:0]
These bits control the pull-down resistor for each corresponding GPIOD[3:0] pin. For information on the possible usages of the GPIOD[3:0] pins, refer to Section 5.2.4, “GPIO / Multi Function Interface” on page 23 and Section 5.6, “GPIO Pin Mapping” on page 34.
When this bit = 0b, the corresponding pull-down resistor is enabled. (default after reset)
When this bit = 1b, the corresponding pull-down resistor is disabled.

bits 7-0 GPIOC[7:0] Pull-down Control bits [7:0]
These bits control the pull-down resistor for each corresponding GPIOC[7:0] pin. For information on the possible usages of the GPIOC[7:0] pins, refer to Section 5.2.4, “GPIO / Multi Function Interface” on page 23 and Section 5.6, “GPIO Pin Mapping” on page 34.
When this bit = 0b, the corresponding pull-down resistor is enabled. (default after reset)
When this bit = 1b, the corresponding pull-down resistor is disabled.

REG[0466h] is Reserved

This register is Reserved and should not be written.

REG[0468h] GPIOG Pull-down Resistor Control Register
Default = 0000h Read/Write

n/a		Reserved					
15	14	13	12	11	10	9	8
n/a			GPIOG[4:0] Pull-down Control bits 4-0				
7	6	5	4	3	2	1	0

bits 13-8 Reserved
The default value for these bits is 000000b.

bits 4-0 GPIOG[4:0] Pull-down Control bits [4:0]
These bits control the pull-down resistor for each corresponding GPIOG[4:0] pin. For information on the possible usages of the GPIOG[4:0] pins, refer to Section 5.2.2, “LCD Interface” on page 20 and Section 5.6, “GPIO Pin Mapping” on page 34.
When this bit = 0b, the corresponding pull-down resistor is enabled. (default after reset)
When this bit = 1b, the corresponding pull-down resistor is disabled.

Note
The GPIOG[4:0] pins are used by some panel types and may not be available for use as general purpose IO pins.

REG[046Ah] MEMDQ Pull-down Resistor Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
MEMDQ[15:8] Pull-down Control bits 15-8							
7	6	5	4	3	2	1	0
MEMDQ[7:0] Pull-down Control bits 7-0							

bits 15-0 MEMDQ[15:0] Pull-down Control bits [15:0]
These bits control the pull-down resistor for each corresponding MEMDQ[15:0] pin. For detailed pin information, refer to Section 5.2.3, “SDRAM Interface” on page 22.
When this bit = 0b, the corresponding pull-down resistor is enabled. (default after reset)
When this bit = 1b, the corresponding pull-down resistor is disabled.

REG[046Ch] is Reserved

This register is Reserved and should not be written.

REG[046Eh] CNF Pull-down Resistor Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							CNF8 Pull-down Control bit 8
7	6	5	4	3	2	1	0
CNF[7:0] Pull-down Control bits 7-0							

bits 8-0 CNF[8:0] Pull-down Control bits [8:0]
These bits control the pull-down resistor for each corresponding CNF[8:0] pin. The CNF[8:0] pins are used for configuration of the S1D13L04 (see Section 5.3, “Summary of Configuration Options” on page 29). The configuration information is latched at RESET. Then if necessary, the pull-down resistor can be disabled in order to cut constant current via the pull-down resistor (i.e. when a pull-up resistor is attached on a CNF pin).
When this bit = 0b, the corresponding pull-down resistor is enabled. (default after reset)
When this bit = 1b, the corresponding pull-down resistor is disabled.

REG[0470h] Power Down Mode Control Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable

bit 0 Power Save Mode Enable
This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13L04 is operating normally. When power save mode is enabled, the S1D13L04 is operating in a power efficient state. In this state, all IO clocks are disabled, but the Host interface bus clock is still enabled.
When this bit = 0b, power save mode is disabled.
When this bit = 1b, power save mode is enabled.

Note
When Power Save Mode is enabled, synchronous registers (see Section 10.1, “Register Mapping” on page 71) and SDRAM memory must not be accessed.

REG[0472h] Bus Time-out Reset Control Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					Bus Time-Out Reset Interrupt Flag (RO)	Bus Time-out Reset Interrupt Disable	Bus Time-out Reset Disable

bit 2 Bus Time-out Reset Interrupt Flag (Read Only)
This bit indicates whether a bus time-out reset has occurred. This bit is masked by the Bus Time-out Reset Interrupt Enable bit, REG[0472h] bit 1, and is cleared by disabling the Bus Time-out Reset Interrupt Enable, REG[0472h] bit 1 = 1b.
When this bit = 0b, a bus time-out reset has not occurred.
When this bit = 1b, a bus time-out reset has occurred.

bit 1 Bus Time-out Reset Interrupt Disable
This bit controls the bus time-out reset interrupt. The status of the bus time-out reset interrupt is indicated by the Bus Time-out Reset Interrupt Flag bit, REG[0472h] bit 2.
When this bit = 0b, the bus time-out reset interrupt is enabled.
When this bit = 1b, the bus time-out reset interrupt is disabled.

bit 0 Bus Time-out Reset Disable
This bit controls the bus time-out reset function which can reset the S1D13L04 after a bus time-out occurs. For further information, see Section 16.2, “Host Bus Time-out Function” on page 184.
When this bit = 0b, the bus time-out reset function is enabled and will release WAIT#, if WAIT# is held for more than 2048-3072 PLL1 reference clocks (as selected by CNF[8:7]), before resetting the S1D13L04.
When this bit = 1b, the bus time-out reset function is disabled. (default)

REG[04A0h] through REG[04A2h] are Reserved

These registers are Reserved and should not be written.

10.4.3 LCD Panel Configuration Registers

Note
Some pins used by the LCD panel interface are multiplexed with GPIO function pins. Therefore, before enabling the LCD panel interface, the appropriate GPIO pins must be configured for use by the LCD panel interface. For a summary of GPIO pin usage, see Section 5.6, “GPIO Pin Mapping” on page 34.

REG[0800h] LCD Panel Type Select Register
Default = 0000h — Read/Write

Reserved					Panel Data Bus Width bits 2-0		
15	14	13	12	11	10	9	8
FPSHIFT Polarity Select	n/a				TFT Panel Type Select bits 2-0		
7	6	5	4	3	2	1	0

bits 15-11 Reserved
The default value for these bits is 00000b.

bits 10-8 Panel Data Bus Width bits [2:0]
These bits are used to select the data bus width of the selected panel.

Table 10-18: Panel Data Bus Width Selection

REG[0800h] bits 10-8	Panel Data Bus Width
	TFT Panel
000b	Reserved
001b	16-bit
010b	18-bit
011b	Reserved
100b - 111b	Reserved

bit 7 FPSHIFT Polarity Select
This bit selects the polarity of the shift clock for RGB type panels (inverts FPSHIFT).

Note
The polarity of the shift clock (FPSHIFT) cannot be changed while LCD Output is active (REG[0830h] bit 1 = 1b). If a change in polarity is required, use the following steps.
1. Disable LCD output (REG[0830h] bit 0 = 0b)
2. Wait until the LCD interface is no longer active (REG[0830h] bit 2 = 0b)
3. Set the desired polarity of the shift clock (REG[0800h] bit 7)
4. Enable LCD output again (REG[0830h] bit 0 = 1b)

bits 2-0 TFT Panel Type Select bits [2:0]

When a TFT panel is selected (REG[0800h] bit 14 = 0b), these bits select the type of TFT panel connected to the LCD panel interface. For TFT panel types using a Serial Command Interface, the GPIOG[4:0] pins must be configured for the appropriate function using REG[0C1Ah]. For a summary of the functions, see Section 5.6, “GPIO Pin Mapping” on page 34.

Table 10-19: TFT Panel Type Selection

REG[0800h] bits 2-0	TFT Panel Type Select
000b	General TFT/ND-TFD
001b - 111b	Reserved

REG[0802h] LCD Horizontal Total Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Horizontal Total bits 11-8			
7	6	5	4	3	2	1	0
Horizontal Total bits 7-0							

bits 11-0 Horizontal Total bits [11:0]

These bits specify the Horizontal Total (FPLINE) period, in pixel clock periods. The Horizontal Total is the sum of the Horizontal Display Period and the Horizontal Non-Display Period.

REG[0802h] bits 11-0 = Horizontal Total Period - 1

Note

This register must be programmed such that the following formula is valid.

HT ≥ HDP + HNDP

REG[0804h] LCD Horizontal Display Period Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					Horizontal Display Period bits 10-8		
7	6	5	4	3	2	1	0
Horizontal Display Period bits 7-0							

bits 10-0 Horizontal Display Period bits [10:0]

These bits specify the Horizontal Display Period, in 2 pixel resolution. The Horizontal Display Period must be less than the Horizontal Total to allow for sufficient Horizontal Non-Display Period.

REG[0804h] bits 10-0 = (Horizontal Display Period ÷ 2) - 1

Note

This register must be programmed such that the following formula is valid.

HT ≥ HDP + HNDP

REG[0806h] LCD Horizontal Display Period Start Position Register

Default = 0000h — Read/Write

n/a				Horizontal Display Period Start Position bits 11-8			
15	14	13	12	11	10	9	8
Horizontal Display Period Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Horizontal Display Period Start Position bits [11:0]

These bits specify the Horizontal Display Period Start Position, in pixel clock periods.

REG[0806h] bits 11-0 = Horizontal Display Period Start Position - 1

REG[0808h] LCD Horizontal Pulse Width Register

Default = 0000h — Read/Write

Horizontal Polarity Select	n/a						Horizontal Pulse Width bit 8
15	14	13	12	11	10	9	8
Horizontal Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bit 15 Horizontal Polarity Select

This bit selects the polarity of the horizontal sync signal (FPLINE).

When this bit = 0b, the horizontal sync signal (FPLINE) is active low. (default)

When this bit = 1b, the horizontal sync signal (FPLINE) is active high.

bits 8-0 Horizontal Pulse Width bits [8:0]

These bits specify the pulse width of the horizontal sync signal (FPLINE), in pixel clock periods.

REG[0808h] bits 8-0 = Horizontal Pulse Width - 1

REG[080Ah] LCD Horizontal Pulse Start Position Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Horizontal Pulse Start Position bits 11-8			
7	6	5	4	3	2	1	0
Horizontal Pulse Start Position bits 7-0							

bits 11-0 Horizontal Pulse Start Position bits [11:0]

These bits specify the start position of the horizontal sync pulse (FPLINE), in pixel clock period.

REG[080Ah] bits 11-0 = Horizontal Pulse Start Position

REG[080Ch] LCD Vertical Total Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Vertical Total bits 11-8			
7	6	5	4	3	2	1	0
Vertical Total bits 7-0							

bits 11-0 Vertical Total bits [11:0]

These bits specify the Vertical Total (FPFRAME) period, in lines. The Vertical Total is the sum of the Vertical Display Period and the Vertical Non-Display Period.

REG[080Ch] bits 11-0 = Vertical Total Period in lines - 1

Note

These bits must be set to a value greater than 000h.

REG[080Eh] LCD Vertical Display Period Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Vertical Display Period bits 11-8			
7	6	5	4	3	2	1	0
Vertical Display Period bits 7-0							

bits 11-0 Vertical Display Period bits [11:0]

These bits specify the Vertical Display Period, in lines. The Vertical Display Period must be less than the Vertical Total to allow for sufficient Vertical Non-Display Period.

REG[080Eh] bits 11-0 = Vertical Display Period in lines - 1

Note

These bits must be set to a value less than FFFh.

REG[0810h] LCD Vertical Display Period Start Position Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a				Vertical Display Period Start Position bits 11-8			
7	6	5	4	3	2	1	0
Vertical Display Period Start Position bits 7-0							

bits 11-0 Vertical Display Period Start Position bits [11:0]
These bits specify the Vertical Display Period Start Position, in lines.
REG[0810h] bits 11-0 = Vertical Display Period Start Position in lines

REG[0812h] LCD Vertical Pulse Width Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Vertical Polarity Select	n/a						
7	6	5	4	3	2	1	0
n/a			Vertical Pulse Width bits 4-0				

bit 15 Vertical Polarity Select
This bit selects the polarity of the vertical sync signal (FPFRAME).
When this bit = 0b, the vertical sync signal (FPFRAME) is active low. (default)
When this bit = 1b, the vertical sync signal (FPFRAME) is active high.

bits 4-0 Vertical Pulse Width bits [4:0]
These bits specify the pulse width of the vertical sync signal (FPFRAME), in lines.
REG[0812h] bits 4-0 = Vertical Pulse Width in lines - 1

REG[0814h] Vertical Pulse Start Position Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a				Vertical Pulse Start Position bits 11-8			
7	6	5	4	3	2	1	0
Vertical Pulse Start Position bits 7-0							

bits 11-0 Vertical Pulse Start Position bits [11:0]
These bits specify the start position of the vertical sync pulse (FPFRAME), in lines.
REG [0814h] bits 11-0 = Vertical Pulse Start Position in lines

REG[0816h] LCD Serial Interface Configuration Register

Default = 0000h — Read/Write

Reserved	n/a						
15	14	13	12	11	10	9	8
LCD Serial Command Type bits 2-0			LCD Serial Command Direction	n/a		LCD Serial Clock Phase	LCD Serial Clock Polarity
7	6	5	4	3	2	1	0

bit 15 Reserved

The default value for this bit is 0b.

bits 7-5 LCD Serial Command Type bits [2:0]

These bits determine the serial command type. For AC timing information, see Section 7.6.2, “ND-TFD 8-Bit Serial Interface Timing” on page 57, Section 7.6.3, “ND-TFD 9-Bit Serial Interface Timing” on page 58, Section 7.6.4, “a-Si TFT Serial Interface Timing” on page 59, and Section 7.6.5, “uWIRE Serial Interface Timing” on page 60.

Table 10-20: LCD Serial Command Type Selection

REG[0816h] bits 7-5	LCD Serial Command Type
000b	ND-TFT 4 pin Serial (8-bit serial data)
001b	ND-TFD 3 pin Serial (9-bit serial data)
010b	a-Si TFT Serial (8-bit serial data)
011b	Reserved
100b	µWire serial (16-bit serial data)
101b	24-bit serial data
110b ~ 111b	Reserved

bit 4 LCD Serial Command Direction

This bit determines the serial command bit direction.

When this bit = 0b, the MSB (most significant bit) is first. (default)

When this bit = 1b, the LSB (least significant bit) is first.

Note

For details on timing, see Section 7.6, “Panel Interface Timing” on page 53 and refer to the appropriate serial interface.

bit 1 LCD Serial Clock Phase

This bit specifies the serial clock phase. For a summary of the serial clock phase and polarity settings, see Table 10-21:, “Serial Clock Phase and Polarity,” on page 106.

Note

For details on timing, see Section 7.6, “Panel Interface Timing” on page 53 and refer to the appropriate serial interface.

bit 0 LCD Serial Clock Polarity
This bit specifies the serial clock polarity. For a summary of the serial clock phase and polarity settings, see Table 10-21:, “Serial Clock Phase and Polarity,” on page 106.

Table 10-21: Serial Clock Phase and Polarity

REG[0816h] bit 1	REG[0816h] bit 0	Valid Data	Clock Idling Status
0b	0b	Rising edge of Serial Clock	Low
	1b	Falling edge of Serial Clock	High
1b	0b	Falling edge of Serial Clock	Low
	1b	Rising edge of Serial Clock	High

Note
For details on timing, see Section 7.6, “Panel Interface Timing” on page 53 and refer to the appropriate serial interface.

REG[0818h] LCD Status Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
VSYNC Interrupt Enable	n/a			VSYNC Interrupt Status	VSYNC Interrupt Mask Disable	n/a	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a							VNDP Status (RO)

bit 15 VSYNC Interrupt Enable
This bit controls whether the VSYNC Interrupt is output to the Host CPU interface.
When this bit = 0b, the interrupt status is not output to the Host CPU.
When this bit = 1b, the interrupt status is output to the Host CPU.

bit 11 VSYNC Interrupt Status
This bit indicates the status of the VSYNC Interrupt. The VSYNC Interrupt can be masked (or disabled) using the VSYNC Interrupt Mask Disable bit, REG[0818h] bit 10.
When this bit = 0b, a VSYNC Interrupt has not occurred.
When this bit = 1b, a VSYNC Interrupt has occurred.

To clear this bit, write a 1b to this bit.

bit 10 VSYNC Interrupt Mask Disable
This bit determines whether the VSYNC Interrupt is masked. The status of the VSYNC Interrupt is indicated by the VSYNC Interrupt Status bit, REG[0818h] bit 11.
When this bit = 0b, the VSYNC interrupt is masked (the interrupt will not be set).
When this bit = 1b, the VSYNC interrupt is not masked (the interrupt will be set).

bit 0 VNDP Status (Read Only)
This bit indicates whether the LCD panel is in a Vertical Display Period or a Vertical Non-Display Period. To use this bit, the configured VNDP must be greater than 1 line.
When this bit = 0b, the LCD panel output is in a Vertical Display Period.
When this bit = 1b, the LCD panel output is in a Vertical Non-Display Period.

Note
This bit indicates the period between the last horizontal line of data output and 1 line before data output starts again.

REG[081Ah] LCD VSYNC Interrupt Delay Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a				LCD VSYNC Interrupt Delay bits 11-8			
LCD VSYNC Interrupt Delay bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 LCD VSYNC Interrupt Delay bits [11:0]
These bits specify the VSYNC interrupt assertion timing delay from the start of the frame, in lines.

These bits specify the delay, in lines, for the VSYNC interrupt from the start of FPFRAME. The delay can be used by software to prevent display tearing by ensuring that display updates are not overlapping the current line being displayed.

REG[081Ch] LCD Serial Command/Parameter Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
LCD Serial Command bits 7-0							
LCD Serial Parameter bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 LCD Serial Command bits [7:0]
These bits are used for 24-bit serial interface and uWire serial interface panels only.
When either of these interfaces are enabled (see REG[0816h] bits 7-5), these bits are used as bits 7-0 (CD[15:8]) of the command to the LCD serial interface. For the other panels, bit 8 is only used to determine whether the LCD Serial Parameter bits (REG[081Ch] bits 7-0) contain a command or data.

Note
The serial command is issued to the panel module once REG[081Ch] is written.

bits 7-0 LCD Serial Parameter bits [7:0]
These bits specify the parameter to the LCD serial interface. When 24-bit serial interface mode is enabled (REG[0816h] bits 7-5 = 101b), these bits are used as bits 7-0 (CD[7:0]) of the command to the LCD serial interface.

REG[081Eh] Serial Command Register
Default = 0000h — Read/Write

LCD Serial Command bits 15-8							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

bits 15-8 LCD Serial Command bits [15:8]
These bits are used for 24-bit serial interface panels only. When 24-bit serial interface mode is enabled (REG[0816h] bits 7-5 = 101b), these bits are used as bits 15-8 (CD[23:16]) of the command to the LCD serial interface. The serial command is issued to the panel module once REG[081Ch] is written. Therefore, these bits must be set before writing to REG[081Ch].

bits 7-0 Reserved
The default value for these bits is 00000000b.

REG[0820h] through REG[082Eh] are Reserved

These registers are Reserved and should not be written.

10.4.4 LCD Display Mode Registers

Note
Some pins used by the LCD panel interface are multiplexed with GPIO function pins. Therefore, before enabling the LCD panel interface, the appropriate GPIO pins must be configured for use by the LCD panel interface. For a summary of GPIO pin usage, see Section 5.6, “GPIO Pin Mapping” on page 34.

REG[0830h] Display Mode Setting Register 0
Default = 0000h — Read/Write

Reserved	n/a	Reserved		n/a	Display Mode Select bits 2-0		
15	14	13	12	11	10	9	8
LCD Software Reset (WO)	Display Blank Enable	Video Invert Enable	Reserved	n/a	LCD Output Status (RO)	n/a	LCD Output Enable
7	6	5	4	3	2	1	0

Note
Any changes to bits in this register take effect at the end of the current frame.

bit 15 Reserved
The default value for this bit is 0b.

bits 13-12 Reserved
The default value for these bits are 00b.

bits 10-8 Display Mode Select [2:0]

These bits select the display mode. To avoid any visual tearing, Display Mode settings should only be changed during non-display period which is indicated by REG[0818h] bit 0 or the interrupt status (see REG[0818h] bit 11). For further details, refer to the register descriptions for REG[0818h] bit 15, REG[0818h] bit 10, and REG[081Ah].

Table 10-22: Display Mode Selection

REG[0830h] bits 10-8	Display Mode
000b	Main Window Only
001b	Main Window + PIP1 Window (see Note)
010b	Main Window + PIP2 Window
011b	Main Window + PIP1 + PIP2 Window (see Note)
100b - 111b	Reserved

Note

The PIP1 window Y start position (REG[084Eh] bits 10-0), must be set to 0 before disabling the PIP1 window.

bit 7 LCD Software Reset (Write Only)

This bit initiates a software reset of the LCD control module. All LCD pins are reset to their reset states and REG[0800h] ~ REG[086Eh] are reset to their default values.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit performs a software reset of the LCD control module.

bit 6 Display Blank Enable

This bit blanks the display by forcing all display data outputs low. All display control signals remain unchanged.
When this bit = 0b, the display is active.
When this bit = 1b, the display is blanked.

bit 5 Video Invert Enable

This bit inverts the display by inverting all display data outputs. All display control signals remain unchanged. This bit has no effect if display blank is enabled, REG[0830h] bit 6 = 1b.
When this bit = 0b, the display data is unchanged (normal).
When this bit = 1b, the display data is inverted.

bit 4 Reserved

The default value for this bit is 0b.

bit 2 LCD Output Status (Read Only)

This bit indicates whether the S1D13L04 is outputting to the LCD interface.
When this bit = 0b, LCD output is not active.
When this bit = 1b, LCD output is active.

bit 0 LCD Output Enable

This bit controls whether the LCD controls signals and display data are output on the LCD interfaces. REG[0800h] bits 2-0 control whether the LCD interface is selected for display data output.
When this bit = 0b, LCD output is disabled.
When this bit = 1b, LCD output is enabled.

REG[0832h] Display Mode Setting Register 1
Default = 0000h Read/Write

PIP Window Priority Control	n/a			PIP2 Window ARGB Format Select	PIP2 Window Bpp Select bits 2-0		
15	14	13	12	11	10	9	8
n/a	PIP1 Window Bpp Select bits 2-0			n/a	Main Window Bpp Select bits 2-0		
7	6	5	4	3	2	1	0

bit 15 PIP Window Priority Control
This bit determines which PIP window is the top layer.
When this bit = 0b, PIP2 is the top layer. (default)
When this bit = 1b, PIP1 is the top layer.

bit 11 PIP2 Window ARGB Format Select
This bit selects the format that PIP2 window display data is stored in the display buffer.
When this bit = 0b, display data is stored as RGB. (normal)
When this bit = 1b, display data is stored as ARGB.

bits 10-8 PIP2 Window Bpp Select bits [2:0]
These bits select the color depth, in bits-per-pixel, for the PIP2 window. The following table lists the available color depths for the PIP2 window, and how the data is stored in the display buffer. The display data can be stored as either RGB or ARGB based on the setting of the PIP2 Window ARGB Format Select bit, REG[0832h] bit 11.

Table 10-23: PIP2 Window Bpp Selection

REG[0832h] bits 10-8	Color Depth (bpp)	RGB Format REG[0832h] bit 11 = 0b	ARGB Format REG[0832h] bit 11 = 1b
000b	8 bpp	RGB 3:3:2	Reserved
001b	16 bpp	RGB 5:6:5	ARGB 1:5:5:5
010b	16 bpp	Reserved	ARGB 4:4:4:4
011b	32 bpp	RGB 8:8:8 Unpacked	Reserved
100b	32 bpp	Reserved	ARGB 8:8:8:8
101b ~ 111b	Reserved		

bits 6-4 PIP1 Window Bpp Selection bits [2:0]

These bits select the color depth, in bits-per-pixel, for the PIP1 window. The following table lists the available color depths for the PIP1 window, and how the data is stored in the display buffer.

Table 10-24: PIP1 Window Bpp Selection

REG[0832h] bits 6-4	Color Depth (bpp)	Display Buffer Format
000b	8 bpp	RGB 3:3:2
001b	16 bpp	RGB 5:6:5
010b	Reserved	
011b	32 bpp	RGB 8:8:8 Unpacked
100b	Reserved	
101b ~ 111b	Reserved	

bits 2-0 Main Window Bpp Select bits [2:0]

These bits select the color depth, in bits-per-pixel, for the Main Window. The following table lists the available color depths for the main window, and how the data is stored in the display buffer.

Table 10-25: Main Window Bpp Selection

REG[0832h] bits 2-0	Color Depth (bpp)	Display Buffer Format
000b	8 bpp	RGB 3:3:2
001b	16 bpp	RGB 5:6:5
010b	Reserved	
011b	32 bpp	RGB 8:8:8 Unpacked
100b	Reserved	
101b ~ 111b	Reserved	

REG[0834h] Display Mode Setting Register 2

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Reserved					PIP2 Window Mirror Enable	PIP2 Window SwivelView Mode Select bits 1-0	
7	6	5	4	3	2	1	0
n/a					View Port (Main + PIP1) Mirror Enable	View Port (Main + PIP1) SwivelView Select bits 1-0	

bits 15-11 Reserved

The default value for these bits is 00000b.

bit 10 PIP2 Window Mirror Enable

This bit controls the Mirror display function for the PIP2 window. For further information on the mirror display function, see Section 13.2, “Mirror Display” on page 167.

When this bit = 0b, mirror display for the PIP2 window is disabled.

When this bit = 1b, mirror display for the PIP2 window is enabled.

bits 9-8 PIP2 Window SwivelView Mode Select bits [1:0]
These bits select the SwivelView mode of the PIP2 window. SwivelView is a counter-clockwise hardware rotation of the PIP2 window. For further information on the Swivel-View function, see Section 13.1, “SwivelView™” on page 164.

Table 10-26: PIP2 Window SwivelView Mode Selection

REG[0834h] bits 9-8	PIP2 Window Swivel View Mode
00b	Normal (0°)
01b	Reserved
10b	180°
11b	Reserved

bit 2 View Port (Main + PIP1) Mirror Enable
This bit controls the Mirror display function for the View Port (Main + PIP1 window). For further information on the mirror display function, see Section 13.2, “Mirror Display” on page 167.
When this bit = 0b, mirror display for the View Port is disabled.
When this bit = 1b, mirror display for the View Port is enabled.

bits 1-0 View Port (Main + PIP1) SwivelView Mode Select bits [1:0]
These bits select the SwivelView mode of the View Port (Main + PIP1). SwivelView is a counter-clockwise hardware rotation of the View Port. For further information on the SwivelView function, see Section 13.1, “SwivelView™” on page 164.

Table 10-27: View Port (Main + PIP1) SwivelView Mode Selection

REG[0834h] bits 1-0	View Port (Main + PIP1) SwivelView Mode
00b	Normal (0°)
01b	Reserved
10b	180°
11b	Reserved

REG[0836h] PIP2 Window Alpha Blending Mode Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a	PIP2 Alpha Map Value Shift Enable	PIP2 Alpha Pixel Swap	PIP2 Window Transparent Enable	n/a	PIP2 Window Alpha Blending Mode bits 1-0		PIP2 Window Alpha Blending Enable
Constant Alpha Value bits 7-0							
7	6	5	4	3	2	1	0

bit 14 PIP2 Alpha Map Value Shift Enable

This bit shifts the alpha map value by one bit to the right. For example, if ARGB 1:5:5:5 format is selected, the converted 8-bit alpha value is either 0h (0% blend) or 80h (50% blend). When this bit is set to 1b, the new alpha value becomes either 0h or C0h (75% blend) respectively.

When this bit = 0b, the alpha map value is not shifted.

When this bit = 1b, the alpha map value is shifted.

Note

This bit has no effect when the alpha map value is 0h or when constant alpha blending is enabled, REG[0836h] bits 10-9 = 00b.

bit 13 PIP2 Alpha Pixel Swap

This bit controls whether the two pixels are swapped in the alpha blending formula listed in REG[0836h] bits 10-9.

When this bit = 0b, PIP2 alpha pixel swapping is disabled.

When this bit = 1b, PIP2 alpha pixel swapping is enabled and the formula changes as follows.

Output Pixel Color = $(Pm \times \alpha) + (Pp \times (1 - \alpha)$

$\alpha = \alpha m \times \alpha c$

Where:

Pm = colors of a pixel in the Main Window

Pp = colors of a pixel in the PIP2 Window

αm = an alpha value in the alpha map

αc = a constant alpha value specified by REG[0836h] bits 7-0

bit 12 PIP2 Window Transparent Enable

This bit controls PIP2 window transparency.

When this bit = 0b, transparency is disabled.

When this bit = 1b, transparency is enabled.

bits 10-9 PIP2 Window Alpha Blending Mode bits [1:0]
These bits determine the alpha blending mode used for the PIP2 window.

Table 10-28: PIP2 Window Alpha Blending Mode Selection

REG[0836h] bits 10-9	PIP2 Window Alpha Blending Mode
00b	Constant Alpha Blending
01b	Blending with Alpha Map (ARGB Format)
10b	Blending with Constant Value and Alpha Map (ARGB Format)
11b	Reserved

Alpha blending is defined by the following formula,
Output Pixel Colors = (Pp x α) + (Pm x (1 - α)
$\alpha = \alpha m \times \alpha c$

Where:
Pm = colors of a pixel in the Main Window
Pp = colors of a pixel in the PIP2 Window
αm = an alpha value in the alpha map
αc = a constant alpha value specified by REG[0836h] bits 7-0

If these bits are 00b, $\alpha=\alpha c$. If these bits are 01b, $\alpha = \alpha m$. The α value is normalized to 1 and ranges from 0 to 1. The αm is quantized by the bit width of the alpha value in the ARGB format pixel data, specified by REG[0832h] bits 10-8. For example, if ARGB 1:5:5:5 format is selected, αm is 0 or 0.5 in decimal. If ARGB 4:4:4:4 is selected, αm ranges from 0 to 15/16 in 1/16 increments. If ARGB 8:8:8:8 format is selected, αm ranges from 0 to 255/256 in 1/256 increments.

When alpha blending with alpha map values, REG[0836h] bits 10-9 = 01b or 10b, then ARGB data format must be enabled, REG[0832h] bit 11 = 1b.

bit 8 PIP2 Window Alpha Blending Enable
This bit controls the alpha blending function for the PIP2 window.
When this bit = 0b, alpha blending is disabled.
When this bit = 1b, alpha blending is enabled.

bits 7-0 Constant Alpha Value bits [7:0]
These bits specify the constant alpha value used when the PIP2 Window alpha blending mode requires a constant alpha value (REG[0836h] bits 10-9 = 00b or 10b).

REG[0838h] PIP2 Window Transparent Key Color Red Register

Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
PIP2 Window Transparent Key Color Red bit 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Window Transparent Key Color Red bits [7:0]
These bits only have an effect when the PIP2 Window Transparent Enable bit is set, REG[0836h] bit 12 = 1b. These bits set the red color component of the Transparent Key Color.

Note
To match the color of a pixel in the Main Window with a format using less than 8-bits for the red component (i.e. 8 or 16 bpp), the least significant bits must be padded with 0.

REG[083Ah] PIP2 Window Transparent Key Color Green Register

Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
PIP2 Window Transparent Key Color Green bit 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Window Transparent Key Color Green bits [7:0]
These bits only have an effect when the PIP2 Window Transparent Enable bit is set, REG[0836h] bit 12 = 1b. These bits set the green color component of the Transparent Key Color.

Note
To match the color of a pixel in the Main Window with a format using less than 8-bits for the green component (i.e. 8 or 16 bpp), the least significant bits must be padded with 0.

REG[083Ch] PIP2 Window Transparent Key Color Blue Register

Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
PIP2 Window Transparent Key Color Blue bit 7-0							
7	6	5	4	3	2	1	0

bits 7-0 PIP2 Window Transparent Key Color Blue bits [7:0]
These bits only have an effect when the PIP2 Window Transparent Enable bit is set, REG[0836h] bit 12 = 1b. These bits set the blue color component of the Transparent Key Color.

Note
To match the color of a pixel in the Main Window with a format using less than 8-bits for the blue component (i.e. 8 or 16 bpp), the least significant bits must be padded with 0.

REG[083Eh] Gamma Control Register

Default = 0000h — Read/Write

n/a	Main Window Gamma LUT Bypass Enable	PIP2 Window Gamma LUT Bypass Enable	PIP1 Window Gamma LUT Bypass Enable	Gamma LUT PIP Window Select bits 1-0		Gamma LUT Write Color Select bits 1-0	
15	14	13	12	11	10	9	8
n/a		Gamma LUT Display Bank Select bits 1-0		Input Data Extra Bit Expansion Enable	Input Data Extra Bit Clip Disable	Gamma LUT Address Auto Increment	Gamma LUT Enable
7	6	5	4	3	2	1	0

bit 14 Main Window Gamma LUT Bypass Enable

This bit controls whether the Gamma LUT, as selected by the Gamma LUT Display Bank Select bits (REG[083Eh] bits 5-4), is used to determine the main window image. When the Gamma LUT is bypassed, gamma correction does not take place.

When this bit = 0b, the Gamma LUT is used (not bypassed).

When this bit = 1b, the Gamma LUT is not used (bypassed).

Note

The Main window must not be Gamma LUT enabled if the window is not selected for gamma display in REG[083Eh] bits 11-10 and bits 5-4.

bit 13 PIP2 Window Gamma LUT Bypass Enable

This bit controls whether the Gamma LUT, as selected by the Gamma LUT Display Bank Select bits (REG[083Eh] bits 5-4), is used to determine the PIP2 window image. When the Gamma LUT is bypassed, gamma correction does not take place.

When this bit = 0b, the Gamma LUT is used (not bypassed).

When this bit = 1b, the Gamma LUT is not used (bypassed).

Note

The PIP2 window must not be Gamma LUT enabled if the window is not selected for gamma display in REG[083Eh] bits 11-10 and bits 5-4.

bit 12 PIP1 Window Gamma LUT Bypass Enable

This bit controls whether the Gamma LUT, as selected by the Gamma LUT Display Bank Select bits (REG[083Eh] bits 5-4), is used to determine the PIP1 window image. When the Gamma LUT is bypassed, gamma correction does not take place.

When this bit = 0b, the Gamma LUT is used (not bypassed).

When this bit = 1b, the Gamma LUT is not used (bypassed).

Note

The PIP1 window must not be Gamma LUT enabled if the window is not selected for gamma display in REG[083Eh] bits 11-10 and bits 5-4.

bits 11-10 Gamma LUT PIP Window Select bits [1:0]

These bits only have an effect when REG[083Eh] bits 5-4 = 10b.

When the Gamma LUT Display Bank Select bits are configured for Bank B to be used by the PIP window, these bits allow selection of which PIP window(s) will be gamma corrected.

Table 10-29: Gamma LUT PIP Window Selection

REG[083Eh] bits 11-10	Gamma LUT PIP Window
00b	PIP1 window + PIP2 window
01b	PIP1 window
10b	PIP2 window
11b	Reserved

bits 9-8 Gamma LUT Write Color Select bits [1:0]

These bits select which RGB component of the Gamma LUT is written to when data is written to the Gamma LUT Access Data Port, REG[0842h]. The address (or index) of the Gamma LUT written to is selected by the Gamma LUT Access Address Port, REG[0840h].

When option 11b is selected, the same data value is written to each component (R, G, and B) of the Gamma LUT.

Table 10-30: Gamma LUT Write Color Selection

REG[083Eh] bits 9-8	Gamma LUT Write Color
00b	Red Color LUT Write Enable
01b	Green Color LUT Write Enable
10b	Blue Color LUT Write Enable
11b	All Color LUT Write Enable

bits 5-4 Gamma LUT Display Bank Select bits [1:0]

These bits determine how the Gamma LUT banks (A and B) are used for display and accessed by the Host. A Gamma LUT bank cannot be used for gamma correction of the display window and simultaneously programmed by the Host.

Table 10-31: Gamma LUT Display Bank Selection

REG[083Eh] bits 5-4	Gamma LUT Display Bank
00b	Bank A is used for gamma correction of the View Port (Main + PIP1 Window). Bank B is enabled for accesses from the Host interface.
01b	Bank B is used for gamma correction of the View Port (Main + PIP1 Window). Bank A is enabled for accesses from the Host interface.
10b	Bank A is used for gamma correction of the Main window Bank B is used for gamma correction of the selected PIP Windows (see REG[083Eh] bits 11-10). In this mode, neither Gamma LUT bank can be accessed by the Host interface.
11b	Both Bank A and Bank B are enabled for accesses from Host interface. When writing to the Gamma LUT using the Gamma LUT Access Data Port (REG[0842h]), the same value will be written to both banks of the Gamma LUT. The Gamma LUT should not be read in this mode. In this mode, neither Gamma LUT bank can be used for gamma correction.

bit 3 Input Data Extra Bit Expansion Enable

When this bit = 0b, the extra data bits input to gamma correction are clipped to 0.
When this bit = 1b, the extra data bits input to gamma correction are filled with the MSB bit in each color. For example, if the display buffer format is RGB 5:6:5 and the panel data bus width is 18-bit (R'G'B' 666), the MSB bit, R[5] or B[5], is put in the extra bit of displayed data bit, R'[6] or B'[6], respectively.

bit 2 Input Data Extra Bit Clip Disable

When this bit = 0b, extra bits in displayed data bits at the point after color conversion and before gamma correction, not read from the display buffer, are clipped. For example, if the display buffer format is RGB 5:6:5 and the panel data bus width is 18-bit (RGB 6:6:6), the extra bits of displayed bits, R'[0],B'[0] are clipped before gamma correction.
When this bit = 1b, all data bits input to the gamma correction module are not clipped and are left as is.

bit 1 Gamma LUT Address Auto Increment

This bit determines whether the Gamma LUT Access Address Port (REG[0840h]) must be set before each write to the Gamma LUT Access Data Port (REG[0842h]).
When this bit = 0b, the address of the Gamma LUT must be set before each data write.
When this bit = 1b, only the first address of the Gamma LUT must be set. For each subsequent data write, the Gamma LUT address is incremented automatically.

bit 0 Gamma LUT Enable

This bit controls the Gamma LUT function.
When this bit = 0b, the Gamma LUTs are disabled and gamma correction is not done. The Gamma LUTs are also not accessible from the Host in this mode.
When this bit = 1b, the Gamma LUTs are enabled and operate as configured by the bits in REG[083Eh].

REG[0840h] Gamma LUT Access Address Port Register

Default = 0000h — Write Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Gamma LUT Access Address bits 7-0							

bits 7-0 Gamma LUT Access Address bits [7:0] (Write Only)

These bits specify the address (or index) of the Gamma LUT that will be accessed using the Gamma LUT Access Data Port, REG[0842h]. If more than one Gamma LUT entry will be programmed, the Gamma LUT Address Auto Increment bit can be set (REG[083Eh] bit 1 = 1b) so that the Gamma LUT Access Address must be programmed with the first address only. When auto increment is enabled, after writing the specified value (see REG[083Eh] bits 9-8) to the Gamma LUT, the access address is automatically incremented and the next entry can be programmed immediately.

Note

When reading from the Gamma LUT, these bits must be programmed before each read of the Gamma LUT Access Data Port, REG[0842h].

REG[0842h] Gamma LUT Access Data Port Register

Default = XXXXh — Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Gamma LUT Access Data bits 7-0							

bits 7-0 Gamma LUT Access Data bits [7:0]

These bits specify the RGB data value to be written to the Gamma LUT at the address (or index) specified by the Gamma LUT Access Address Port, REG[0840h].

Note

The LUT (look-up table) is in SRAM and has an unknown default value. Before using the Gamma LUT, it must be initialized.

REG[0844h] Pseudo Color Mode Register

Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a					Pseudo Color Mode bits 2-0		
7	6	5	4	3	2	1	0

bits 2-0 Pseudo Color Mode bits [2:0]

These bits select the pseudo color mode that will be used.

Table 10-32: Pseudo Color Mode Selection

REG[0844h] bits 2-0	Pseudo Color Mode
000b	Disable (each color component is rounded down to Panel Data Bus Width)
001b	2x2 matrix dither enable
010b	FRM enable
011b	Reserved
100b	Error diffusion
101b ~ 111b	Reserved

REG[0846h] Display FIFO1 Threshold Register
Default = 01FFh — Read/Write

15	14	13	12	11	10	9	8
Reserved	n/a						Display FIFO1 High Threshold bit 8
Display FIFO1 High Threshold bits 7-0							
7	6	5	4	3	2	1	0

Note
Use this register value as the default for normal usage.

bit 15 Reserved
The default value for this bit is 0b.

bits 8-0 Display FIFO1 High Threshold bits [8:0]
When the difference between the read and write pointer of Display FIFO1 is less than this value, a memory read request is generated.

REG[0848h] Display FIFO2 Threshold Register
Default = 01FFh — Read/Write

15	14	13	12	11	10	9	8
Reserved	n/a						Display FIFO2 High Threshold bit 8
Display FIFO2 High Threshold bits 7-0							
7	6	5	4	3	2	1	0

Note
Use this register value as the default for normal usage.

bit 15 Reserved
The default value for this bit is 0b.

bits 8-0 Display FIFO2 High Threshold bits [8:0]
When the difference between the read and write pointer of Display FIFO2 is less than this value, a memory read request is generated.

REG[084Ah] PIP1 Window X Start Position Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					PIP1 Window X Start Position bits 10-8		
PIP1 Window X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP1 Window X Start Position bits [10:0]
These bits determine the X start position of the PIP1 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.
REG[084Ah] bits 10-0 = PIP1 window X start position ÷ 2

Note
1.This register must only be changed during Vertical Non-Display Period,
REG[0818h] bit 0 = 1b.
2.PIP coordinates must be set within the panel display area.

REG[084Ch] PIP1 Window X End Position Register
Default = 0000h Read/Write

n/a					PIP1 Window X End Position bits 10-8		
15	14	13	12	11	10	9	8
PIP1 Window X End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP1 Window X End Position bits [10:0]
These bits determine the X end position of the PIP1 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.
REG[084Ch] bits 10-0 = (PIP1 window X end position - 1) ÷ 2

Note
1.This register must only be changed during Vertical Non-Display Period,
REG[0818h] bit 0 = 1b.
2.PIP coordinates must be set within the panel display area.

REG[084Eh] PIP1 Window Y Start Position Register
Default = 0000h Read/Write

n/a					PIP1 Window Y Start Position bits 10-8		
15	14	13	12	11	10	9	8
PIP1 Window Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP1 Window Y Start Position bits [10:0]
These bits determine the Y start position of the PIP1 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.
REG[084Eh] bits 10-0 = PIP1 window Y start position ÷ 2

Note
1.This register must only be changed during Vertical Non-Display Period, REG[0818h] bit 0 = 1b.
2.The PIP1 window Y start position must be set to 0h before disabling the PIP1 window.

REG[0850h] PIP1 Window Y End Position Register
Default = 0000h Read/Write

n/a					PIP1 Window Y End Position bits 10-8		
15	14	13	12	11	10	9	8
PIP1 Window Y End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP1 Window Y End Position bits [10:0]
These bits determine the Y end position of the PIP1 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.
REG[0850h] bits 10-0 = (PIP1 window Y end position - 1) ÷ 2

Note
This register must only be changed during Vertical Non-Display Period, REG[0818h] bit 0 = 1b.

REG[0852h] PIP2 Window X Start Position Register
Default = 0000h Read/Write

n/a					PIP2 Window X Start Position bits 10-8		
15	14	13	12	11	10	9	8
PIP2 Window X Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP2 Window X Start Position bits [10:0]
These bits determine the X start position of the PIP2 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.
REG[0852h] bits 10-0 = PIP2 window X start position ÷ 2

REG[0854h] PIP2 Window X End Position Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					PIP2 Window X End Position bits 10-8		
PIP2 Window X End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP2 Window X End Position bits [10:0]

These bits determine the X end position of the PIP2 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.

REG[0854h] bits 10-0 = (PIP2 window X end position - 1) ÷ 2

REG[0856h] PIP2 Window Y Start Position Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					PIP2 Window Y Start Position bits 10-8		
PIP2 Window Y Start Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP2 Window Y Start Position bits [10:0]

These bits determine the Y start position of the PIP2 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.

REG[0852h] bits 10-0 = PIP2 window Y start position ÷ 2

REG[0858h] PIP2 Window Y End Position Register

Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a					PIP2 Window Y End Position bits 10-8		
PIP2 Window Y End Position bits 7-0							
7	6	5	4	3	2	1	0

bits 10-0 PIP2 Window Y End Position bits [10:0]

These bits determine the Y end position of the PIP2 window in relation to the origin of the panel, in 2 pixel resolution. The origin is assumed to be 0,0.

REG[0858h] bits 10-0 = (PIP2 window Y end position - 1) ÷ 2

REG[085Ah] Main Window Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Main Window Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Main Window Buffer Start Address bits 7-0							

REG[085Ch] Main Window Buffer Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Main Window Buffer Start Address bits 25-24	
7	6	5	4	3	2	1	0
Main Window Buffer Start Address bits 23-16							

REG[085Ch] bits 9-0

REG[085Ah] bits 15-0 Main Window Buffer Start Address bits [25:0]
These bits specify the memory start address of the Main Window buffer, in bytes.

Note
For 32 bpp (REG[0832h] bits 2-0 = 011b), bits 1-0 must be set to 00b.
For 16 bpp (REG[0832h] bits 2-0 = 001b), bit 0 must be set to 0b.

REG[085Eh] PIP1 Window Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
PIP1 Window Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
PIP1 Window Buffer Start Address bits 7-0							

REG[0860h] PIP1 Window Buffer Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						PIP1 Window Buffer Start Address bits 25-24	
7	6	5	4	3	2	1	0
PIP1 Window Buffer Start Address bits 23-16							

REG[0860h] bits 9-0

REG[085Eh] bits 15-0 PIP1 Window Buffer Start Address bits [25:0]
These bits specify the memory start address of the PIP1 Window buffer, in bytes.

Note
For 32 bpp (REG[0832h] bits 6-4 = 011b), bits 1-0 must be set to 00b.
For 16 bpp (REG[0832h] bits 6-4 = 001b), bit 0 must be set to 0b.

REG[0862h] PIP2 Window Buffer Start Address Register 0

Default = 0000h Read/Write

PIP2 Window Buffer Start Address bits 15-8							
15	14	13	12	11	10	9	8
PIP2 Window Buffer Start Address bits 7-0							
7	6	5	4	3	2	1	0

REG[0864h] PIP2 Window Buffer Start Address Register 1

Default = 0000h Read/Write

n/a						PIP2 Window Buffer Start Address bits 25-24	
15	14	13	12	11	10	9	8
PIP2 Window Buffer Start Address bits 23-16							
7	6	5	4	3	2	1	0

REG[0864h] bits 9-0

REG[0862h] bits 15-0 PIP2 Window Buffer Start Address bits [25:0]
These bits specify the memory start address of the PIP2 Window buffer, in bytes.

Note
For 32 bpp (see REG[0832h] bits 10-8), bits 1-0 must be set to 00b.
For 16 bpp (see REG[0832h] bits 10-8), bit 0 must be set to 0b.

REG[0866h] and REG[0868h] are Reserved

These registers are Reserved and should not be written.

REG[086Ah] Main Window Buffer Line Address Offset Register
Default = 0000h Read/Write

n/a		Main Window Buffer Line Address Offset bits 13-8					
15	14	13	12	11	10	9	8
Main Window Buffer Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 13-0 Main Window Buffer Line Address Offset bits [13:0]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the Main Window buffer, in bytes.

REG[086Ch] PIP1 Window Buffer Line Address Offset Register
Default = 0000h Read/Write

n/a		PIP1 Window Buffer Line Address Offset bits 13-8					
15	14	13	12	11	10	9	8
PIP1 Window Buffer Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 13-0 PIP1 Window Buffer Line Address Offset bits [13:0]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the PIP1 Window buffer, in bytes.

Note
This register must only be changed during Vertical Non-Display Period, REG[0818h] bit 0 = 1b.

REG[086Eh] PIP2 Window Buffer Line Address Offset Register
Default = 0000h Read/Write

n/a		PIP2 Window Buffer Line Address Offset bits 13-8					
15	14	13	12	11	10	9	8
PIP2 Window Buffer Line Address Offset bits 7-0							
7	6	5	4	3	2	1	0

bits 13-0 PIP2 Window Buffer Line Address Offset bits [13:0]
These bits specify the offset from the beginning of one display line to the beginning of the next display line in the memory used for the PIP2 Window buffer, in bytes.

REG[0870h] is Reserved

This register is Reserved and should not be written.

REG[0880h] Color Conversion Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
UV Offset Enable	n/a		Color Conversion Window Select bits 1-0		n/a		Color Conversion Enable

bit 7 UV Offset Enable
When this bit = 0b, UV offset is disabled.
When this bit = 1b, UV offset is enabled.

bits 4-3 Color Conversion Window Select bits [1:0]
When color conversion is enabled (REG[0880h] bit 0 = 1b), these bits select which window color conversion is applied to.

Table 10-33: Color Conversion Window Selection

REG[0880h] bits 4-3	Color Conversion is Applied to
00b	Main, PIP1, and PIP2 windows
01b	PIP1 window only
10b	PIP2 window only
11b	PIP1 and PIP2 windows only

bit 0 Color Conversion Enable
This bit controls the color conversion function.
When this bit = 0b, color conversion is disabled (or bypassed).
When this bit = 1b, color conversion is enabled.

REG[0882h] ~ REG[0892h] Color Conversion Matrix Coefficient Registers 0-8
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a					Color Conversion Matrix Coefficient X bits 10-8		

7	6	5	4	3	2	1	0
Color Conversion Matrix Coefficient X bits 7-0							

bits 10-0 Color Conversion Matrix Coefficient X bits [10:0]
These bits form the matrix coefficients used for color conversion. Bit 10 is the sign bit. Bits 9-8 are the integer, and bits 7-0 are the fractional part.

10.4.5 GPIO Registers

Note
All GPIO function pins are multiplexed with other function pins. After reset, the GPIO pins must be configured according to the alternate functions required by the implementation. For detailed pin descriptions, refer to Section Chapter 5, “Pins” on page 14. For a summary of GPIO pin usage, see Section 5.6, “GPIO Pin Mapping” on page 34.

REG[0C00h] GPIOA Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIOA Data bits 7-4				Reserved			
7	6	5	4	3	2	1	0

bits 7-4 GPIOA Data bits [7:4]
These bits are used differently based on the configuration of the corresponding GPIOA [7:4] pin. To determine the configuration of the GPIOAx pin, refer to the GPIOA Pin Function register, REG[0C02h].
For Reads:
When the GPIOAx pin is configured as an input, the corresponding GPIOA Data bit indicates the input state of the pin. For example, if GPIOA7 is high, GPIOA Data bit 7 will return a 1b.
When the GPIOAx pin is configured as an output, the corresponding GPIOA Data bit indicates the value of the register bit.
For Writes:
When the GPIOAx pin is configured as an output, the corresponding GPIOA Data bit controls the output level of the pin. For example, if GPIOA Data bit 7 is set to 1b, GPIOA7 will output high.

bits 3-0 Reserved
The default value for these bits is 0000b.

REG[0C02h] GPIOA Pin Function Register
Default = 0000h Read/Write

GPIOA7 Mode bits 1-0		GPIOA6 Mode bits 1-0		GPIOA5 Mode bits 1-0		GPIOA4 Mode bits 1-0	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

bits 15-8 GPIOAx Mode bits [1:0]
Each GPIOA[7:4] pin can be configured as an input, output, or one of two non-GPIO functions. These bits specify the pin function (or mode) for the corresponding GPIOAx pin. For details on the non-GPIO functions assigned to each GPIOAx pin, see Section 5.2.4, “GPIO / Multi Function Interface” on page 23.

Table 10-34: GPIOAx Pin Function

GPIOAx Mode bits 1-0	GPIOAx Pin Function
00b (default)	GPIOAx is configured as an input
01b	GPIOAx is configured for Non-GPIO Function #1
10b	GPIOAx is configured as an output
11b	Reserved

Note
For GPIOA4, the Non-GPIO Function #1 is Reserved and should not be selected

bits 7-0 Reserved
The default value for these bits is 00000000b.

REG[0C04h] GPIOB Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIOB Data bits 7-4				Reserved			
7	6	5	4	3	2	1	0

bits 7-4 GPIOB Data bits [7:4]
These bits are used differently based on the configuration of the corresponding GPIOB [7:4] pin. To determine the configuration of the GPIOBx pin, refer to the GPIOB Pin Function register, REG[0C06h].
For Reads:
When the GPIOBx pin is configured as an input, the corresponding GPIOB Data bit indicates the input state of the pin. For example, if GPIOB7 is high, GPIOB Data bit 7 will return a 1b.
When the GPIOBx pin is configured as an output, the corresponding GPIOB Data bit indicates the value of the register bit.
For Writes:
When the GPIOBx pin is configured as an output, the corresponding GPIOB Data bit controls the output level of the pin. For example, if GPIOB Data bit 7 is set to 1b, GPIOB7 will output high.

bits 3-0 Reserved
The default value for these bits is 0000b.

REG[0C06h] GPIOB Pin Function Register
Default = 0000h Read/Write

GPIOB7 Mode bits1-0		GPIOB6 Mode bits 1-0		GPIOB5 Mode bits 1-0		GPIOB4 Mode bits 1-0	
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0

bits 15-8 GPIOBx Mode bits [1:0]
Each GPIOB[7:4] pin can be configured as an input, output, or one of two non-GPIO functions. These bits specify the pin function (or mode) for the corresponding GPIOBx pin. For details on the non-GPIO functions assigned to each GPIOBx pin, see Section 5.2.4, “GPIO / Multi Function Interface” on page 23

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Table 10-35: GPIOBx Pin Function

GPIOBx Mode bits 1-0	GPIOBx Pin Function
00b (default)	GPIOBx is configured as an input
01b	GPIOBx is configured for Non-GPIO Function #1
10b	GPIOBx is configured as an output
11b	Reserved

Note
For GPIOB[6:4], the Non-GPIO Function #1 is Reserved and should not be selected.

bits 7-0 Reserved
The default value for these bits is 00000000b.

REG[0C08h] GPIOC Data Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
GPIOC Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 GPIOC Data bits [7:0]
These bits are used differently based on the configuration of the corresponding GPIOC[7:0] pin. To determine the configuration of the GPIOCx pin, refer to the GPIOC Pin Function register, REG[0C0Ah].
For Reads:
When the GPIOCx pin is configured as an input, the corresponding GPIOC Data bit indicates the input state of the pin. For example, if GPIOC7 is high, GPIOC Data bit 7 will return a 1b.
When the GPIOCx pin is configured as an output, the corresponding GPIOC Data bit indicates the value of the register bit.
For Writes:
When the GPIOCx pin is configured as an output, the corresponding GPIOC Data bit controls the output level of the pin. For example, if GPIOC Data bit 7 is set to 1b, GPIOC7 will output high.

REG[0C0Ah] GPIOC Pin Function Register
Default = 0000h Read/Write

GPIOC7 Mode bits1-0		GPIOC6 Mode bits 1-0		GPIOC5 Mode bits 1-0		GPIOC4 Mode bits 1-0	
15	14	13	12	11	10	9	8
GPIOC3 Mode bits 1-0		GPIOC2 Mode bits 1-0		GPIOC1 Mode bits 1-0		GPIOC0 Mode bits 1-0	
7	6	5	4	3	2	1	0

bits 15-0 GPIOCx Mode bits [1:0]
Each GPIOC[7:0] pin can be configured as an input, output, or one of two non-GPIO functions. These bits specify the pin function (or mode) for the corresponding GPIOCx pin. For details on the non-GPIO functions assigned to each GPIOCx pin, see Section 5.2.4, “GPIO / Multi Function Interface” on page 23.

Table 10-36: GPIOCx Pin Function

GPIOCx Mode bits 1-0	GPIOCx Pin Function
00b (default)	GPIOCx is configured as an input
01b	Reserved
10b	GPIOCx is configured as an output
11b	Reserved

REG[0C0Ch] GPIOD Data Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				GPIOD Data bits 3-0			

bits 3-0 GPIOD Data bits [3:0]

These bits are used differently based on the configuration of the corresponding GPIOD[3:0] pin. To determine the configuration of the GPIODx pin, refer to the GPIOD Pin Function register, REG[0C0Eh].

For Reads:

When the GPIODx pin is configured as an input, the corresponding GPIOD Data bit indicates the input state of the pin. For example, if GPIOD3 is high, GPIOD Data bit 3 will return a 1b.

When the GPIODx pin is configured as an output, the corresponding GPIOD Data bit indicates the value of the register bit.

For Writes:

When the GPIODx pin is configured as an output, the corresponding GPIOD Data bit controls the output level of the pin. For example, if GPIOD Data bit 3 is set to 1b, GPIOD3 will output high.

REG[0C0Eh] GPIOD Pin Function Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
GPIOD3 Mode bits 1-0		GPIOD2 Mode bits 1-0		GPIOD1 Mode bits 1-0		GPIOD0 Mode bits 1-0	

bits 7-0 GPIODx Mode bits [1:0]

Each GPIOD[3:0] pin can be configured as an input, output, or one of two non-GPIO functions. These bits specify the pin function (or mode) for the corresponding GPIODx pin. For details on the non-GPIO functions assigned to each GPIODx pin, see Section 5.2.4, “GPIO / Multi Function Interface” on page 23.

Table 10-37: GPIODx Pin Function

GPIODx Mode bits 1-0	GPIODx Pin Function
00b (default)	GPIODx is configured as an input
01b	GPIODx is configured for Non-GPIO Function #1
10b	GPIODx is configured as an output
11b	Reserved

Note
For GPIOD[2:0], the Non-GPIO Function #1 is Reserved and should not be selected

REG[0C10h] through REG[0C16h] are Reserved

These registers are Reserved and should not be written.

REG[0C18h] GPIOG Data Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a			GPIOG Data bits 4-0				

bits 4-0 GPIOG Data bits [4:0]

These bits are used differently based on the configuration of the corresponding GPIOG[4:0] pin. To determine the configuration of the GPIOGx pin, refer to the GPIOG Pin Function register, REG[0C1Ah].

For Reads:

When the GPIOGx pin is configured as an input, the corresponding GPIOG Data bit indicates the input state of the pin. For example, if GPIOG4 is high, GPIOG Data bit 4 will return a 1b.

When the GPIOGx pin is configured as an output, the corresponding GPIOG Data bit indicates the value of the register bit.

For Writes:

When the GPIOGx pin is configured as an output, the corresponding GPIOG Data bit controls the output level of the pin. For example, if GPIOG Data bit 4 is set to 1b, GPIOG4 will output high.

REG[0C1Ah] GPIOG Pin Function Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIOG4 Mode bits 1-0	

7	6	5	4	3	2	1	0
GPIOG3 Mode bits 1-0		GPIOG2 Mode bits 1-0		GPIOG1 Mode bits 1-0		GPIOG0 Mode bits 1-0	

bits 9-0 GPIOGx Mode bits [1:0]

Each GPIOG[4:0] pin can be configured as an input, output, or one of two non-GPIO functions. These bits specify the pin function (or mode) for the corresponding GPIOGx pin. For details on the non-GPIO functions assigned to each GPIOGx pin, see Section 5.2.4, “GPIO / Multi Function Interface” on page 23.

Table 10-38: GPIOGx Pin Function

GPIOGx Mode bits 1-0	GPIOGx Pin Function
00b (default)	GPIOGx is configured as an input
01b	Reserved
10b	GPIOGx is configured as an output
11b	GPIOGx is configured for Non-GPIO Function #2

REG[0C1Ch] through REG[0C22h] are Reserved

These registers are Reserved and should not be written.

REG[0C24h] GPIOA&B Interrupt Type Register
Default = 0000h — Read/Write

GPIOB Interrupt Type Select bits 7-4				Reserved			
15	14	13	12	11	10	9	8
GPIOA Interrupt Type Select bits 7-4				Reserved			
7	6	5	4	3	2	1	0

bits 15-12 GPIOB Interrupt Type Select bits [7:4]
These bits individually control the trigger type of the interrupts associated with the GPIOB[7:4] pins. The interrupt function is controlled using REG[0C28h].
When this bit = 0b, the interrupt uses a level trigger.
When this bit = 1b, the interrupt uses an edge trigger.

For example when bit 15 = 1b, the interrupt associated with the GPIOB7 pin uses an edge trigger.

Note
Before changing any of these bits, all outstanding interrupts must be cleared using REG[0C2Ah].

bits 11-8 Reserved
The default value for these bits is 0000b.

bits 7-4 GPIOA Interrupt Type Select bits [7:4]
These bits individually control the trigger type of the interrupts associated with the GPIOA[7:4] pins. The interrupt function is controlled using REG[0C28h].
When this bit = 0b, the interrupt uses a level trigger.
When this bit = 1b, the interrupt uses a edge trigger.

For example when bit 7= 0b, the interrupt associated with the GPIOA7 pin uses a level trigger.

Note
Before changing any of these bits, all outstanding interrupts must be cleared using REG[0C2Ah].

bits 3-0 Reserved
The default value for these bits is 0000b.

REG[0C26h] GPIOA&B Interrupt Polarity Register
Default = 0000h Read/Write

GPIOB Interrupt Polarity Select bits 7-4				Reserved			
15	14	13	12	11	10	9	8
GPIOA Interrupt Polarity Select bits 7-4				Reserved			
7	6	5	4	3	2	1	0

bits 15-12 GPIOB Interrupt Polarity Select bits [7:4]
These bits individually control the polarity of the interrupts associated with the GPIOB[7:4] pins. The interrupt function is controlled using REG[0C28h].
When this bit = 0b, the interrupt is triggered when high (for level trigger) or when rising (for edge trigger).
When this bit = 1b, the interrupt is triggered when low (for level trigger) or when falling (for edge trigger).

Note
Before changing any of these bits, all outstanding interrupts must be cleared using REG[0C2Ah].

bits 11-8 Reserved
The default value for these bits is 0000b.

bits 7-4 GPIOA Interrupt Polarity Select bits [7:4]
These bits individually control the polarity of the interrupts associated with the GPIOA[7:4] pins. The interrupt function is controlled using REG[0C28h].
When this bit = 0b, the interrupt is triggered when high (for level trigger) or when rising (for edge trigger).
When this bit = 1b, the interrupt is triggered when low (for level trigger) or when falling (for edge trigger).

Note
Before changing any of these bits, all outstanding interrupts must be cleared using REG[0C2Ah].

bits 3-0 Reserved
The default value for these bits is 0000b.

REG[0C28h] GPIOA&B Interrupt Enable Register

Default = 0000h Read/Write

GPIOB Interrupt Enable bits 7-4				Reserved			
15	14	13	12	11	10	9	8
GPIOA Interrupt Enable bits 7-4				Reserved			
7	6	5	4	3	2	1	0

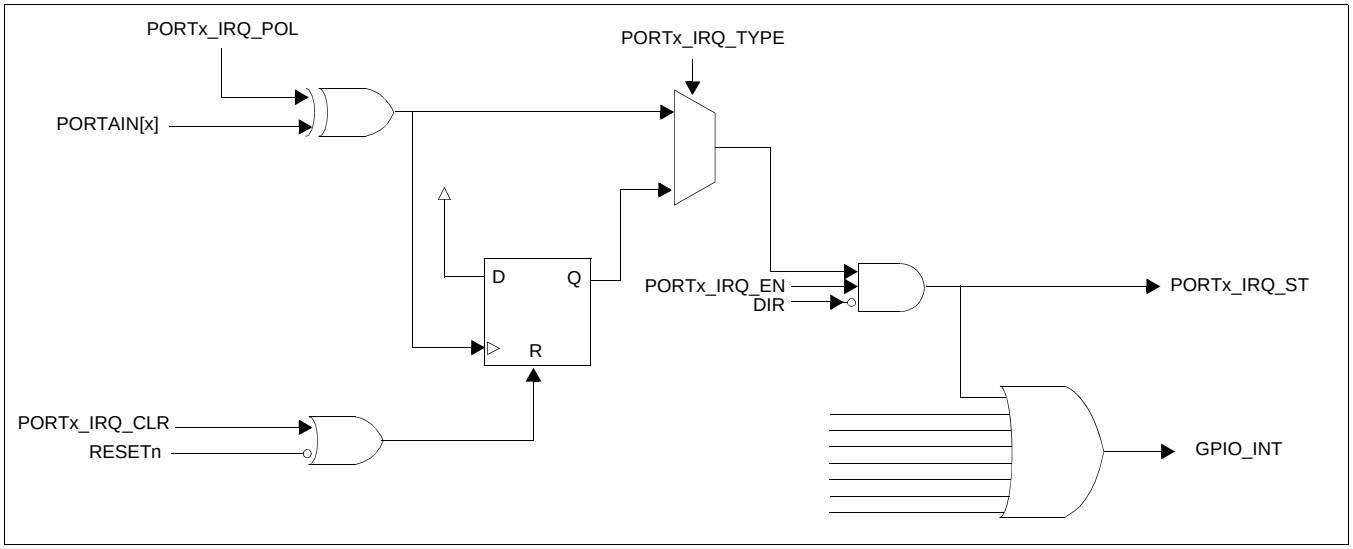

Figure 10-1: GPIOA and GPIOB Interrupt Logic

bits 15-12 GPIOB Interrupt Enable bits [7:4]

The GPIOB[7:4] pins can generate interrupts based on the setting of these bits. Each bit controls whether the corresponding GPIOB[7:4] pin has interrupts enabled. For example, setting bit 7 to 1b enables the interrupt for the GPIOB7 pin. The status of each interrupt is indicated by the bits in REG[0C2Ah]. Before enabling any interrupts, the Interrupt Type (REG[0C24h]) and Interrupt Polarity (REG[0C26h]) should be configured.

When this bit = 0b, the interrupt associated with GPIOBx is disabled.

When this bit = 1b, the interrupt associated with GPIOBx is enabled.

bits 11-8 Reserved

The default value for these bits is 0000b.

bits 7-4 GPIOA Interrupt Enable bits [7:4]

The GPIOA[7:4] pins can generate interrupts based on the setting of these bits. Each bit controls whether the corresponding GPIOA[7:4] pin has interrupts enabled. For example, setting bit 7 to 1b enables the interrupt for the GPIOA7 pin. The status of each interrupt is indicated by the bits in REG[0C2Ah]. Before enabling any interrupts, the Interrupt Type (REG[0C24h]) and Interrupt Polarity (REG[0C26h]) should be configured.

When this bit = 0b, the interrupt associated with GPIOAx is disabled.

When this bit = 1b, the interrupt associated with GPIOAx is enabled.

bits 3-0 Reserved

The default value for these bits is 0000b.

REG[0C2Ah] GPIOA&B IRQ Status and Clear Register

Default = 0000h — Read/Write

GPIOB Interrupt Status bits 7-4				Reserved			
15	14	13	12	11	10	9	8
GPIOA Interrupt Status bits 7-4				Reserved			
7	6	5	4	3	2	1	0

bits 15-12 GPIOB Interrupt Status bits [7:4]
When an interrupt is enabled using REG[0C28h], these bits indicate the status of the corresponding GPIOB[7:4] interrupt. For example, reading bit 7 indicates the status of the GPIOB7 interrupt.
When this bit = 0b, an interrupt has not occurred.
When this bit = 1b, an interrupt has occurred.

To clear the interrupt status bit, write a 1b then a 0b to the corresponding bit.

bits 11-8 Reserved
The default value for these bits is 0000b.

bits 7-4 GPIOA Interrupt Status bits [7:4]
When an interrupt is enabled using REG[0C28h], these bits indicate the status of the corresponding GPIOA[7:4] interrupt. For example, reading bit 7 indicates the status of the GPIOA7 interrupt.
When this bit = 0b, an interrupt has not occurred.
When this bit = 1b, an interrupt has occurred.

To clear the interrupt status bit, write a 1b then a 0b to the corresponding bit.

bits 3-0 Reserved
The default value for these bits is 0000b.

10.4.6 Memory Controller Registers

REG[1C00h] Memory Control Register
Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
SDRAM Write Protect Enable	n/a	Reserved	Reserved	Reserved	Reserved		
7	6	5	4	3	2	1	0

Note
This register must be set to 11h before the SDRAM memory is enabled using REG[1C02h] bit 0.

bit 7 SDRAM Write Protect Enable
This bit determines whether the external SDRAM memory is write protected.
When this bit = 0b, write protection is disabled. (default)
When this bit = 1b, write protection is enabled.

bit 5 Reserved
This bit must be set to 0b.

bit 4 Reserved
This bit must be set to 1b.

bit 3 Reserved
This bit must be set to 0b.

bits 2-0 Reserved
These bits must be set to 001b.

REG[1C02h] Memory Configuration Register 0
Default = 0002h — Read/Write

n/a							
15	14	13	12	11	10	9	8
Memory Initialized (RO)	n/a				Reserved		Memory Enable
7	6	5	4	3	2	1	0

bit 7 Memory Initialized (Read Only)
This bit indicates the initialization status of the external SDRAM memory. This bit must be checked after the first time the SDRAM memory is enabled using the Memory Enable bit (REG[1C02h] bit 0) to determine if the SDRAM initialization process has completed.
When this bit = 0b, the SDRAM has not be initialized.
When this bit = 1b, the SDRAM has been initialized and can be accessed when REG[1C02h] bit 0 = 1b.

Note
To access the SDRAM, both the Memory Initialized bit and the Memory Enable bit (REG[1C02h] bit 0) must equal 1b.

bits 2-1 Reserved
These bits must be set to 01b.

bit 0 Memory Enable
This bit enables the external SDRAM memory. If the memory has not been initialized, an initialization sequence is sent to the SDRAM when this bit is set to 1b. When this bit is set, the Memory Initialized bit (REG[1C02h] bit 7) must be checked to confirm that initialization is complete **before** accessing the SDRAM memory.
When this bit = 0b, the SDRAM memory is disabled.
When this bit = 1b, the SDRAM memory is enabled and the initialization process is started. The SDRAM can be accessed once REG[1C02h] bit 7 = 1b.

Note
1.To access the SDRAM, both the Memory Initialized bit (REG[1C02h] bit 7) and the Memory Enable bit must equal 1b.
2.To lower power consumption, the SDRAM should be put into self-refresh mode before disabling the SDRAM interface.
3.REG[1C00h] must be set to 11h before enabling the SDRAM memory.

REG[1C04h] Memory Configuration Register 1
Default = 7AAFh Read/Write

Active to Precharge Cycle bits 3-0				Auto Refresh to Active Cycle bits 3-0			
15	14	13	12	11	10	9	8
Write to Precharge bits 1-0		Return to Precharge bits 1-0		RAS to CAS Delay bits 1-0		CAS Latency bits 1-0	
7	6	5	4	3	2	1	0

bits 15-12 Active to Precharge Cycle bits [3:0]
These bits are used to configure the Active to Precharge cycle for the external SDRAM, in MEMCLK periods.
Active to Precharge Cycle = REG[1C04h] bits 15-12 + 1

Note
If the Active to Precharge Cycle is configured to a value less than the number of cycles required for a specific operation, this setting is ignored.

bits 11-8 Auto Refresh to Active Cycle bits [3:0]
These bits control the minimum amount of time, in SDRAM clock cycles, an active command can be issued after an auto refresh command.

Table 10-39: Auto Refresh to Active Cycle Time

REG[1C04h] bits 11-8	Refresh to Active Time	REG[1C04h] bits 11-8	Refresh to Active Time
0000b	Reserved	1000b	9 SDRAM clocks
0001b	Reserved	1001b	10 SDRAM clocks
0010b	3 SDRAM clocks	1010b (default)	11 SDRAM clocks
0011b	4 SDRAM clocks	1011b	12 SDRAM clocks

Table 10-39: Auto Refresh to Active Cycle Time

REG[1C04h] bits 11-8	Refresh to Active Time	REG[1C04h] bits 11-8	Refresh to Active Time
0100b	5 SDRAM clocks	1100b	13 SDRAM clocks
0101b	6 SDRAM clocks	1101b	14 SDRAM clocks
0110b	7 SDRAM clocks	1110b	15 SDRAM clocks
0111b	8 SDRAM clocks	1111b	16 SDRAM clocks

bits 7-6 Write to Precharge bits [1:0] (TWR)

These bits are used to configure the Write to Precharge value for the external SDRAM, in cycles.

Table 10-40: Write to Precharge Selection

REG[1C04h] bits 7-6	Write to Precharge
00b	Reserved
01b	2 Clocks
10b (default)	3 Clocks
11b	4 Clocks

Note

1.The Write to Precharge value only has an effect if:
RAS to CAS delay + Write to Precharge time + time from first write latched to last write latched > Active to Precharge time (see REG[1C04h] bits 15-12)
2.If the Write to Precharge is set to 2 clocks, the RAS to CAS delay must be set to 3 clocks (REG[1C04h] bits 3-2 = 11b).

bits 5-4 Return to Precharge bits [1:0] (TRP)

These bits are used to configure the Return to Precharge value for the external SDRAM, in cycles.

Table 10-41: Return to Precharge Selection

REG[1C04h] bits 5-4	Return to Precharge
00b	Reserved
01b	2 Clocks
10b (default)	3 Clocks
11b	4 Clocks

bits 3-2 RAS to CAS Delay bits [1:0] (TRCD)

These bits are used to configure the delay time between RAS# and CAS# for the external SDRAM, in cycles.

Table 10-42: RAS to CAS Delay Selection

REG[1C04h] bits 3-2	RAS to CAS Delay
00b	Reserved
01b	Reserved
10b	2 Clocks
11b (default)	3 Clocks

bits 1-0 CAS Latency bits [1:0]
These bits are used to configure the CAS Latency for the external SDRAM, in cycles.

Table 10-43: CAS Latency Selection

REG[1C04h] bits 1-0	CAS Latency
00b	Reserved
01b	Reserved
10b	2 Clocks
11b (default)	3 Clocks

REG[1C06h] Memory Configuration Register 2
Default = C010h Read/Write

Reserved	Dynamic SDRAM CKE Control	n/a					
15	14	13	12	11	10	9	8
n/a		Reserved		Auto Precharge	Memory Size bits 1-0		Reserved
7	6	5	4	3	2	1	0

bit 15 Reserved
The default value for this bit is 1b.

bit 14 Dynamic SDRAM CKE Control
This bit controls when the clock enable (MEMCKE) to the external SDRAM memory is asserted.
When this bit = 0b, clock enable is always asserted regardless of the SDRAM bus state.
When this bit = 1b, clock enable to the external SDRAM is driven high or low depending on the state of the SDRAM bus. (default)

bits 5-4 Reserved
The default value for these bits is 01b.

bit 3 Auto Precharge
This bit controls whether the SDRAM memory banks are precharged.
When this bit = 0b, the SDRAM memory banks are not precharged. (default)
When this bit = 1b, the SDRAM memory banks are precharged.

bits 2-1 Memory Size bits [1:0]

These bits configure the size of the external SDRAM memory connected to the S1D13L04.

Table 10-44: Memory Size Selection

REG[1C06h] bits 2-1	Memory Size
00b (default)	128 Mbit
01b	Reserved
10b	Reserved
11b	64 Mbit

The following table summarizes the address widths for each memory interface configuration.

Table 10-45: Memory Interface Address Widths

	Memory Size (REG[1C06h] bits 2-1)	
16-bit Memory Interface	**64 Mbit**	**128 Mbit**
Column Address Width	8	9
Bank Address Width	2	2
Row Address Width	12	12

bit 0 Reserved

The default value for this bit is 0b.

REG[1C08h] Memory Advanced Configuration Register
Default = 0F1Ah — Read/Write

Self Refresh Re-entry Cycle Count bits 7-0							
15	14	13	12	11	10	9	8
n/a	Reserved				Reserved	Self Refresh Re-entry Control	Self Refresh Mode Enable (WO)
7	6	5	4	3	2	1	0

bits 15-8 Self Refresh Re-entry Cycle Count bits [7:0]

These bits specify the number of cycles that must take place without further accesses before the SDRAM will re-enter self refresh mode. This happens when the SDRAM has been awoken from self refresh mode for a read or write access **and** the Self Refresh Re-entry Control bit is set to 1b (REG[1C08h] bit 1 = 1b). The default value is 0Fh and the minimum value is 02h. The count clock uses 1/4 of MEMCLK.

Self Refresh Re-entry delay = (REG[1C08h] bits 15-8) x 4 SDRAM clocks

bits 6-3 Reserved

The default value for these bits is 0011b.

bit 2 Reserved

The default value for this bit is 0b.

bit 1 Self Refresh Re-entry Control

This bit controls whether the SDRAM will re-enter self refresh mode after it has been awoken for a read or write access. If this function is enabled, the SDRAM will re-enter self refresh mode if there are no further accesses for the number of cycles specified by the Self Refresh Re-entry Cycle Counter bits, REG[1C08h] bits 15-8.

When this bit = 0b, the SDRAM will not re-enter self refresh mode. (default)

When this bit = 1b, the SDRAM will re-enter self refresh mode if there are no further accesses for the specified number of cycles.

Note

If the SDRAM is brought out of self refresh mode by setting REG[1C08h] bit 0 to 0b, the SDRAM will still re-enter self refresh if this bit is set to 1b.

bit 0 Self Refresh Mode Enable (Write Only)

This bit controls self refresh mode for the SDRAM. When the Self Refresh Re-entry Control bit is set to 1b (REG[1C08h] bit 1 = 1b), the SDRAM will automatically re-enter self refresh mode after the specified number of cycles.

When this bit = 0b, exits the SDRAM from self refresh mode (disabled). (default)

When this bit = 1b, places the SDRAM in self refresh mode (enabled).

Note

The exit self refresh to active time is 3 MEMCLKs. To prevent data corruption, verify that this time does not violate the SDRAM specification before entering self refresh mode.

REG[1C0Ah] Memory Initialization Configuration Register

Default = 0000h — Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				SDRAM Initialization Sequence	SDRAM Load Mode	SDRAM Auto Refresh	SDRAM All Banks Precharge
7	6	5	4	3	2	1	0

Note
This register allows manual triggering of commands to the SDRAM, such as initializing and precharging. For normal use these bits do not have to be changed.

bit 3 SDRAM Initialization Sequence
This bit manually triggers a SDRAM initialization sequence.
When this bit = 0b, a SDRAM initialization sequence is not performed. (default)
When this bit = 1b, a SDRAM initialization sequence is performed. This bit is automatically cleared to 0b after it is written.

Note
1.This bit must not be set to 1b unless the SDRAM interface is idle.
2.If this bit is set to 1b while the SDRAM is in self refresh mode, the command is sent as the next command proceeding the next SDRAM write or read operation.

bit 2 SDRAM Load Mode
This bit manually triggers a load mode register command to the SDRAM. For normal use this bit does not have to be changed.
When this bit = 0b, a load mode register command is not issued. (default)
When this bit = 1b, a load mode register command is issued to the SDRAM. This bit is automatically cleared to 0b after it is written.

Note
1.This bit must not be set to 1b unless the SDRAM interface is idle.
2.If this bit is set to 1b while the SDRAM is in self refresh mode, the command is sent as the next command proceeding the next SDRAM write or read operation.

bit 1 SDRAM Auto Refresh
This bit manually triggers a precharge command followed by an auto refresh command to the SDRAM. For normal use this bit does not have to be changed.
When this bit = 0b, precharge and auto refresh commands are not issued. (default)
When this bit = 1b, precharge and auto refresh commands are issued with, but proceeding, the next SDRAM operation. This bit is automatically cleared to 0b after it is written.

bit 0 SDRAM All Banks Precharge
This bit manually triggers a precharge all banks command to the SDRAM. For normal use this bit does not have to be changed.
When this bit = 0b, a precharge all banks command is not issued. (default)
When this bit = 1b, a precharge all banks command is issued with, but proceeding, the next SDRAM operation. This bit is automatically cleared to 0b after it is written.

REG[1C0Ch] Memory Refresh Timer Register
Default = 0411h — Read/Write

SDRAM Auto Refresh Timer bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Auto Refresh Timer bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 SDRAM Auto Refresh Timer bits [15:0]
These bits control the period between SDRAM auto refresh cycles. These bits must not be set to a value less than 4h.
period between auto refresh cycles = REG[1C0Ch] bits 15-0 + 9 MEMCLK periods

The number of REF cycles per MEMCKE high pulse is controlled by REG[1C04h] bits 11-8.

REG[1C0Eh] is Reserved

This register is Reserved and should not be written.

REG[1C10h] SDRAM Mode Setting Value Register
Default = 0000h — Read Only

SDRAM Mode Setting Value bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Mode Setting Value bits 7- 0							
7	6	5	4	3	2	1	0

bits 15-0 SDRAM Mode Setting Value bits [15:0] (Read Only)
These bits indicate the value that is written to the SDRAM mode register. The mode register specifies the operational parameters for the external SDRAM.

REG[1C12h] Mobile SDRAM Configuration Register
Default = 4000h — Read/Write

TRSC bits 1-0		n/a					
15	14	13	12	11	10	9	8
Mobile Select	n/a	Auto Temperature Compensated Self Refresh Enable	Reserved		Partial Array Self Refresh Select bits 2-0		
7	6	5	4	3	2	1	0

bits 15-14 TRSC bits [1:0]

These bits specify the number of clocks between the Mode Register Set Cycles (clocks between Mode Setting and Extended Mode Setting) when mobile SDRAM is selected, REG[1C12h] bit 7 = 1b.

Table 10-46: Mode Register Set Cycle

REG[1C12h] bits 15-14	TRSC
00b	Reserved
01b	2 Clocks
10b	3 Clocks
11b	4 Clocks

bit 7 Mobile Select

This bit selects whether normal SDRAM or mobile SDRAM is used. When this bit is set, the Extended Mode Setting register is programmed for mobile SDRAM after the SDRAM is initialized (see REG[1C02h] bit 0).

When this bit = 0b, normal SDRAM is selected.

When this bit = 1b, mobile SDRAM is selected.

bit 5 Auto Temperature Compensated Self Refresh Enable

This bit controls the auto temperature compensated self refresh function.

When this bit = 0b, auto temperature compensated self refresh is disabled.

When this bit = 1b, auto temperature compensated self refresh is enabled.

bits 4-3 Reserved

These bits must be set to 00b.

bits 2-0 Partial Array Self Refresh Select bits [2:0]

These bits control which banks of the mobile SDRAM are self refreshed. The value of these bits should be programmed according to the requirements of the mobile SDRAM used. For details, refer to the Mobile SDRAM Specification.

Table 10-47: Partial Array Self Refresh Selection

REG[1C12h] bits 2-0	Partial Array Self Refresh
000b	All Banks
001b	Bank A and Bank B (BA1 = 0)
010b	Bank A (BA1=0 and BA0 = 0)
011b - 111b	Reserved

REG[1C14h] Mobile SDRAM Extended Mode Setting Register

Default = 0000h Read Only

Mobile SDRAM Extended Mode Setting bits 15-8							
15	14	13	12	11	10	9	8
Mobile SDRAM Extended Mode Setting bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0	Mobile SDRAM Extended Mode Setting bits [15:0] (Read Only) These bits indicates the value that is written to the SDRAM extended mode register. The extended mode register specifies the operational parameters for the external mobile SDRAM.

10.4.7 PWM Registers

Note
The pins used by the PWM interface are multiplexed with GPIO function pins. Therefore, before enabling the PWM interface, the appropriate GPIO pins must be configured for use by the PWM interface. For a summary of GPIO pin usage, see Section 5.6, “GPIO Pin Mapping” on page 34.

REG[3400h] PWM Control Register
Default = 0000h — Read/Write

Reserved				Blue Enable	Green Enable	Red Enable	White Enable
15	14	13	12	11	10	9	8
n/a	Reserved	AUDIN Active State Select	AUDIN Control Enable	n/a	Output Polarity	PWM RGB Output Enable	PWM White Output Enable
7	6	5	4	3	2	1	0

Note
If REG[3400h] bits 11-8 equal 0000b (all PWM outputs are disabled), the clock to the entire PWM circuit is dynamically disabled in order to save power and minimize current drain.

bits 15-12 Reserved
The default value for these bits is 0000b.

bit 11 Blue Enable
This bit controls the Blue LED PWM output. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, the PWMB output is disabled (becomes logic 0 before the polarity inversion circuit specified by REG[3400h] bit 2).
When this bit = 1b, the PWMB output is enabled.

Note
If all of the Red Enable, Green Enable, and Blue Enable bits are disabled, then the 128 clock reference point described in Section 15.1, “PWM Circuit Overview” on page 177 is reset to zero.

bit 10 Green Enable
This bit controls the Green LED PWM output. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, the PWMG output is disabled (becomes logic 0 before the polarity inversion circuit specified by REG[3400h] bit 2).
When this bit = 1b, the PWMG output is enabled.

Note
If all of the Red Enable, Green Enable, and Blue Enable bits are disabled, then the 128 clock reference point described in Section 15.1, “PWM Circuit Overview” on page 177 is reset to zero.

bit 9 Red Enable
This bit controls the Red LED PWM output. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, the PWMR output is disabled (becomes logic 0 before the polarity inversion circuit specified by REG[3400h] bit 2).
When this bit = 1b, the PWMR output is enabled.

Note
If all of the Red Enable, Green Enable, and Blue Enable bits are disabled, then the 128 clock reference point described in Section 15.1, “PWM Circuit Overview” on page 177 is reset to zero.

bit 8 White Enable
This bit controls the White LED PWM output. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, the PWMW output is disabled (becomes logic 0 before the polarity inversion circuit specified by REG[3400h] bit 2).
When this bit = 1b, the PWMW output is enabled.

bit 6 Reserved
The default value for this bit is 0b.

bit 5 AUDIN Active State Select
When AUDIN control of the PWM outputs is enabled (REG[3400h] bit 4 = 1b), this bit selects the active state of the digital audio input, AUDIN. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, a high on the digital audio input enables the color PWM outputs.
When this bit = 1b, a low on the digital audio input enables the color PWM outputs.

Note
This bit should be used in conjunction with REG[0C0Eh] bits 7-6 to set the function of GPIOD3.

bit 4 AUDIN Control Enable
This bit enables/disables control of the three color PWM outputs (PWMB, PWMG, PWMR) by the digital audio input, AUDIN. For PWM pin mapping, see Section 5.7, “PWM Interface Pin Mapping” on page 35.
When this bit = 0b, the digital audio input does not control the PWM outputs.
When this bit = 1b, the digital audio input controls the PWM outputs.

Note
Before using the AUDIN input, the appropriate GPIO pin must be configured for use by the PWM interface.

bit 2 Output Polarity
This bit specifies the polarity of the output pin relative to the digital value output by the PWM circuit for all 4 LED output pins (three color and one white).
When this bit = 0b, the LED pin voltage is driven low when a logic 1 is driven from the PWM circuit and driven high when a logic 0 is driven from the PWM circuit.
When this bit = 1b, the LED output pin is driven high when the PWM circuit is driving a logic 1.

bit 1 PWM RGB Output Enable
This bit controls the three color LED PWM outputs (PWMB, PWMG, PWMR).
When this bit = 0b, the color LED PWM outputs are held high.
When this bit = 1b, the color LED PWM outputs are enabled.

Note
If both bit 0 and bit 1 are zero (i.e. both PWM outputs are held high), then the clock to the entire PWM circuit is turned off (to save power and minimize current drain) once all PWM Enable bits are disabled (see REG[3400h] bits 11-8).

bit 0 PWM White Output Enable
This bit controls the white LED PWM output (PWMW).
When this bit = 0b, the white LED PWM output is held high.
When this bit = 1b, the white LED PWM output is enabled.

Note
If both bit 0 and bit 1 are zero (i.e. both PWM outputs are held high), then the clock to the entire PWM circuit is turned off (to save power and minimize current drain) once all PWM Enable bits are disabled (see REG[3400h] bits 11-8).

REG[3402h] PWM Clock Divide Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a				PWM Clock Divide Select bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 PWM Clock Divide Select bits [3:0]
These bits select the clock divide for the PWM clock used by the PWMR, PWMG and PWMB circuits. It has no effect on PWMW. The clock source for the PWM clock is the internal clock PWMSRCCLK. PWMSRCCLK should be configured to provide an approximately 16KHz clock which allows for an LED pulse rate ranging from 0.5Hz to 8Hz. For further details on PWMSRCLK, see Section Chapter 9, “Clocks” on page 69.

Table 10-48: PWM Clock Divide Selection

REG[3402h] bits 3-0	PWM Clock Divide Ratio
0000b	1:1
0001b	2:1
0010b	4:1
0011b	6:1
0100b	8:1
0101b	10:1
0110b	12:1
0111b	14:1
1000b	16:1
1001b - 1111b	Reserved (PWM Clock is stopped)

REG[3404h] Red On/Off Control Register
Default = 0000h Read/Write

n/a	Red Off bits 6-0						
15	14	13	12	11	10	9	8
n/a	Red On bits 6-0						
7	6	5	4	3	2	1	0

bits 14-8 Red Off bits [6:0]
These bits specify the point at which the red LED turns off relative to the start of the 128 clock pulse cycle. This value must be greater than that of the “Red On” value specified in REG[3404h] bits 6-0 or unpredictable results may occur. For further information on using PWM, see Section Chapter 15, “Pulse Width Modulation (PWM)” on page 177.
REG[3404h] bits 14-8 = Off Time - 1

Note
If a value of 7Fh is entered, the LED is on for the entire duration of the red duty cycle, REG[340Ch] bits 3-0.

bits 6-0 Red On bits [6:0]
These bits specify the point at which the red LED turns on relative to the start of the 128 clock pulse cycle. A value of 0 means the LED starts the turn on sequence immediately at the start of the 128 clock cycle. For further information on using PWM, see Section Chapter 15, “Pulse Width Modulation (PWM)” on page 177.

REG[3406h] Green On/Off Control Register
Default = 0000h — Read/Write

n/a	Green Off bits 6-0						
15	14	13	12	11	10	9	8
n/a	Green On bits 6-0						
7	6	5	4	3	2	1	0

bits 14-8 Green Off bits [6:0]
These bits specify the point at which the green LED turns off relative to the start of the 128 clock pulse cycle. This value must be greater than that of the "Green On" value specified in REG[3406h] bits 6-0 or unpredictable results may occur. For further information on using PWM, see Section Chapter 15, "Pulse Width Modulation (PWM)" on page 177.
REG[3406h] bits 14-8 = Off Time - 1

Note
If a value of 7Fh is entered, the LED is on for the entire duration of the green duty cycle, REG[340Ch] bits 7-4.

bits 6-0 Green On bits [6:0]
These bits specify the point at which the green LED turns on relative to the start of the 128 clock pulse cycle. A value of 0 means the LED starts the turn on sequence immediately at the start of the 128 clock cycle. For further information on using PWM, see Section Chapter 15, "Pulse Width Modulation (PWM)" on page 177.

REG[3408h] Blue On/Off Control Register
Default = 0000h — Read/Write

n/a	Blue Off bits 6-0						
15	14	13	12	11	10	9	8
n/a	Blue On bits 6-0						
7	6	5	4	3	2	1	0

bits 14-8 Blue Off bits [6:0]
These bits specify the point at which the blue LED turns off relative to the start of the 128 clock pulse cycle. This value must be greater than that of the "Blue On" value specified in REG[3408h] bits 6-0 or unpredictable results may occur. For further information on using PWM, see Section Chapter 15, "Pulse Width Modulation (PWM)" on page 177.
REG[3408h] bits 14-8 = Off Time - 1

Note
If a value of 7Fh is entered, the LED is on for the entire duration of the blue duty cycle, REG[340Ch] bits 11-8.

bits 6-0 Blue On bits [6:0]
These bits specify the point at which the blue LED turns on relative to the start of the 128 clock pulse cycle. A value of 0 means the LED starts the turn on sequence immediately at the start of the 128 clock cycle. For further information on using PWM, see Section Chapter 15, "Pulse Width Modulation (PWM)" on page 177.

REG[340Ah] PWM Slope Register
Default = 0000h — Read/Write

n/a	LED Pulse Counter (M) bits 2-0	Blue Slope bits 3-0

REG[340Ah] PWM Slope Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Green Slope bits 3-0				Red Slope bits 3-0			
7	6	5	4	3	2	1	0

Note

Using a slope that is not divisible by the color's maximum duty cycle before the down slope will result in an asymmetrical signal.

bits 14-12 LED Pulse Counter (M) bits [2:0]

These bits determine the M value used for the slope calculation. At every M+1 clocks of the 128 clock wide LED pulse the duty cycle increases by a value (1/16 x N), where N is determined by the corresponding Red (bits 3-0), Green (bits 7-4), and Blue (bits 11-8) Slope bits. These bits have no effect when the Slope bits for a particular color are set to 0. REG[340Ah] bits 14-12 = M value for slope calculation - 1

bits 11-8 Blue Slope bits [3:0]

These bits specify the rate of change at which the duty cycle changes as the blue LED goes from completely off to the maximum duty cycle specified in REG[340Ch] bits 11-8. At every output pulse (M+1) of 128 pulse counter (M is specified in REG[340Ah] bits 14-12), the duty cycle increases by (1/16 x N) where N is the decimal value represented by these bits. If these bits are set to a value of 0h, the duty cycle immediately changes from completely off, to the maximum duty cycle as specified by the Blue Duty Cycle bits, REG[340Ch] bits 11-8.

bits 7-4 Green Slope bits [3:0]

These bits specify the rate of change at which the duty cycle changes as the green LED goes from completely off to the maximum duty cycle specified in REG[340Ch] bits 7-4. At every output pulse (M+1) of 128 pulse counter (M is specified in REG[340Ah] bits 14-12), the duty cycle increases by (1/16 x N) where N is the decimal value represented by these bits. If these bits are set to a value of 0h, the duty cycle immediately changes from completely off, to the maximum duty cycle as specified by the Green Duty Cycle bits, REG[340Ch] bits 7-4.

bits 3-0 Red Slope bits [3:0]

These bits specify the rate of change at which the duty cycle changes as the red LED goes from completely off to the maximum duty cycle specified in REG[340Ch] bits 3-0. At every output pulse (M+1) of 128 pulse counter (M is specified in REG[340Ah] bits 14-12), the duty cycle increases by (1/16 x N) where N is the decimal value represented by these bits. If these bits are set to a value of 0h, the duty cycle immediately changes from completely off, to the maximum duty cycle as specified by the Red Duty Cycle bits, REG[340Ch] bits 3-0.

REG[340Ch] PWM Duty Cycle Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a				Blue Duty Cycle bits 3-0			
7	6	5	4	3	2	1	0
Green Duty Cycle bits 3-0				Red Duty Cycle bits 3-0			

Note
Using a slope that is not divisible by the color's maximum duty cycle before the down slope will result in an asymmetrical signal.

bits 11-8 Blue Duty Cycle bits [3:0]
These bits specify the "full-on" duty cycle which determines the maximum brightness that the LED reaches at the peak of the pulse. A value of Fh indicates full brightness (i.e. continuously on). A value of 0 means the LED is on for 1/16th of the time.

Note
When the blue slope (REG[340Ah] bits 11-8) is non-zero, the blue duty cycle must not be set to 1111b (Fh).

bits 7-4 Green Duty Cycle bits [3:0]
These bits specify the "full-on" duty cycle which determines the maximum brightness that the LED reaches at the peak of the pulse. A value of Fh indicates full brightness (i.e. continuously on). A value of 0 means the LED is on for 1/16th of the time.

Note
When the green slope (REG[340Ah] bits 7-4) is non-zero, the green duty cycle must not be set to 1111b (Fh).

bits 3-0 Red Duty Cycle bits [3:0]
These bits specify the "full-on" duty cycle which determines the maximum brightness that the LED reaches at the peak of the pulse. A value of Fh indicates full brightness (i.e. continuously on). A value of 0 means the LED is on for 1/16th of the time.

Note
When the red slope (REG[340Ah] bits 3-0) is non-zero, the red duty cycle must not be set to 1111b (Fh).

REG[340Eh] White LED Control Register

Default = 0000h Read/Write

n/a		White LED Duty Cycle bits 5-0					
15	14	13	12	11	10	9	8
n/a		White LED Period bits 5-0					
7	6	5	4	3	2	1	0

bits 13-8 White LED Duty Cycle bits [5:0]

These bits specify the duty cycle, or “on” time, for the White LED. A value of 00h represents the dimmest LED brightness (the shortest time which the LED can be “on” for each period as specified in REG[340Eh] bits 5-0. When the white LED duty cycle is set to 3Fh, the LED is continuously “on”.

REG[340Eh] bits 13-8 = white LED duty cycle - 1

Note

The output of the white LED can be forced to an “off” state using the PWM White Output Enable bit (REG[3400h] bit 0) or the White Enable bit (REG[3400h] bit 8).

bits 5-0 White LED Period bits [5:0]

These bits specify the period of the white LED PWM output. For a PWMSRCCLK of approximately 16kHz, the following formula provides a frequency range of between 64Hz to 1Hz for the white LED.

PWM period = 256 x (1 ÷ PWMSRCCLK) x ((REG[340Eh] bits 5-0) + 1)

REG[3410h] through REG[5010h] are Reserved

These registers are Reserved and should not be written.

Chapter 11 Power Save Modes

11.1 Power-On/Power-Off Sequence

The following power-on/power-off sequence is recommended for the S1D13L04.

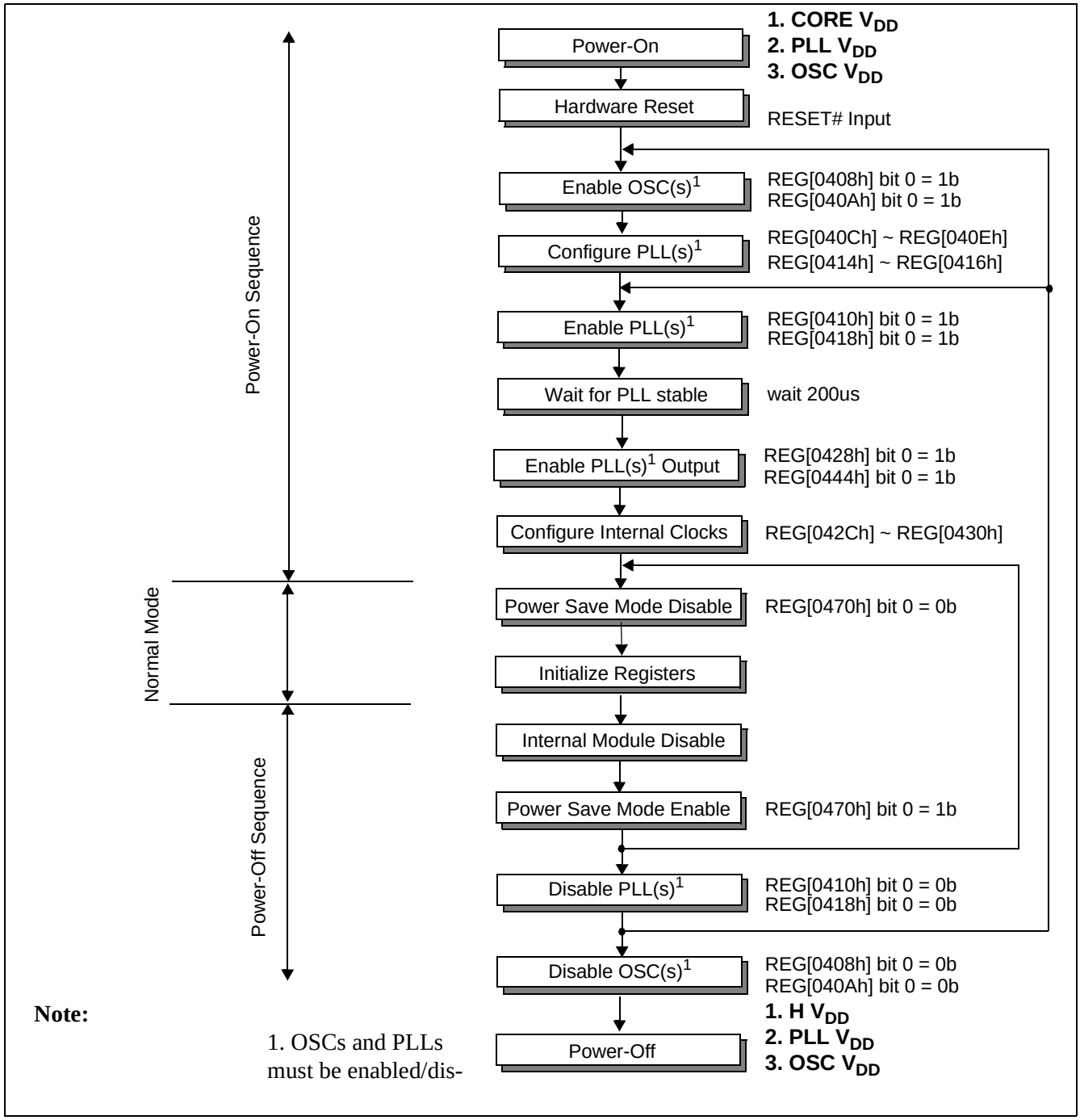

Figure 11-1: Power-On/Power-Off Sequence

11.2 Operational Modes

The S1D13L04 operates in the following modes.

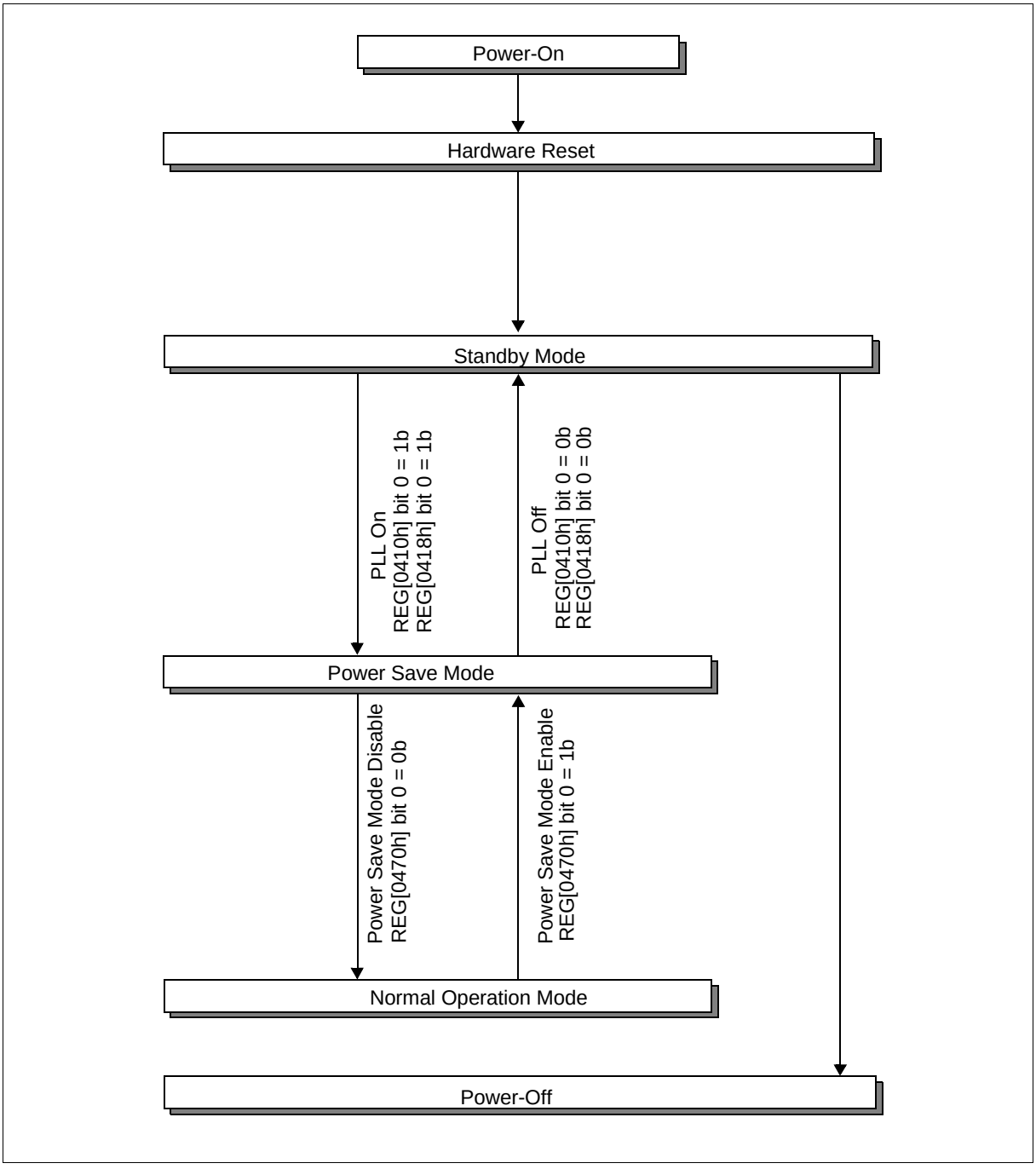

Figure 11-2: Operational Modes

11.2.1 Power-On

When powering-on the S1D13L04, the following sequence must be used.

1. CORE V_{DD} On, OSC V_{DD}, PLL V_{DD} On
2. H V_{DD} (HVDD1 ~ HVDD5) On

Note
H V_{DD} is 0.8V when CORE V_{DD} is enabled and H V_{DD} is not enabled.

11.2.2 Reset

After power-on, an active low hardware reset pulse, which is two external clock cycles (see Power-On Section and RESET# section???) in length, must be input to the S1D13L04 RESET# pin. All registers are reset by a hardware reset. After releasing the RESET# signal, the Clock Setting registers are immediately accessible.

A software reset is enabled by writing a value of A55Ah to REG[0460h]. All synchronous registers are reset to their default values (see Section 10.1, “Register Mapping” on page 71).

11.2.3 Standby Mode

Standby Mode offers the lowest power consumption because all internal clock supplies are stopped and the PLL is disabled. This mode must be entered before turning off the power supplies or setting the PLL registers.

In standby mode, the asynchronous registers (see Section 10.1, “Register Mapping” on page 71) can be accessed.

11.2.4 Power Save Mode

Power Save Mode stops all internal clock supplies. This mode must be entered before configuring the PWM Source Clock Control Register (REG[042Eh]). Also, there may be up to a 200us delay before the PLL output becomes stable after it is enabled. The S1D13L04 should be in Power Save Mode during this time.

In power save mode, the asynchronous registers (see Section 10.1, “Register Mapping” on page 71) can be accessed.

Note
When Power Save Mode is enabled, synchronous registers and SDRAM memory must not be accessed.

11.2.5 Normal Mode

All functions are available in Normal Mode. However, clocks to modules that are not in use are dynamically stopped. Before enabling Power Save Mode (REG[0470h] bit 0 = 1b) from Normal Mode, confirm that the memory controller is idle (REG[1C02h] bit 7= 1b).

11.2.6 Power-Off

When powering-off the S1D13L04, the following sequence must be used.

1. H V_{DD} (HVDD1 ~ HVDD5) Off
2. OSC V_{DD}, PLL V_{DD} Off, CORE V_{DD} Off

Note
H V_{DD} is 0.8V when CORE V_{DD} is enabled and H V_{DD} is not enabled.

11.3 Power Save Mode Functions

To place the S1D13L04 into a power efficient state, perform the following steps.

1. Place the SDRAM into “Self Refresh Mode”.
    a. Set REG[1C06h] bit 14 = 1b.
    b. Set REG[1C08h] bits 1-0 = 11b.
2. Enable Power Save Mode.
    a. Set REG[0470h] = 0001h.

To return the S1D13L04 into normal operating mode, perform the following steps.

1. Disable Power Save Mode.
    a. Set REG[0470h] = 0000h.
2. Remove the SDRAM from “Self Refresh Mode”.
    a. Set REG[1C06h] bit 14 = 0b.
    b. Set REG[1C08h] bits 1-0 = 00b.
    c. Set REG[1C0Ah] = 0002h (executes an auto refresh).

Chapter 12 Data Formats

12.1 Memory Data Formats

The S1D13L04 supports 8/16/32 bpp color depths for the Main and PIP1 windows. The selected color depth is controlled by the Main Window Bpp Select bits (REG[0832h] bits 2-0) and the PIP1 Window Bpp Select bits (REG[0832h] bits 6-4), respectively. The image data is stored in memory as shown in the tables below. For 8 bpp, R_0^2 defines the most significant bit of R data for pixel 0.

Table 12-1: 8 Bpp (RGB 3:3:2) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	R_1^2	R_1^1	R_1^0	G_1^2	G_1^1	G_1^0	B_1^1	B_1^0	R_0^2	R_0^1	R_0^0	G_0^2	G_0^1	G_0^0	B_0^1	B_0^0
0002h	R_3^2	R_3^1	R_3^0	G_3^2	G_3^1	G_3^0	B_3^1	B_3^0	R_2^2	R_2^1	R_2^0	G_2^2	G_2^1	G_2^0	B_2^1	B_2^0
0004h	R_5^2	R_5^1	R_5^0	G_5^2	G_5^1	G_5^0	B_5^1	B_5^0	R_4^2	R_4^1	R_4^0	G_4^2	G_4^1	G_4^0	B_4^1	B_4^0
0006h	R_7^2	R_7^1	R_7^0	G_7^2	G_7^1	G_7^0	B_7^1	B_7^0	R_6^2	R_6^1	R_6^0	G_6^2	G_6^1	G_6^0	B_6^1	B_6^0

Table 12-2: 16 Bpp (RGB 5:6:5) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
0004h	R_2^4	R_2^3	R_2^2	R_2^1	R_2^0	G_2^5	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0
0006h	R_3^4	R_3^3	R_3^2	R_3^1	R_3^0	G_3^5	G_3^4	G_3^3	G_3^2	G_3^1	G_3^0	B_3^4	B_3^3	B_3^2	B_3^1	B_3^0

Table 12-3: 32 Bpp (RGB 8:8:8) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	—	—	—	—	—	—	—	—	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
0004h	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
0006h	—	—	—	—	—	—	—	—	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0

The PIP2 window supports ARGB, which is used for alpha blending, in addition to the standard 8/16/32 bpp color depths. The PIP2 Window ARGB Format Select bit (REG[0832h] bit 11) determines whether an ARGB or RGB format is specified, while the PIP2 Window Bpp Select bits (REG[0832h] bits 10-8) select the actual format. For ARGB data formats, the image data is stored in memory as shown below.

Table 12-4: 16 Bpp (ARGB 1:5:5:5) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	A_0^0	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	A_1^0	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
0004h	A_2^0	R_2^4	R_2^3	R_2^2	R_2^1	R_2^0	G_2^4	G_2^3	G_2^2	G_2^1	G_2^0	B_2^4	B_2^3	B_2^2	B_2^1	B_2^0
0006h	A_3^0	R_3^4	R_3^3	R_3^2	R_3^1	R_3^0	G_3^4	G_3^3	G_3^2	G_3^1	G_3^0	B_3^4	B_3^3	B_3^2	B_3^1	B_3^0

Table 12-5: 16 Bpp (ARGB 4:4:4:4) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	A_0^3	A_0^2	A_0^1	A_0^0	R_0^3	R_0^2	R_0^1	R_0^0	G_0^3	G_0^2	G_0^1	G_0^0	B_0^3	B_0^2	B_0^1	B_0^0
0002h	A_1^3	A_1^2	A_1^1	A_1^0	R_1^3	R_1^2	R_1^1	R_1^0	G_1^3	G_1^2	G_1^1	G_1^0	B_1^3	B_1^2	B_1^1	B_1^0
0004h	A_2^3	A_2^2	A_2^1	A_2^0	R_2^3	R_2^2	R_2^1	R_2^0	G_2^3	G_2^2	G_2^1	G_2^0	B_2^3	B_2^2	B_2^1	B_2^0
0006h	A_3^3	A_3^2	A_3^1	A_3^0	R_3^3	R_3^2	R_3^1	R_3^0	G_3^3	G_3^2	G_3^1	G_3^0	B_3^3	B_3^2	B_3^1	B_3^0

Table 12-6: 32 Bpp (ARGB 8:8:8:8) Format Data

Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000h	G_0^7	G_0^6	G_0^5	G_0^4	G_0^3	G_0^2	G_0^1	G_0^0	B_0^7	B_0^6	B_0^5	B_0^4	B_0^3	B_0^2	B_0^1	B_0^0
0002h	A_0^7	A_0^6	A_0^5	A_0^4	A_0^3	A_0^2	A_0^1	A_0^0	R_0^7	R_0^6	R_0^5	R_0^4	R_0^3	R_0^2	R_0^1	R_0^0
0004h	G_1^7	G_1^6	G_1^5	G_1^4	G_1^3	G_1^2	G_1^1	G_1^0	B_1^7	B_1^6	B_1^5	B_1^4	B_1^3	B_1^2	B_1^1	B_1^0
0006h	A_1^7	A_1^6	A_1^5	A_1^4	A_1^3	A_1^2	A_1^1	A_1^0	R_1^7	R_1^6	R_1^5	R_1^4	R_1^3	R_1^2	R_1^1	R_1^0

Chapter 13 Display Functions

The S1D13L04 supports SwivelView and Mirror functions for both the PIP2 window and the View Port (Main+PIP1). These functions are controlled using Display Mode Setting Register 2 (REG[0834h]) and are explained in the following sections.

13.1 SwivelView™

Most computer displays are refreshed in landscape orientation - from left to right and top to bottom. Computer images are stored in the same manner. SwivelView is designed to rotate the displayed image on a LCD by 180° in a counter-clockwise direction.

This rotation is done in hardware and is transparent to the user for all display buffer reads and writes. This is accomplished by rotating the image during display refresh. Therefore, the image is not actually rotated in the display buffer since there is no address translation required during Host CPU reads/writes. By processing the rotation in hardware, SwivelView offers a performance advantage over software rotation of the displayed image.

The SwivelView function can be independently controlled for either the View Port (Main+PIP1) using REG[0834h] bits 1-0, the PIP2 window using REG[0834h] bits 9-8, or both.

13.1.1 0° SwivelView

The following figure shows the relationship between the image stored in the display buffer and the image as displayed on the LCD panel when 0° SwivelView is selected. The image is written to the S1D13L04 display buffer in the following sense: A-B-C-D. However, the LCD display is refreshed in the following sense: D-C-B-A.

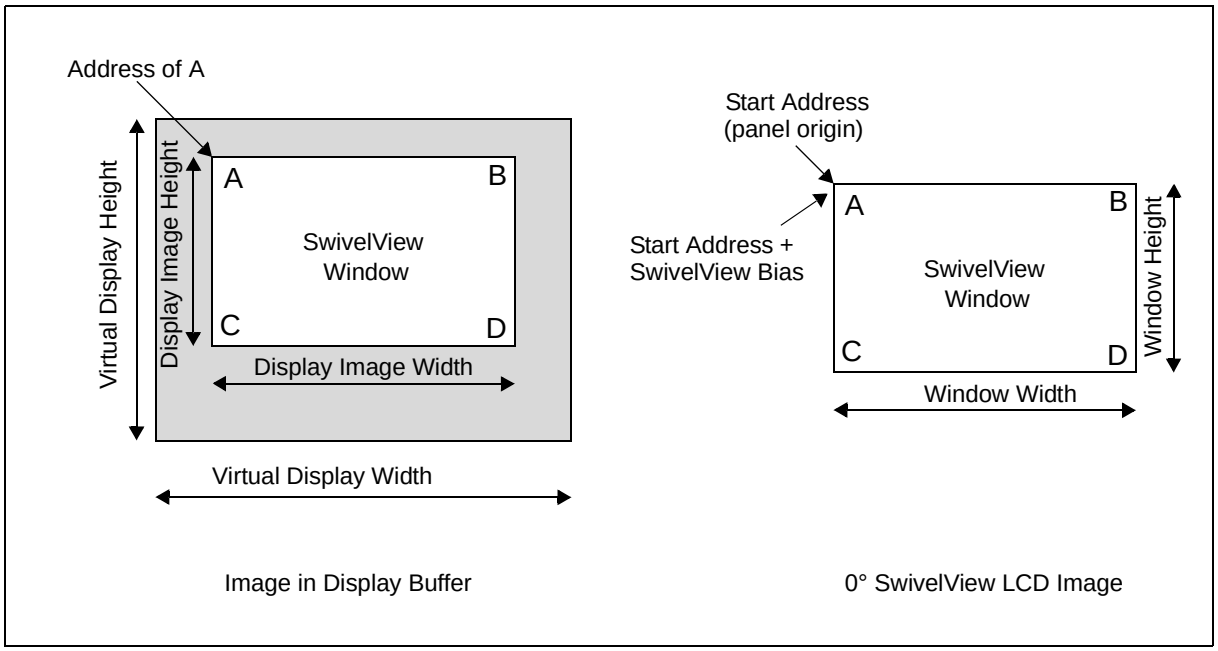

Figure 13-1: Relationship Between Display Buffer Image and LCD Image for 0° SwivelView

Display Start Address

The display refresh circuitry starts at pixel “A”, therefore the Start Address registers must be programmed with the address of pixel “A” and the SwivelView Bias must be set to 0.

SwivelView Bias = 0

Line Address Offset

The Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset= Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the View Port or PIP2 window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x virtual panel height] x bpp ÷ 8

13.1.2 180° SwivelView

The following figure shows the relationship between the image stored in the display buffer and the image as displayed on the LCD panel when 180° SwivelView is enabled. The image is written to the S1D13L04 display buffer in the following sense: A-B-C-D. However, the LCD display is refreshed in the following sense: D-C-B-A.

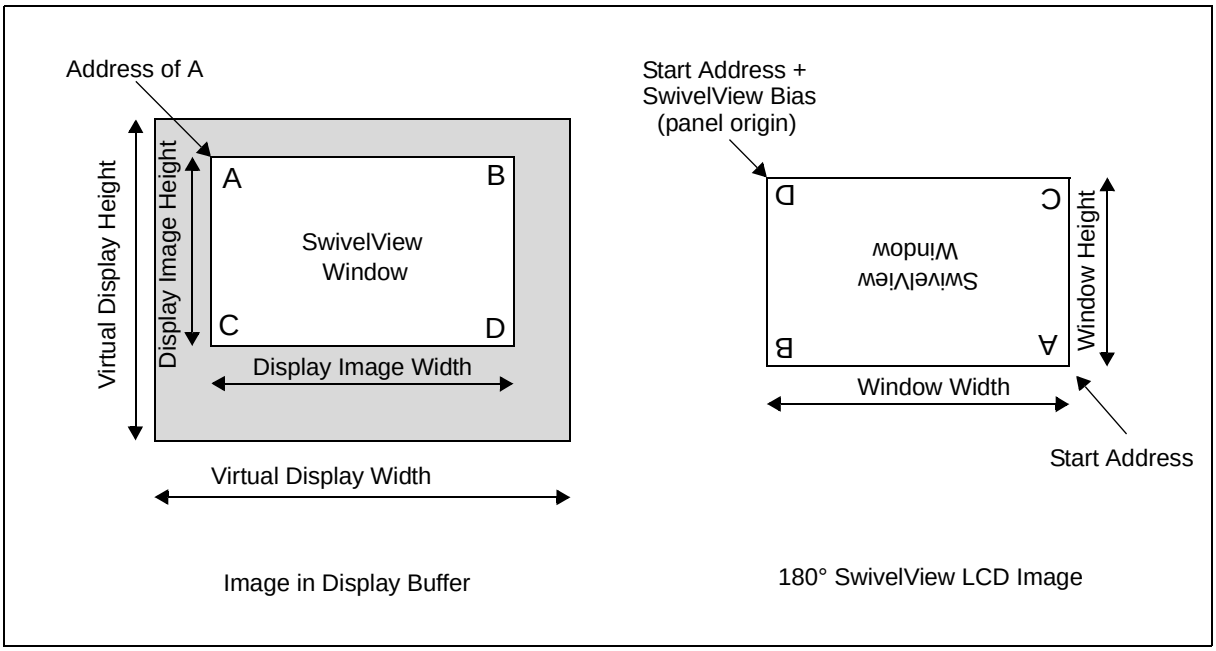

Figure 13-2: Relationship Between Display Buffer Image and LCD Image for 180° SwivelView

Display Start Address

The display refresh circuitry starts at pixel “D”, therefore the Start Address registers must be programmed with the address of pixel “A” and the SwivelView Bias should be programmed as follows.

SwivelView Bias = Line Address Offset x Window Height - (bpp ÷ 8)

Line Address Offset

The Line Address Offset is set as byte counts per 1 line of virtual image.

Line Address Offset= Virtual Image Width x bpp ÷ 8

Memory Address of a Given Pixel

To calculate the address of pixel at any given position for the View Port or PIP2 window, use the following formula.

Memory Address (X,Y) = [(X - 1) + (Y - 1) x virtual panel height] x bpp ÷ 8

13.2 Mirror Display

Most computer displays are refreshed from left to right and top to bottom. Computer images are stored in the same manner. Mirror Display is designed to refresh the display from right to left, thus “mirroring” the display. Mirror Display is performed by hardware and no changes in the storage of display data in the display buffer are required. By mirroring the image in hardware, Mirror Display offers a performance advantage over software mirroring of the same image.

Mirror Display can be independently enabled for either the View Port (Main+PIP1) using REG[0834h] bit 2, the PIP2 window using REG[0834h] bit 10, or both.

13.2.1 Mirror Display for 0° SwivelView

The following figure shows the relationship between the image stored in the display buffer and the image as displayed on the LCD panel when no rotation is selected (0° SwivelView). The image is written to the S1D13L04 display buffer in the following sense: A-B-C-D. However, the LCD display is refreshed in the following sense: B-A-D-C.

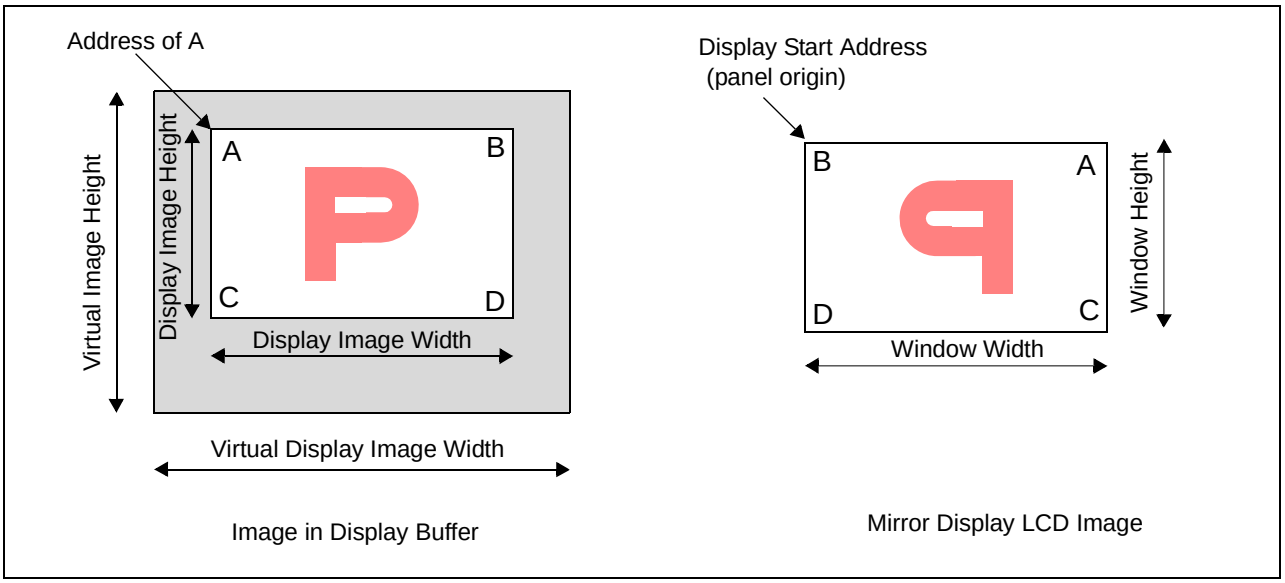

Figure 13-3: Relationship Between Display Buffer Image and LCD Image for Mirror Display (0° SwivelView)

Display Start Address

The display refresh circuitry starts at pixel “B”, therefore the Display Start Address registers must be programmed with the address of pixel “B”.

Display Start Address= Address of A + Line Address Offset - (bpp ÷ 8)

Line Address Offset

The Line Address Offset is set to the number of bytes per line of virtual image.

Line Address Offset= Virtual Image Width x bpp ÷ 8

13.2.2 Mirror Display Combined with SwivelView Modes

When both Mirror Display and SwivelView are enabled, the image is rotated by the SwivelView function after the Mirror Display function takes place. The Display Start Address must be set to the left upper pixel of display image.

Mirror Display with 180° SwivelView

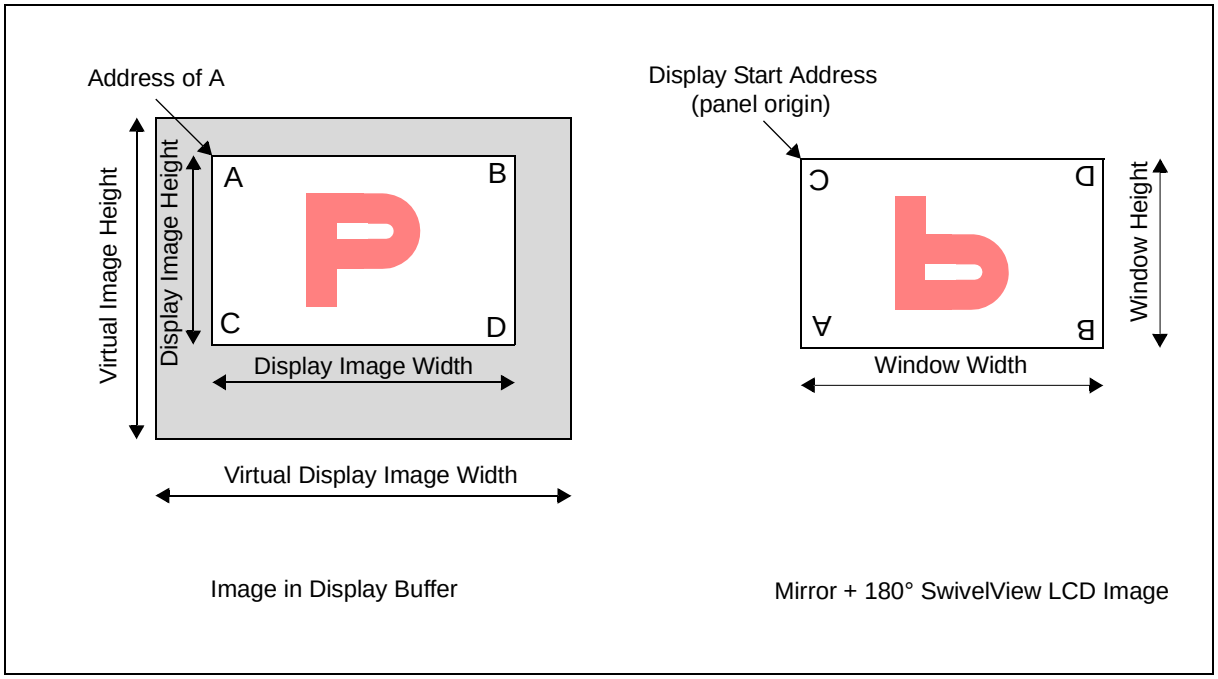

Figure 13-4: Mirror Display with 180° SwivelView Display

13.3 Gamma Correction

The S1D13L04 performs gamma correction using two Look-up Tables (LUTs) which are referred to as Bank A and Bank B. Each LUT has 256 (8-bit) entries for each RGB color component. The Bank used for gamma correction is selected using REG[083Eh] bits 5-4.

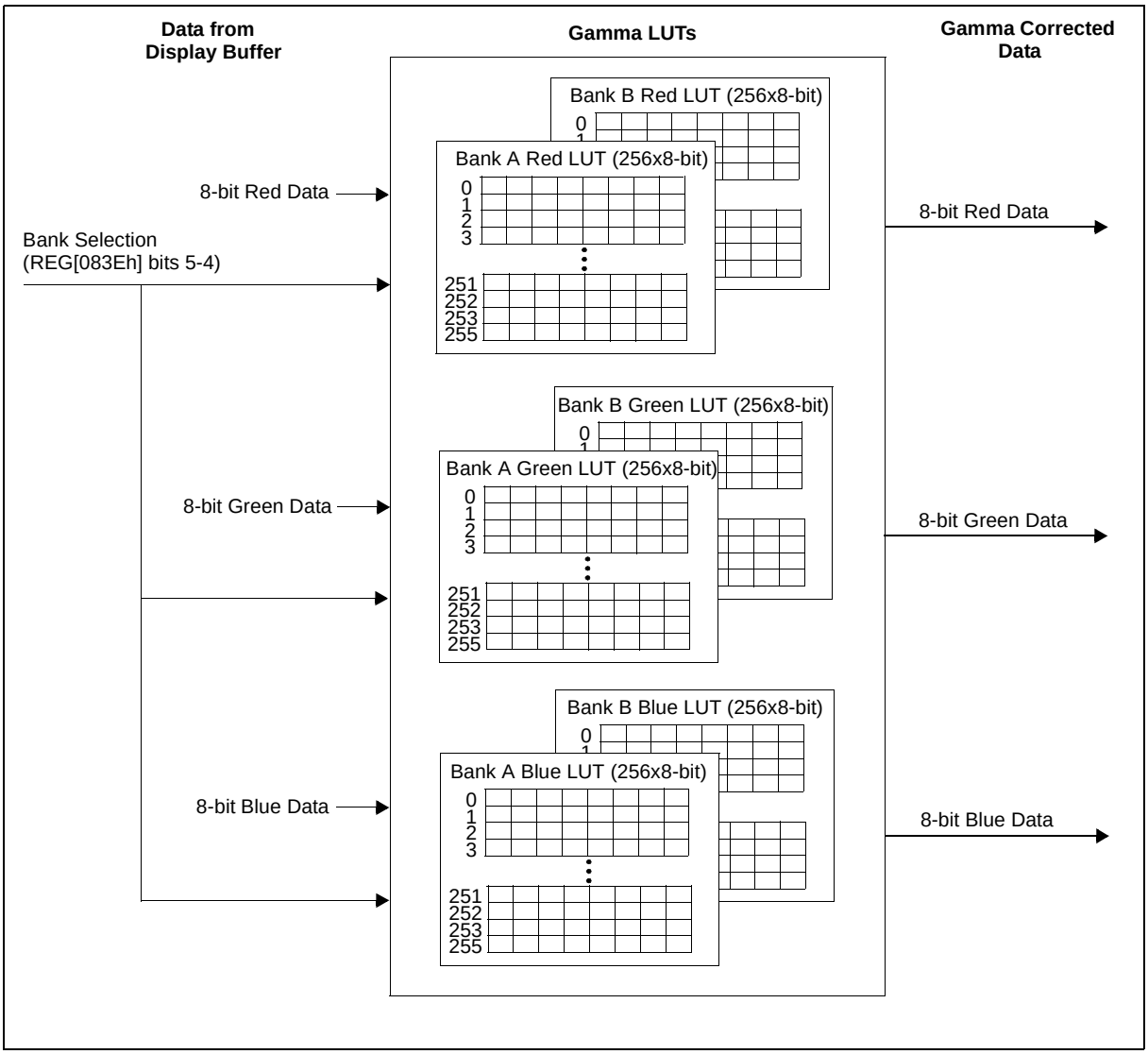

Figure 13-5: Gamma LUT Architecture for Color Modes

Note
In 16 bpp and 8 bpp, the extra bits required for the LUT index are created according to the setting of the Input Data Extra Bit Expansion Enable bit, REG[083Eh] bit 3.

13.3.1 Gamma LUT Bank Selection

There are four bank selection modes (see REG[083Eh] bits 5-4) which determine the windows (Main, PIP1, or PIP2) that are gamma corrected using Bank A or Bank B data. Two bank selection modes allow Gamma Correction using one Bank while the other Bank is being programmed. One mode allows different windows to be gamma corrected based on different banks, and one mode allows for both banks to be programmed together.

The following bank selection modes are available.

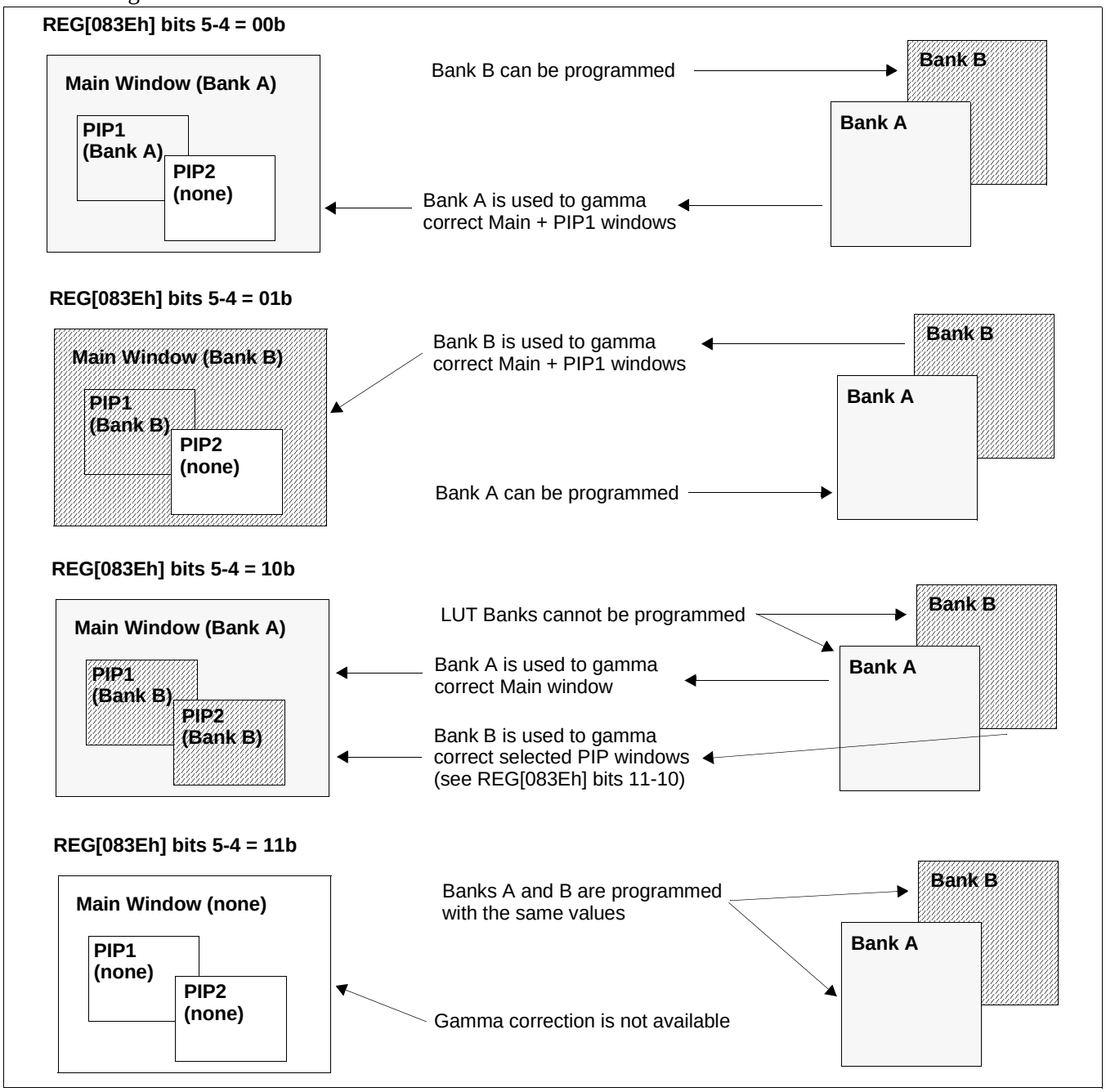

Figure 13-6: Gamma LUT Bank Selection

13.3.2 Programming the Gamma LUTs

The following procedure should be used to program the Gamma LUTs.

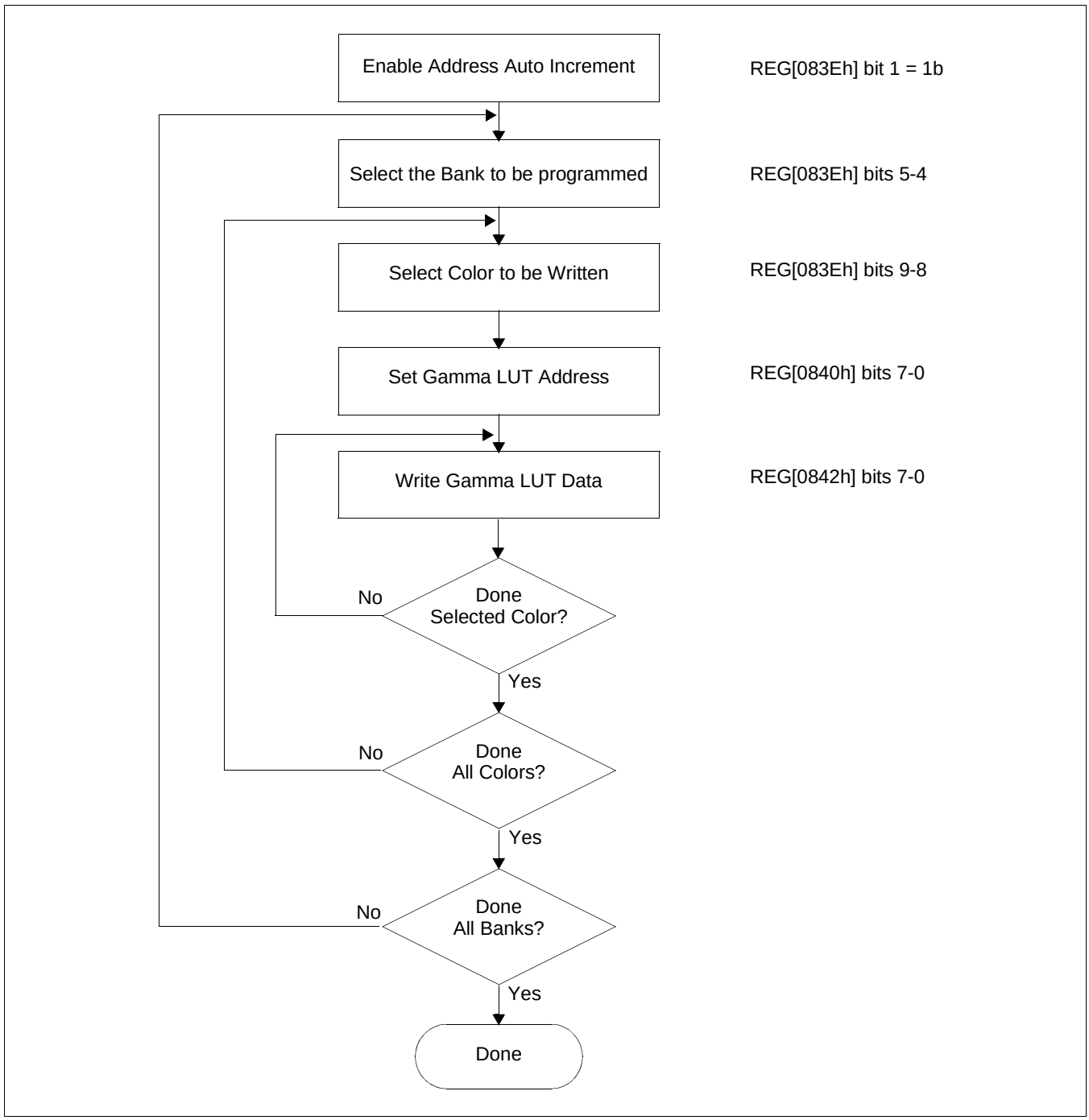

Figure 13-7: Gamma LUT Programming Flowchart

13.4 Pseudo Color Mode

The S1D13L04 supports Pseudo Color Mode which is used to minimize the change in image color quality when the color depth of the image is lowered for output to a panel. This is necessary for panels with a smaller data bus width than the display output size. For example if the S1D13L04 is configured for a 16-bit TFT panel, the internal display image data is RGB 8:8:8 (24-bit) but must be converted to RGB 5:6:5 (16-bit) for output to the panel.

When Pseudo Color Mode is disabled (REG[0844h] bits 2-0 = 000b), each color component (RGB) is rounded down to the data bus width of the panel. When enabled, the following are selectable.

- 2x2 Matrix Dither - REG[0844h] bits 2-0 = 001b
- FRM - REG[0844h] bits 2-0 = 010b
- Error Diffusion - REG[0844h] bits 2-0 = 100b

To determine the optimum Pseudo Color Mode, it may be necessary to perform a visual evaluation for each specific implementation.

Chapter 14 SDRAM Interface

The S1D13L04 SDRAM is designed to use external SDRAM or mobile SDRAM. It supports x16 SDRAM interfaces which allows for SDRAM sizes of 8/16M bytes (64/128Mbit). The S1D13L04 includes no embedded memory.

The S1D13L04 uses the external SDRAM for the display buffer. It is addressable through direct or indirect access modes. For details on addressing the memory, refer to Section Chapter 8, “Memory Map” on page 66.

14.1 SDRAM Initialization

The SDRAM must be initialized using the SDRAM Configuration registers (REG[1C00h] ~ REG[1C14h]) before using the SDRAM. The initialization sequence is differs depending on whether normal SDRAM or Mobile SDRAM is used. The recommended initialization sequence for each type of SDRAM is included in the next sections.

14.1.1 Initializing Normal SDRAM

The following sequence should be used to initialize normal SDRAM. For details on specific SDRAM requirements, refer to the SDRAM specification.

1. Wait at least 100µs after SDRAM Power Up. (For details, refer to the SDRAM specification.)
2. Configure Memory Configuration Register 1 (REG[1C04h]) according to the requirements of the SDRAM used.
3. Configure Memory Configuration Register 2 (REG[1C06h]) according to the SDRAM memory size and clock configuration.
4. Configure Memory Configuration Register 0 (REG[1C02h]) according to the SDRAM bus width. The SDRAM can be enabled (REG[1C02h] bit 0) during the same write. Enabling the SDRAM starts the SDRAM initialization process.
5. Wait until the Memory Initialized bit returns a 1b (REG[1C02h] bit 7 = 1b).
6. The SDRAM is now ready for use.

14.1.2 Initializing Mobile SDRAM

The following sequence should be used to initialize mobile SDRAM. For details on specific mobile SDRAM requirements, refer to the Mobile SDRAM specification.

1. Wait at least 100µs after Mobile SDRAM Power Up. (For details, refer to the Mobile SDRAM specification.)
2. Configure Memory Configuration Register 1 (REG[1C04h]) according to the requirements of the Mobile SDRAM used.
3. Configure Memory Configuration Register 2 (REG[1C06h]) according to the Mobile SDRAM memory size and clock configuration.

4. Configure Mobile SDRAM Configuration Register (REG[1C12h]) depending on the Mobile SDRAM extended mode usage. Bit 7 of REG[1C12h] must be set to 1b when Mobile SDRAM is used.

5. Configure Memory Configuration Register 0 (REG[1C02h]) according to the Mobile SDRAM bus width. The Mobile SDRAM can be enabled (REG[1C02h] bit 0) during the same write. Enabling the Mobile SDRAM starts the initialization process.

6. Wait until the Memory Initialized bit returns a 1b (REG[1C02h] bit 7 = 1b).

7. The Mobile SDRAM is now ready for use.

14.2 Memory Bandwidth

There are many S1D13L04 modules that require access to the SDRAM. If too many S1D13L04 modules are required for a given implementation, there may not be enough total bandwidth for all modules to have adequate access to the SDRAM. This situation may result in corruption of the display.

The following guidelines list the maximum color depth (bpp) supported for each listed resolution when minimal modules are required.

Table 14-1: Resolution vs. Color Depth Guidelines

Resolution	Color Depth
	16-Bit Memory Interface
1024x768	16 bpp (see Note)
800x600	16 bpp (see Note)
640x480	32 bpp (see Note)

Note
For 1024x768 and 800x600 resolution displays, only the Main window can be used. For 640x480 resolution displays, if the color depth is 32bpp, it supports only the Main window.

Note that for implementations where multiple modules are required (i.e. Host interface), the resolutions listed above may not be attainable. If a specified resolution and color depth is required and display corruption is visible, increase the Horizontal Total (HT) parameter to the maximum allowed by the panel. If this step does not eliminate the display corruption, it may be necessary to stop using a module with a higher priority than the LCD Controller. The S1D13L04 gives access priority to each module as follows:

1. Host Interface
2. LCD Controller

Chapter 15 Pulse Width Modulation (PWM)

15.1 PWM Circuit Overview

The PWM circuit operates from an approximate 16KHz PWMSRCCLK clock. The clock divider in REG[3402h] allows this PWM clock to be divided by up to 16 to produce the PWM clock. This PWM clock is 16 times the frequency of a PWM cycle, and that PWM cycle has a variable duty cycle as programmed in the PWM Duty Cycle register, REG[340Ch].

The circuit can pulse the LEDs from completely off to the duty cycle programmed in the PWM Duty Cycle register, REG[340Ch]. An LED pulse is created every 128 clocks of the PULSE_clk which is 1/16th the frequency of the PWM clock.

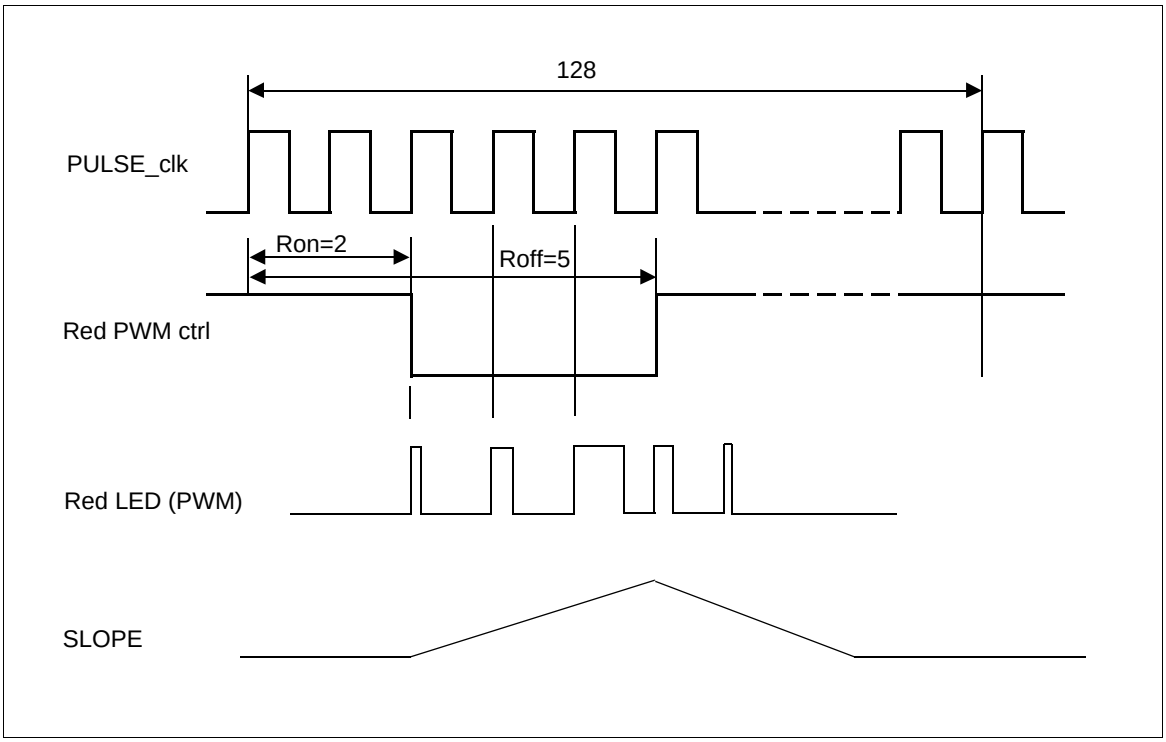

Figure 15-1: PWM Timing Example

In the figure above, the Red on register is programmed to 2 and the Red off register is programmed to 5. If the slope register has a non-zero value, then the PWM duty cycle will ramp up from zero up to the maximum duty cycle programmed in the PWM Duty Cycle register, REG[340Ch].

Notice in the example above, that the PWM circuit may-not have reached its maximum duty cycle (it was still sloping); if the Red off register is programmed with time value that doesn't allow the slope to fully reach the maximum PWM duty cycle, then it is simply truncated and begins sloping down as shown above. It should also be noted that if the PWM Slope register (REG[340Ah]) had been programmed with the value "0", then the PWM output

would have gone immediately from completely off, to the full PWM value programmed in the PWM Duty Cycle register (REG[340Ch]) and then to the completely off state (without sloping through the intermediate PWM duty cycle values).

Below is another example where this time, the slope reaches the maximum duty cycle and stays there until the Red off time arrives. It should be noted that all three PWM circuits are synchronized to the 128 clock period and their cycles are in sync with each other. The Red on and Red off settings are used to adjust the three color LED on/off periods relative to each other.

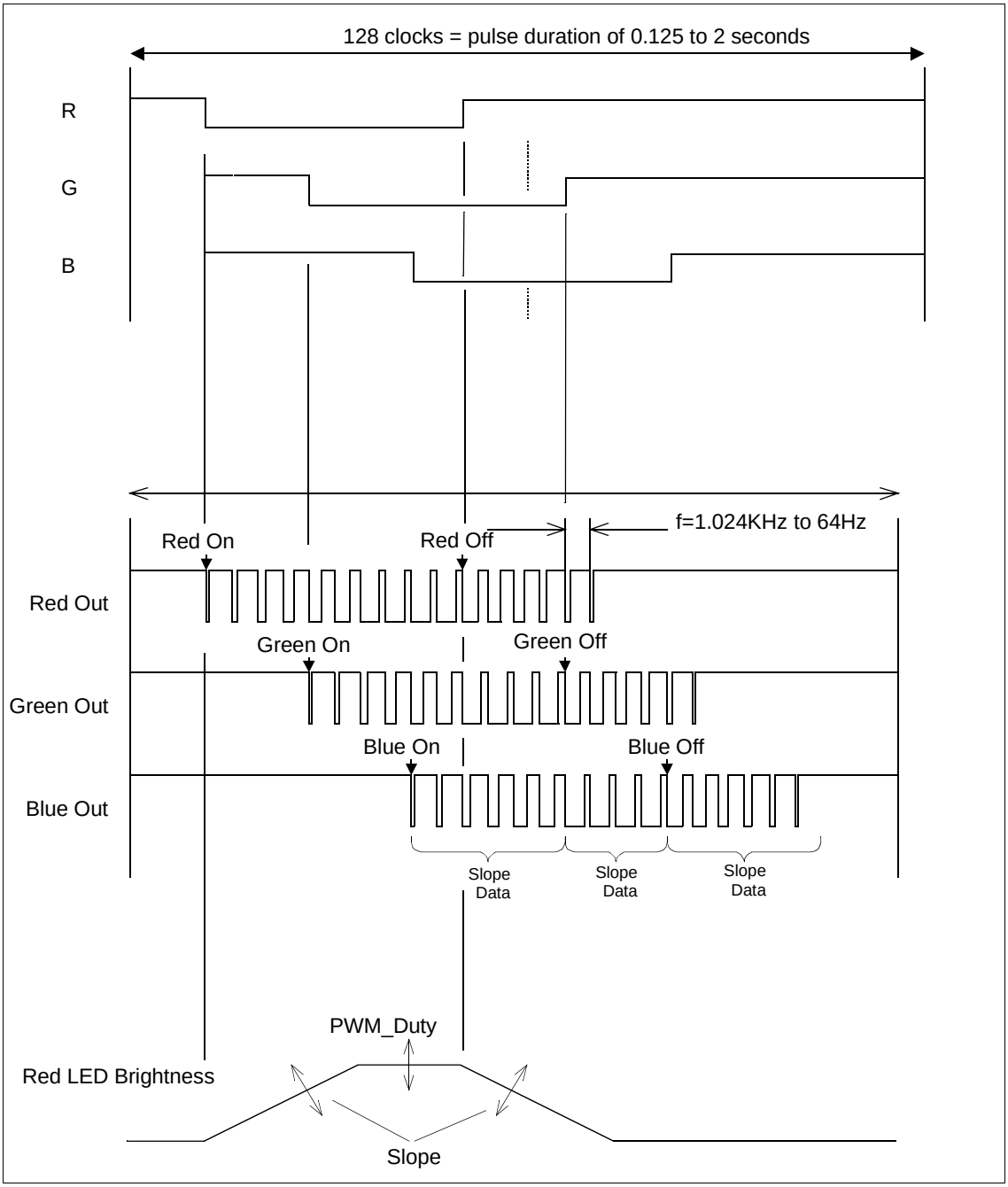

Figure 15-2: PWM Timing Diagram

The White PWM circuit is somewhat different than that of the three color circuits in that it does not have a slope and pulse generation circuit. It is simply turned on to a specific PWM duty cycle or completely turned off.

The clock source for the White PWM circuit is PWMSRCCLK. The period and the duty cycle for the White output are controlled by the White LED Control register, REG[340Eh]. This gives the white PWM output a frequency range of 64Hz to 1Hz, with 64 possible duty cycles.

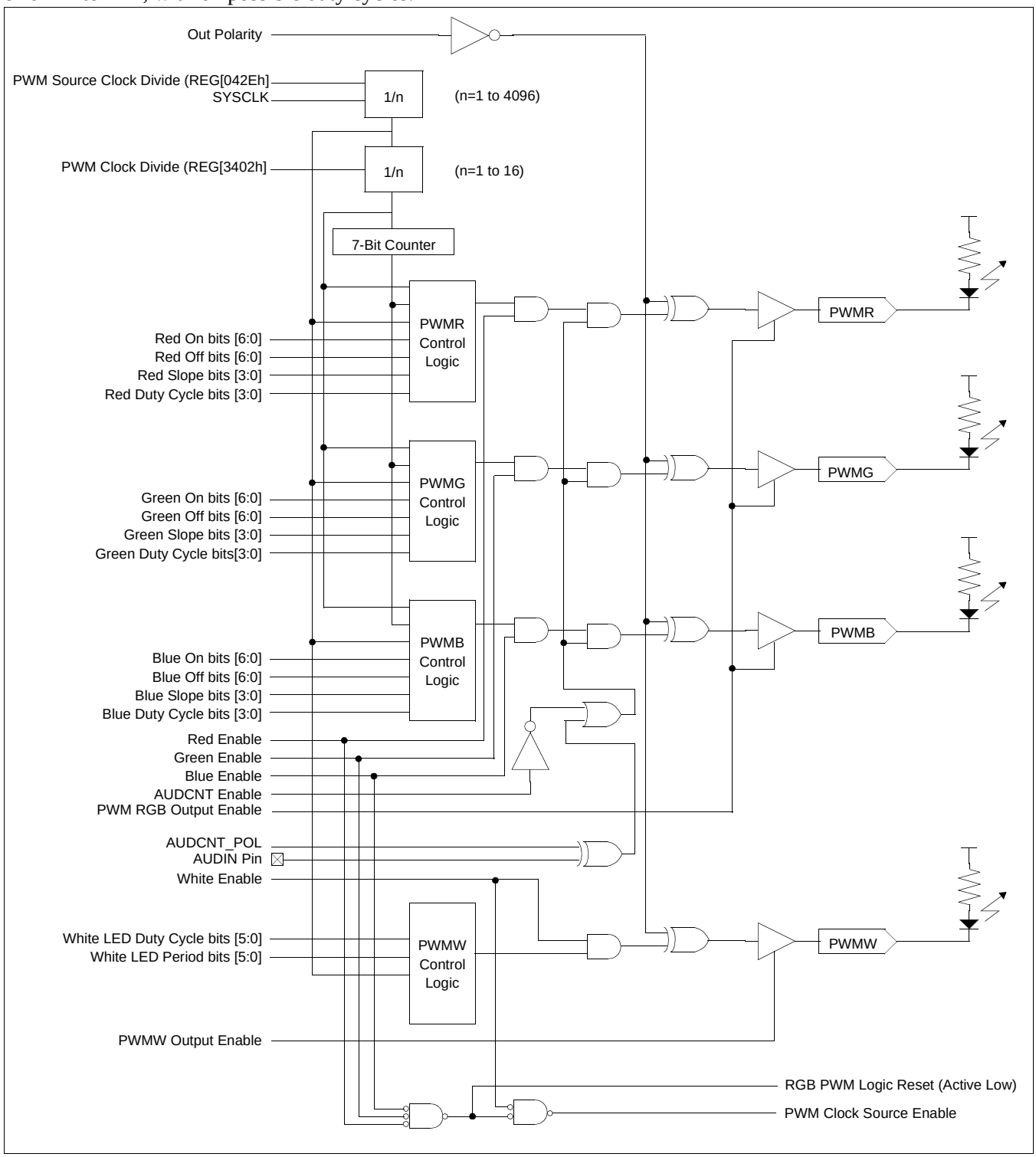

Figure 15-3: PWM Block Diagram

15.2 Other Notes

- The PWM circuit completely shuts down when not in use so users not wanting to make use of it will not suffer any power efficiency degradation when the PWM circuit is idle. For example if REG[3400h] bits 11-8 = 0000b, then the clock to the PWM circuit is completely shut down to prevent any current drain from this circuit.
- HVDD3 is used to supply the output voltage to the output drivers (R,G,B,W)
- All PWM counters and state machines used in the RGB circuit are reset to their initial state when the Red, Green, and Blue PWM enable bits (REG[3400h bits 9, 10, and 11) are ALL turned off (i.e. all three must be zero to reset the PWM reference counters). Since the hardware has no synchronization circuit inside to re-sample the register values that might be being changed by software, it is recommended that the R,G,B PWM circuit be turned off while making changes to the PWM registers. This is not a strict requirement and the circuit will eventually reset to the correct state on the next 128 count cycle, however, strange visual patterns may be seen if the PWM registers are modified mid-cycle while the PWM circuit is operating.
- The AUDIN pin offers further control over the PWM outputs by providing an external input pin. This input pin combined with it’s associated enable bit directly controls the PWM output stage after the PWM circuit.

Chapter 16 Host Interface

16.1 Hardware Configuration

The S1D13L04 is configured using the CNF[8:0] pins which must be connected High through a pull-up resistor or directly to VSS. These configuration pins are used to select the host bus interface type, chip select mode, endian mode, and Clock mode. The state of CNF[8:0] at the rising edge of RESET# determines the configuration of the S1D13L04. Changing the state of CNF[8:0] at any other time has no effect.

For a summary of configuration options, see Section 5.3, “Summary of Configuration Options” on page 29.

16.1.1 Chip Select (1 CS# vs. 2 CS#)

The S1D13L04 supports two types of Chip select mode. Refer to the CNF[5:0] settings for availability of each mode (see Section 5.3, “Summary of Configuration Options” on page 29).

For 1CS# mode, the CS# pin is used for chip select of the S1D13L04 and the M/R# pin is used for space selection between memory and register space.

For 2CS# mode, the CS# pin is used for memory chip select signal (CSM#) of the S1D13L04 and the M/R# pin is used for register chip select signal (CSR#) of the S1D13L04.

Note
Not all of CPU bus types support 2 CS# mode.

16.1.2 Endian Mode

The S1D13L04 supports both big and little endian modes. The endian mode affects the byte lane bus steering of the host data bus.

CNF5 is used to specify the Endian mode as follows.
CNF5 = 0: Little Endian
CNF5 = 1: Big Endian

For a summary, see Section 5.3, “Summary of Configuration Options” on page 29.

Note
When a Big Endian host interface is selected, the memory accesses are byte swapped. Register accesses are not swapped. Therefore, the registers must be accessed using a method which “byte-swaps” the upper and lower data byte in each register. For details on this requirement, see Section 16.6, “Register Accesses for Big Endian Host Interfaces” on page 198.

16.1.3 CNF[4:0]- Host Bus Interface Type

The S1D13L04 supports traditional Mode 80, Mode 68 interfaces.

Mode 80 has two variations that use different combinations of read/write signals (Type 1 and Type 2). Type 1 and Type 2 parallel host interfaces can use either direct or indirect addressing.

When direct addressing is selected, the address is specified with pins AB[20:1]. Indirect addressing specifies the address using an index register.

For a summary of available Host bus interfaces, see Section 5.3, “Summary of Configuration Options” on page 29.

16.1.4 Serial Host Interface Clock Polarity

The serial Host interface can be configured with data valid on either the falling or rising edge.

Table 16-1: Serial Host interface Configuration

CNF[4:0]	HOST Interface type	Valid Edge
10000b	Serial interface	Data valid on falling edge
11000b	Serial interface	Data valid on rising edge

16.2 Host Bus Time-out Function

The S1D13L04 can detect two types of Host Bus Time-out. If enabled, the Host Interrupt Flag (REG[0020h] bit 0) is set when a time-out condition occurs.

16.2.1 Host Read/Write Cycle Time-out

For this type of Host Bus Time-out, a time-out occurs when a Host read or write access to SDRAM exceeds a specified time. This time-out function is supported for both Direct and Indirect host bus interface modes. Both the PCLK Enable (REG[0462h] bit 3) and the HCLK1 Enable (REG[0462h] bit 1) must be enabled for this time-out function to happen.

This Host Bus Time-out is enabled when REG[0024h] bit 7 = 1b. The Host Time-out Value is specified in system clocks and is set using the Host Time-out Value bits, REG[0024h] bits 6-0. If a Host access to SDRAM exceeds this time, the Host Interrupt Flag in REG[0020h] bit 0 is set.

Interrupts can be used to further determine the type of error. Enabling the Memory Read Error and Memory Write Error Interrupts (see REG[0028h] bits 1-0) will set the appropriate flags in REG[0026h] when a Host Time-out occurs. Once the interrupt has been handled, the status flags in REG[0026h] can be cleared by writing a 1b to the corresponding bit.

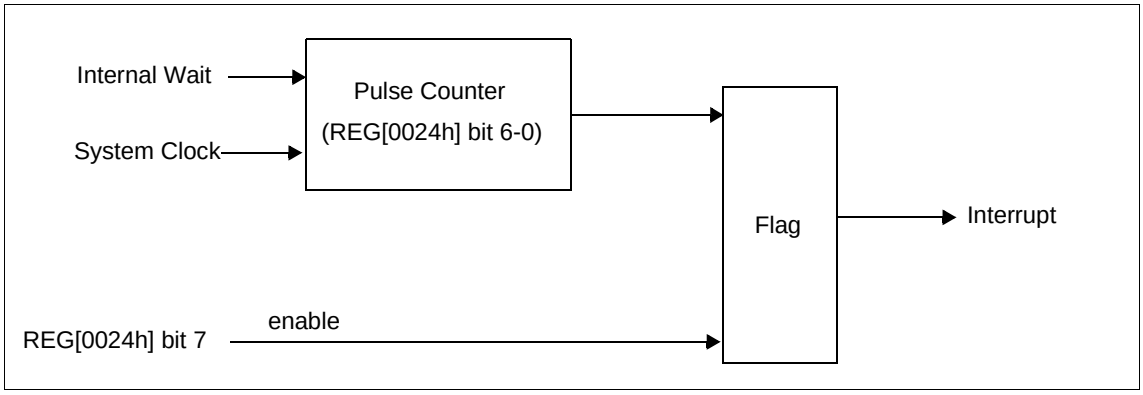

Figure 16-1: Host Read/Write Cycle Time-out Function

16.2.2 Host WAIT# Length Time-out

For this type of Host Bus Time-out, a time-out occurs if the S1D13L04 holds WAIT# for more than 2000 Source Clocks. This time-out function is supported for both Direct and Indirect host bus interface modes. The Source Clock is selected using the CNF[8:7] pins.

This Host Bus Time-out is disabled by default. However, the S1D13L04 can be configured to use this function to automatically reset when this time-out occurs by setting the Bus Time-out Reset Disable bit to 0b (REG[0472h] bit 0 = 0b). When enabled, the Bus Time-out Reset Interrupt Flag is set in REG[0472h] bit 2 if the time-out condition occurs and the interrupt is enabled (see REG[0472h] bit 1). The flag can be cleared by disabling the Bus Time-out Reset Interrupt (REG[0472h] bit 1 = 1b).

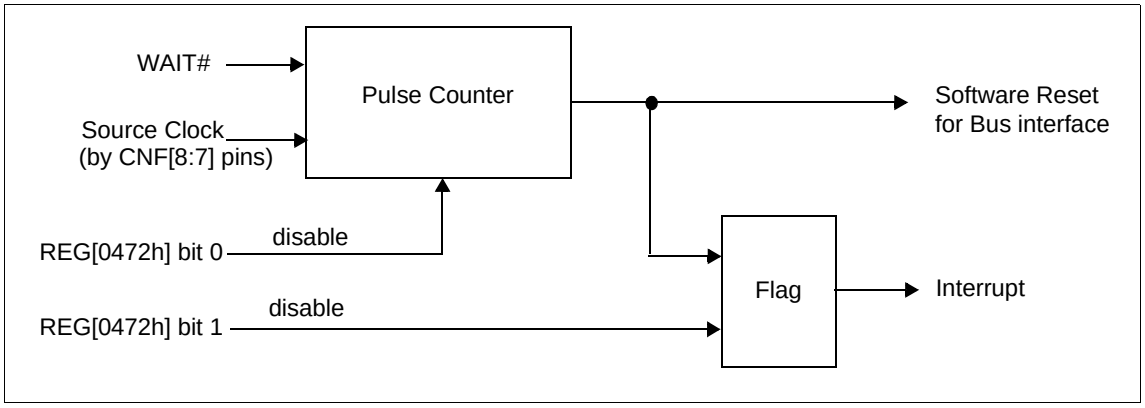

Figure 16-2: Host WAIT# Length Time-out Function

16.3 Indirect Interface

The S1D13L04 supports Indirect host interfaces which use a different method of addressing the registers/memory. The following sections provide example sequences for each access type.

Table 16-2: Indirect Interface Port

AB[2]	AB[1]	RD_x	WR_x	Register Name
0	0	0	1	Index Register
0	0	1	0	Index Register
0	1	0	1	Status Register
0	1	1	0	Reserved
1	0	0	1	Data register
1	0	1	0	Data register
1	1	0	1	Reserved
1	1	1	0	Reserved

Note
The name of RD_x, WR_x may be different, depending on the Host Bus type.

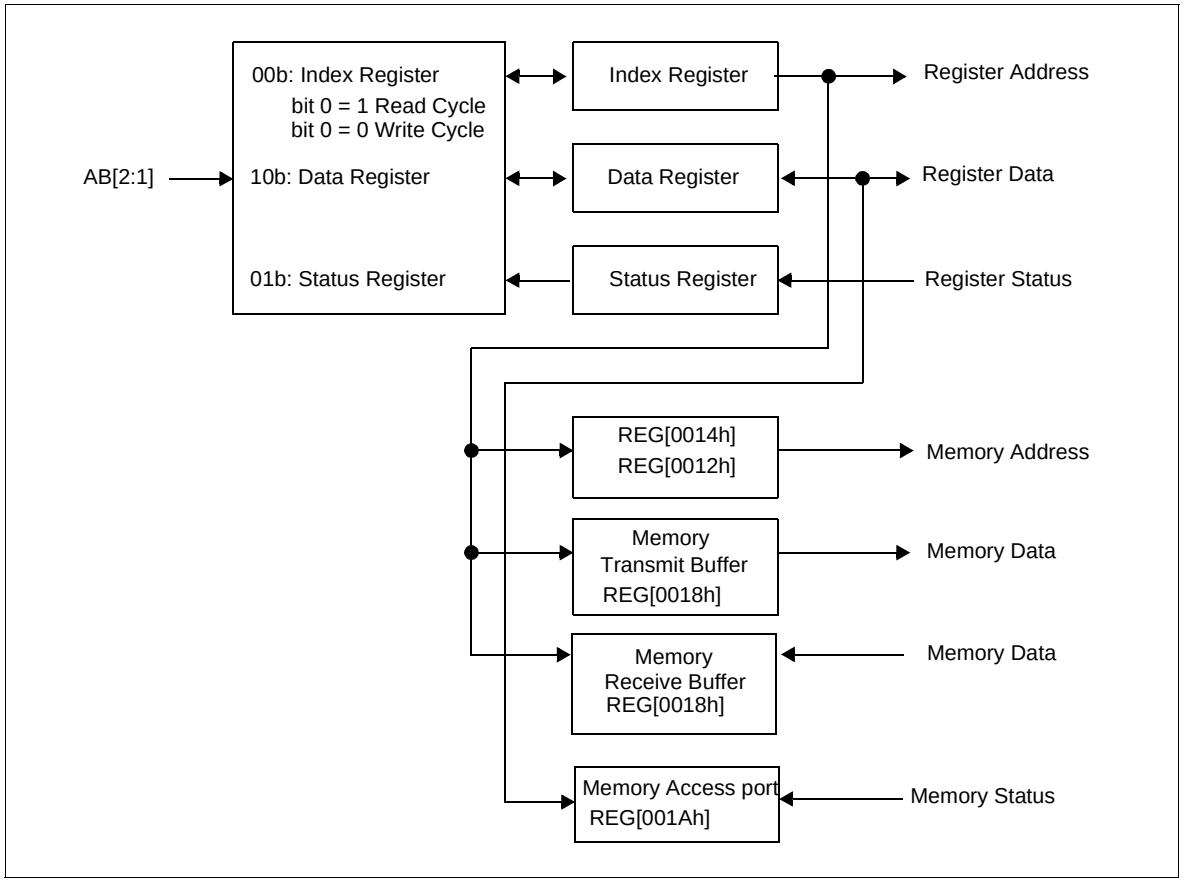

Figure 16-3: Indirect Interface Block Diagram

16.3.1 Indirect Addressing for Register Access

AB[2:1] = 00b Indirect Interface Index Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Register Address bits 15-8							
7	6	5	4	3	2	1	0
Register Address bits 7-1							Read/Write Cycle Select

bits 15-1 Register Address bits [15:1]
These bits are used for Parallel Indirect Interface modes only.
These bits set the register address for the indirect interface.

bit 0 Read/Write Cycle Select
This bit is used for Parallel Indirect Interface modes only.
This bit selects whether a read or a write is performed for the next data port access.
When this bit = 0, a write is performed.
When this bit = 1, a read is performed.

AB[2:1] = 01b Indirect Interface Status Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							Memory Status

bit 0 Memory Status (Read Only)
This bit is used for Parallel Indirect Interface modes only.
This bit indicates the status of the Memory Controller. The status of this bit must be checked before accessing the memory, however confirmation for continuous memory accesses is not necessary.
When this bit = 0b, the memory controller is idle and the Host CPU can access memory.
When this bit = 1b, the memory controller is busy and the Host CPU cannot access memory.

AB[2:1] = 10b Indirect Interface Data Port Register Default = 0000h							Read/Write
Indirect Interface Data Port bits 15-8							
15	14	13	12	11	10	9	8
Indirect Interface Data Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Indirect Interface Data Port bits [15:0]

These bits are used for Parallel Indirect Interface modes only.

These bits are used for read/write data transfers to the register address specified by bits 15-1 of the Indirect Interface Index Register, AB[2:1] = 00b.

16.3.2 Register Access

When the indirect host interface is selected, register accesses should follow the procedure below.

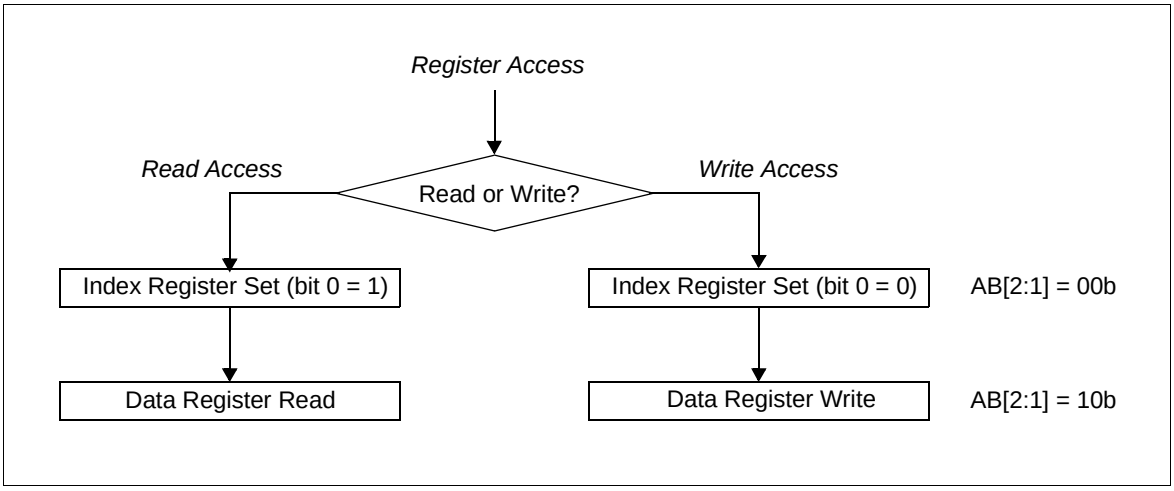

Figure 16-4: Register Access

16.3.3 Memory Access

When the indirect host interface is selected, memory accesses should follow the procedure below. When a memory read or write error occurs, re-start by setting the address again as the byte cannot be accessed.

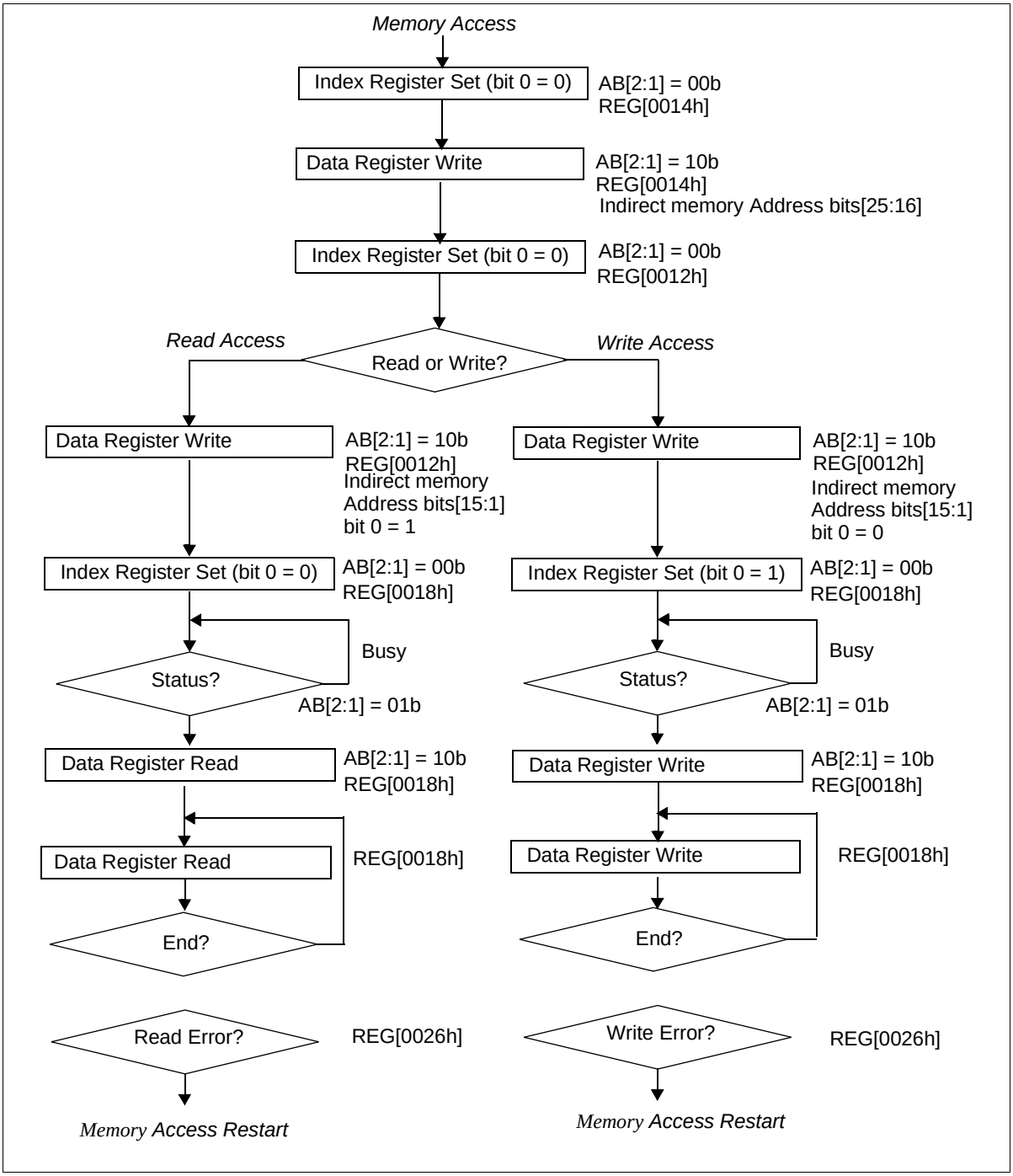

Figure 16-5: Memory Access

16.4 Read Ahead Feature

The Host interface includes a prefetch buffer which accelerates memory accesses by “reading ahead”. When a single read is issued from the Host interface, the S1D13L04 internally reads memory using a burst transfer. The read data is saved in the prefetch buffer. If the next read address is a +2 address to the previous read address, the Host interface can return the data immediately without a new memory read access. This method provides much faster access as long as the memory address is incremented by 2 each time.

The prefetch buffer is cleared when the following occurs:

- a memory write access occurs
- the next read address is not a +2 address to the previous read address

16.5 Serial Interface

The S1D13L04 supports three types of Host CPU interface - parallel direct, parallel indirect, and serial indirect. The serial host interface uses a different method of addressing the registers/memory than the parallel interfaces. The following sections show example sequences for each access type.

16.5.1 Description

The S1D13L04 Serial Host Interface supports the following.

- 16-bit transfers
- maximum frequency of 16MHz
- write and read data transfers
  - single transfers
  - burst transfers for the Memory
- reading the indirect interface status
- sending the MSB first

Five signals are used for the serial interface.

- SI: Serial Data In
- SO: Serial Data Out
- SCK: Serial Clock
- CS#/SCS#: Serial Chip Select
- SA0: Command / Data Select (0 = command, 1 = data)

The SA0 Command / Data pin is used to distinguish between data transfers and command transfers. Command transfers are used to initiate either a Read, Write, or Get Status transfer as follows.

Table 16-3: Serial Host Interface Commands

Command	Value	Function
CMD_WRITE	0000h	Start Write Cycle
CMD_READ	4000h	Start Read Cycle
CMD_END	8000h	End Cycle
CMD_STATUS	C000h	Read Indirect Interface Status

The Serial Host Interface uses the Indirect Data Bus in the S1D13L04 to set the register address and read/write data. The Serial Host Interface has access to the Indirect Interface Status Register which can be read using the CMD_STATUS command. This returns the Memory Status.

The Serial Data Out pin (SO), is Hi-Z when CS# is high and is active when CS# is low.

16.5.2 Burst Mode Operation

Serial host interface burst mode allows the CS# line to be held low and then continuously send or receive data to/from the S1D13L04.

CS# can either be held low between each 16-bit transfer or it can be toggled, but it must change from high to low before the Command portion of the transfer.

The following figure shows burst mode when CS# is held low.

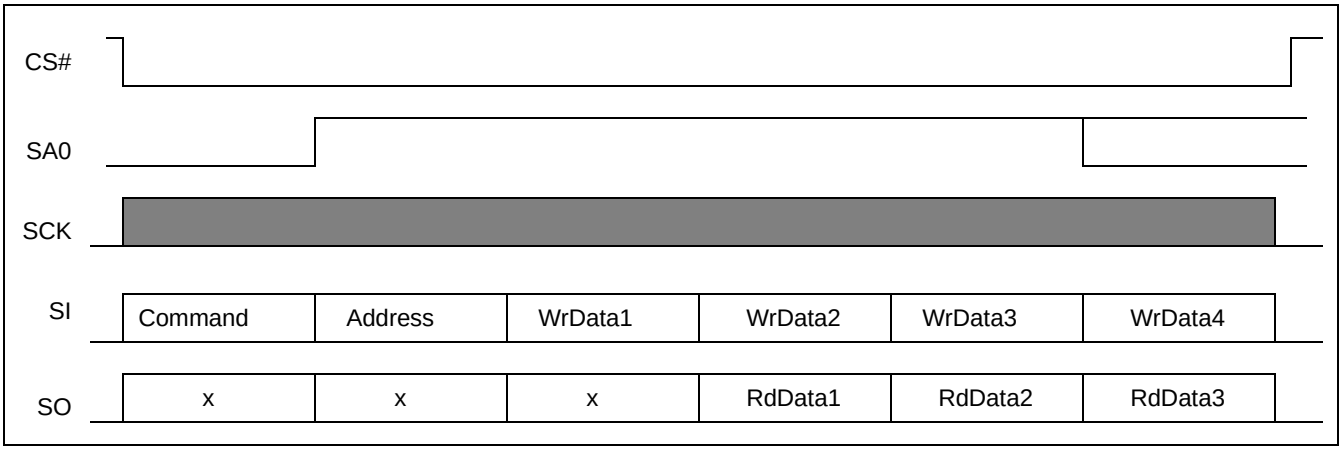

Figure 16-6: Serial Host Interface Burst Mode for CS# Held Low

The following figure shows burst mode when CS# is toggling.

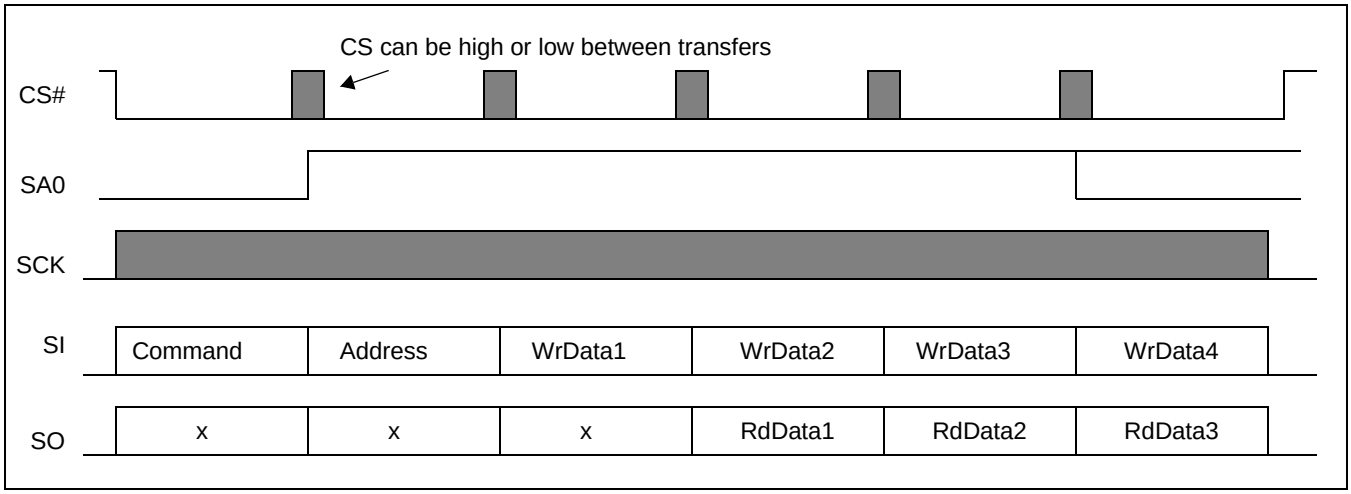

Figure 16-7: Serial Host Interface Burst Mode for CS# Toggling

Note
If CS# goes high between transfers, then it must be held high for at least one SCK period between the last bit and first bit.

16.5.3 Data Transfer Examples

In the following examples X = unknown data

Writing Single Data

1. Send the Write Command.
2. Send the register address where data is to be written.
3. Send the data to be written.

Table 16-4: Writing Single Data

SA0	Data Sent	Data Received
0	CMD_WRITE	X
1	Register address where data is to be written	X
1	Data to be written	X
0	CMD_END	

Writing Burst Data

1. Send the Write Command.
2. Send the register address where data is to be written.
3. Send the data to be written.
4. Repeat step 3 until all data has been written.

Table 16-5: Writing Burst Data

SA0	Data Sent	Data Received
0	CMD_WRITE	X
1	Register address where data is to be written	X
1	Data to be written	X
1	Data to be written	X
...	...	...
1	Data to be written	X
0	CMD_END	

Reading Single Data

1. Send the Read Command.
2. Send the register address that data is to be read from.
3. Write a value. This performs the read operation and captures the data from the specified address.
4. Send the Read End command. This returns the data previously captured and does not perform another read from the register address.

Table 16-6: Reading Single Data

SA0	Data Sent	Data Received
0	CMD_READ	X
1	Register address to read data from	X
1	0	X
0	CMD_END	Read Data from previous read

Reading Burst Data

1. Send the Read Command.
2. Send the register address that data is to be read from.
3. Write a value. This performs the read operation and captures the data from the specified address.
4. Write another value. This returns the data captured from the previous read and performs another read at the same address which captures the data.
5. Repeat step 4 until all the data minus 1 has been read.
6. Send the Read End command. This returns the data previously captured and does not perform another read from the register address.

Table 16-7: Reading Burst Data

SA0	Data Sent	Data Received
0	CMD_READ	X
1	Register address to read data from	X
1	0	X
1	0	Read Data from previous read
1	...	Read Data from previous read
...	...	...
0	CMD_END	Read Data from previous read

Reading the Indirect Interface Status

1. Send the Status Command.
2. Send the Read End command. This returns the Indirect Status.

Table 16-8: Reading the Indirect Interface Status

SA0	Data Sent	Data Received
0	CMD_STATUS	X
0	CMD_END	Indirect Status

Note
For details on the information returned in the Indirect Interface Status register, see Section 16.3.1, “Indirect Addressing for Register Access” on page 187.

16.5.4 Indirect Register Address Auto Increment Serial Examples

Write 8 words to LUT1 starting at address 400h.

Host Bus Cycle	S1D13L04 Operation
Send Command Write	
Set Address to 400h	Set Indirect Address to 0400h
Send Data = 1234h	Write 1234h to Address 0400h
Send Data = 0056h	Write 0056h to Address 0402h
Send Data = 789Ah	Write 789Ah to Address 0404h
Send Data = 00BCh	Write 00BCh to Address 0406h

Write 2 words to address 210h and 212h and then 2 words to address 218h and 21Ah.

Host Bus Cycle	S1D13L04 Operation
Send Command Write	
Set Address to 0210h	Set Indirect Address to 0210h
Send Data = 1234h	Write 1234h to Address 0210h
Send Data = 5678h	Write 5678h to Address 0212h
Send Command Write	
Set Address to 0218h	Set Indirect Address to 0218h
Send Data = 1234h	Write 1234h to Address 0218h
Send Data = 5678h	Write 5678h to Address 021Ah

Read 3 words from address 220h to 224h.

Host Bus Cycle	S1D13L04 Operation
Send Command Read	
Set Address to 0220h	Set Indirect Address to 0220h
Read Dummy Data	Read from Address 0220h
Read Data from address 220h	Read from Address 0222h
Read Data from address 222h	Read from Address 0224h
Send Command Read End and Read	
Data from address 224h	

16.6 Register Accesses for Big Endian Host Interfaces

When a Big Endian host interface is selected (see Section 5.3, “Summary of Configuration Options” on page 29), the registers must be accessed using a method which “byte-swaps” the upper and lower data byte in each register. This requirement applies for both read and write accesses.

For example, reading a certain register which has the value of 0A05h in the S1D13L04 from a Little Endian host will return 0Ah from the upper byte (bits 15-8) and 05h from the lower byte (bits 7-0). If no adjustments are made, a Big Endian host will read the same register and return 05h from the upper byte and 0Ah from the lower byte. This would result in a read out data of 050Ah which is byte swapped. Register writes must also be adjusted or the S1D13L04 will be configured incorrectly.

The following code provides an example of how the required byte-swap can be performed.

```
#define BIG_ENDIAN
#undef  LITTLE_ENDIAN

#if defined(LITTLE_ENDIAN) && !defined(BIG_ENDIAN)

               #define BYTE_SWAP(x) (x)

#elif defined(BIG_ENDIAN) && !defined(LITTLE_ENDIAN)

               #define BYTE_SWAP(x) ((((UInt16)(x) & 0xFF) << 8) | (((UInt16)(x) &
0xFF00) >> 8 ))

#else

#error "Please define either BIG_ENDIAN or LITTLE_ENDIAN."

#endif


UInt16 seReadReg16( UInt32 Index )
{
               UInt16 val =  *(UInt16*)(gRegisterAddress + Index);
               return BYTE_SWAP(val);
}

void seWriteReg16( UInt32 Index, UInt16 Value )
{
               *(UInt16*)(gRegisterAddress + Index) = (UInt16)(BYTE_SWAP(Value));
}
```

Chapter 17 LCD Panel Interface

The S1D13L04 stores image data in external SDRAM memory for output to a single panel including the following LCD panel types.

- 16/18-bit TFT/ND-TFD (includes serial command interface support)
  - ND-TFD 4-pin interface (8-bit)
  - ND-TFD 3-pin interface (9-bit)
  - µ-Wire TFT interface (16-bit)
  - 24-bit Serial interface
  - Serial command interface has configurable bit direction, phase, and polarity
- For information on supported resolutions, see Section 14.2, “Memory Bandwidth” on page 176

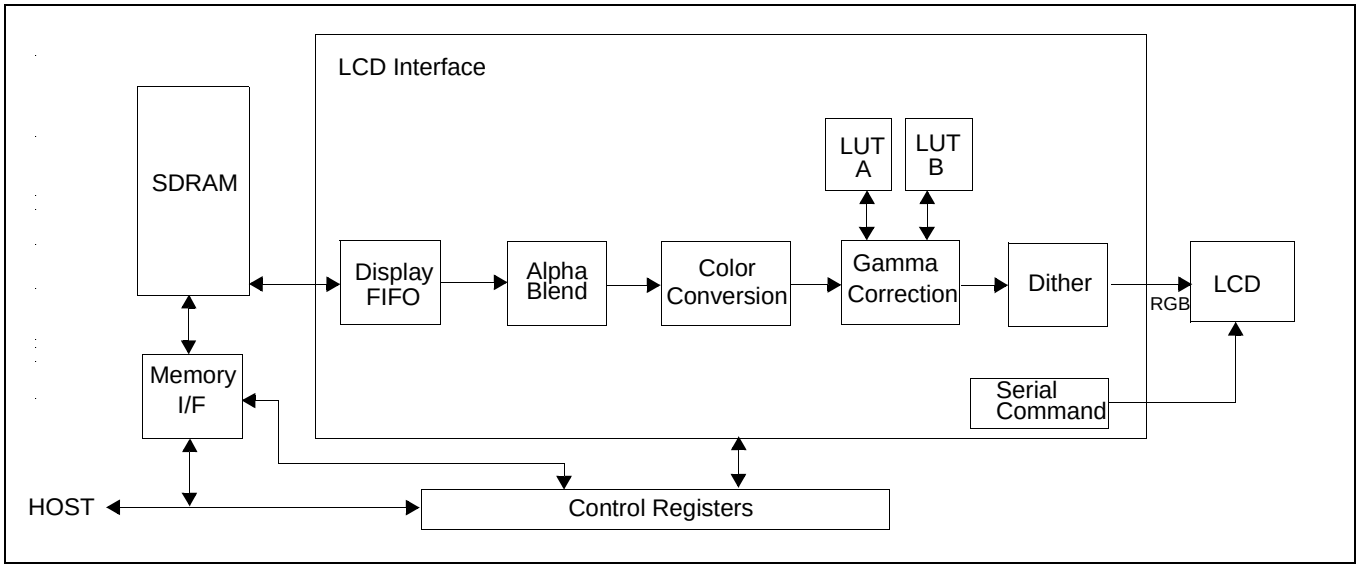

Figure 17-1: LCD Interface Overview

17.1 TFT/ND-TFD Panels

A TFT/ND-TFD RGB interface panel is selected when REG[0800h] bit 14 = 0b and REG[0800h] bits 2-0 = 000b. Data bus widths of 16, and 18-bits are supported and selected using REG[0800h] bits 10-8. For some TFT panel types a Serial Command Interface is used to issue command/parameter information to the panel. The type of Serial Command Interface is selected using REG[0816h] bits 7-5.

For pin mapping details, refer to Section 5.5, “LCD Interface Pin Mapping” on page 33.

17.1.1 TFT/ND-TFD Data Output Formats

The following information shows the data output formats for each panel data bus width.

- 16-bit RGB interface LCD panel RGB 5:6:5 (REG[0800h] bits 10-8 = 001b)
- 18-bit RGB interface LCD panel RGB 6:6:6 (REG[0800h] bits 10-8 = 010b)

17.1.2 RGB Serial Command Interfaces

Table 17-1: 16/18-Bit TFT/ND-TFD Data Output Formats

S1D13L04 Pin	16-Bit	18-Bit
FPDAT0	R^4	R^5
FPDAT1	R^3	R^4
FPDAT2	R^2	R^3
FPDAT3	G^5	G^5
FPDAT4	G^4	G^4
FPDAT5	G^3	G^3
FPDAT6	B^4	B^5
FPDAT7	B^3	B^4
FPDAT8	B^2	B^3
FPDAT9	R^1	R^2
FPDAT10	R^0	R^1
FPDAT11	Low	R^0
FPDAT12	G^2	G^2
FPDAT13	G^1	G^1
FPDAT14	G^0	G^0
FPDAT15	B^1	B^2
FPDAT16	B^0	B^1
FPDAT17	Low	B^0

When a RGB interface panel with a serial command interface is selected (see REG[0816h] bits 7-5, the GPIOG[3:0] pins are used according to the serial command interface type.

- General TFT panel (REG[0816h] bits 7-5 = XXXb)
- ND-TFD 4-pin panel (REG[0816h] bits 7-5 = 000b)
- ND-TFD 3-pin panel (REG[0816h] bits 7-5 = 001b)
- a-Si TFT panel (REG[0816h] bits 7-5 = 010b)
- µ-Wire TFT panel (REG[0816h] bits 7-5 = 100b)
- 24-bit serial data RGB interface LCD panel (REG[0816h] bits 7-5 = 101b)

Table 17-2: RGB Serial Command Interfaces Pin Usage Summary

Interface Type	S1D13L04 Pin			
	GPIOG0	GPIOG1	GPIOG2	GPIOG3
General TFT	—	—	—	—
ND-TFD 4-pin	XCS	SCK	A0	SO
ND-TFD 3-pin	XCS	SCK	—	SO
a-Si TFT	SSTB	SCLK	—	SDATA
uWIRE TFT	LCDCS	SCLK	—	SDO
24-bit Serial TFT	XCS	SCK	—	SO

For timing details, refer to Section 7.6, “Panel Interface Timing” on page 53.

17.1.3 TFT/ND-TFD Programming Flow

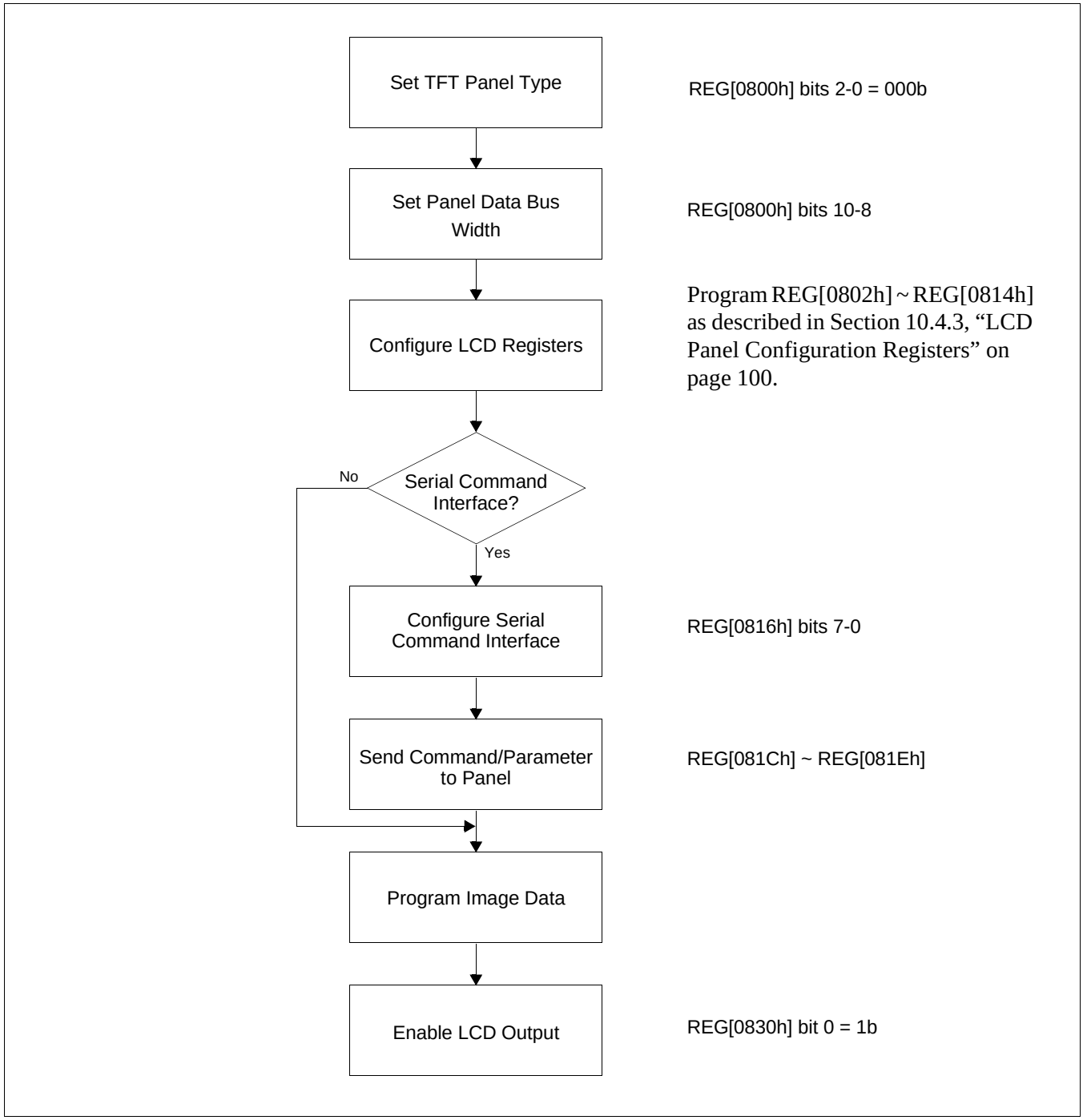

Figure 17-2: TFT/ND-TFD Programming Flow

Chapter 18 Crystal Oscillator Circuit

The S1D13L04 is designed with two crystal oscillation circuits which can be used as clock sources. For details on the clocks, see Section Chapter 9, “Clocks” on page 69.

The oscillation characteristics depend on the components used in the circuit (i.e. X’tal, Rf, Rd, Cg, Cd, and board characteristics). An example circuit and example component values are shown below. Actual values used must be confirmed for each implementation.

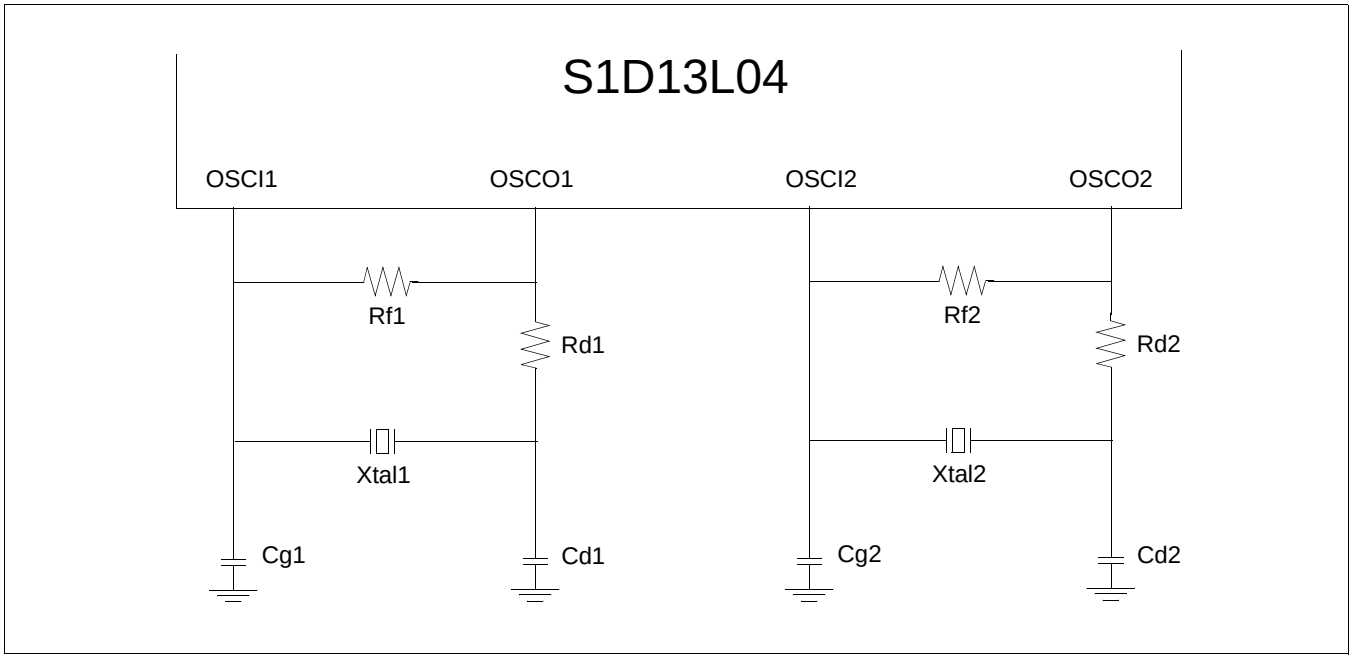

Figure 18-1: Recommended Crystal Oscillator External Circuit

Table 18-1: Recommended Crystal Oscillator External Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Units
Rf1	Rf1	—	1	—	MΩ
Rd1	Rd1	—	0	—	W
Cg1	Cg1	—	10	—	pF
Cd1	Cd1	—	10	—	pF
Xtal1	Fundamental mode crystal	5	—	20	MHz
Rf2	Rf2	—	1	—	MΩ
Rd2	Rd2	—	0	—	W
Cg2	Cg2	—	5	—	pF
Cd2	Cd2	—	5	—	pF
Xtal2	Fundamental mode crystal	5	—	27	MHz

Chapter 19 Design Considerations

19.1 Guidelines for PLL Power Layout

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL, resulting in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

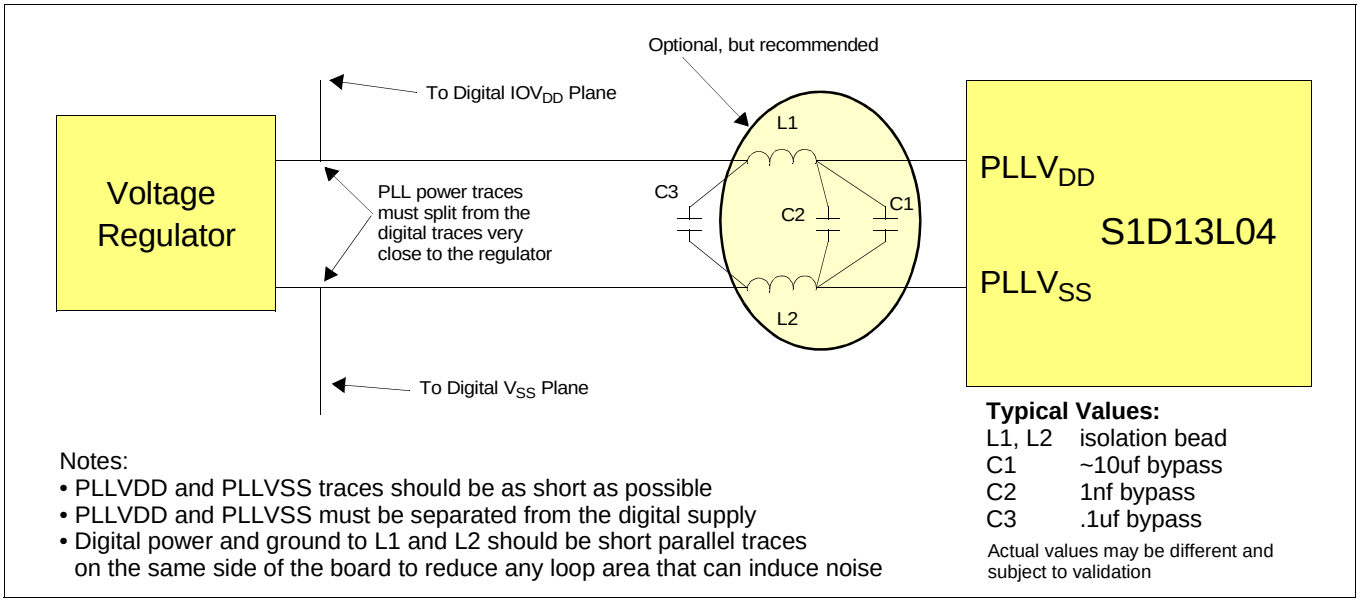

Figure 19-1: PLL Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L1) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the S1D13L04 ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.
- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.

- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

Chapter 20 Mechanical Data

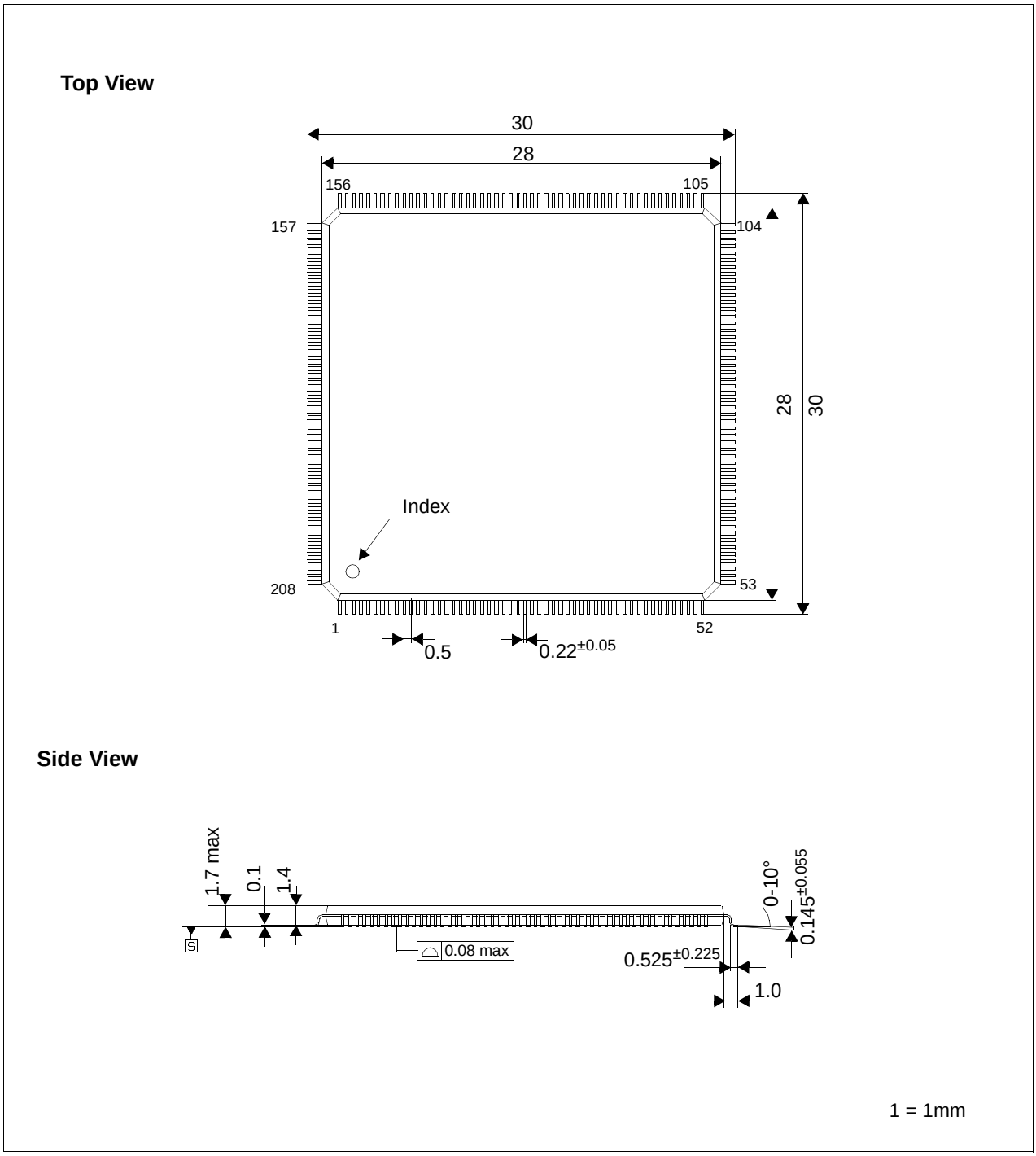

Figure 20-1: S1D13L04 QFP22 208-pin Package

Chapter 21 References

The following documents contain additional information related to the S1D13L04. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Electronics America website at **http://vdc.epson.com**.

- S1D13L04 Product Brief (XB3A-C-001-xx)

Change Record

XB3A-A-001-00 Revision 1.00 - Issued: March 18, 2016

- initial release of document

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Document Code: XB3A-A-001-01
Issued 2016/03/18